FAIRCHILD SEMICONDUCTOR™

August 1993
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Design Considerations

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Interfacing

Interfacing the low voltage and VHC/VHCT families with other technologies is made easier since their input structures are constructed without the input protection diodes to V_{CC}. This layout allows logic functions to reside between systems powered by independent supplies.

Also, the output pull-up for the VHCT family is a N-Channel device which eliminates the output protection diode to V_{CC}. This configuration will ease 3-STATE bus interfacing between CMOS and VHCT.

See Figure 1 to Figure 6 for VHC/VHCU/VHCT interfaces.

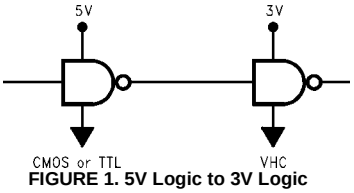


FIGURE 1. 5V Logic to 3V Logic

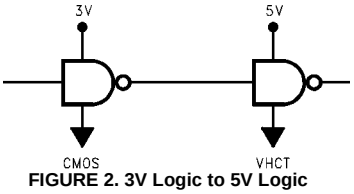


FIGURE 2. 3V Logic to 5V Logic

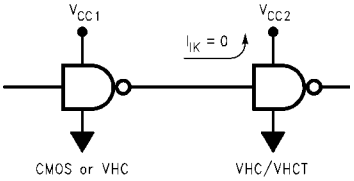


FIGURE 3. (V_{CC1} > or < V_{CC2})

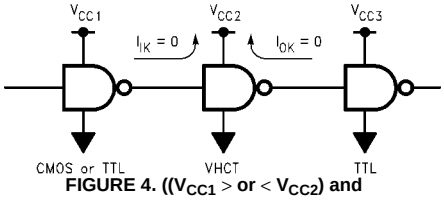


FIGURE 4. ((V_{CC1} > or < V_{CC2}) and (V_{CC2} > or < V_{CC3}))

ECL devices cannot directly drive CMOS/LVTTL devices. Interfacing CMOS/LVTTL-to-ECL can be accomplished by using a F100324 TTL-to-ECL translator and a F100325 ECL-to-TTL translator. Note, a resistor pull-up to V_{DD} of approximately 4.7 kΩ is required for ECL to VHC/VHCU interfacing.

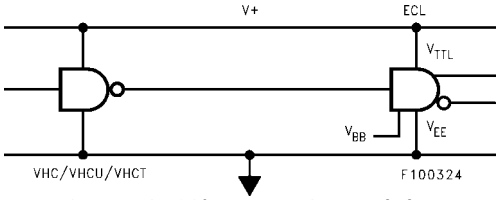


FIGURE 5. CMOS/LVTTL-to-ECL Translation

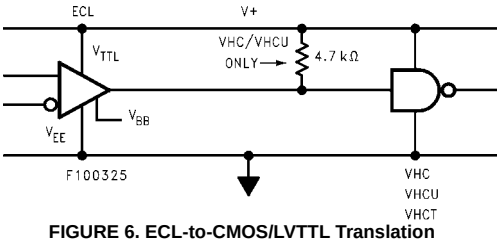


FIGURE 6. ECL-to-CMOS/LVTTL Translation

It should be understood that for LVX/LCX/VCX/VHC, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z'_o, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z'_o and t_{pde} can be calculated with:

$$Z'_o = \frac{Z_o}{\sqrt{1 + C_D/C_L}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_D/C_L}$$

where C_L = intrinsic line capacitance and C_D = additional capacitance due to gate loading.

Line Driving and Termination (continued)

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

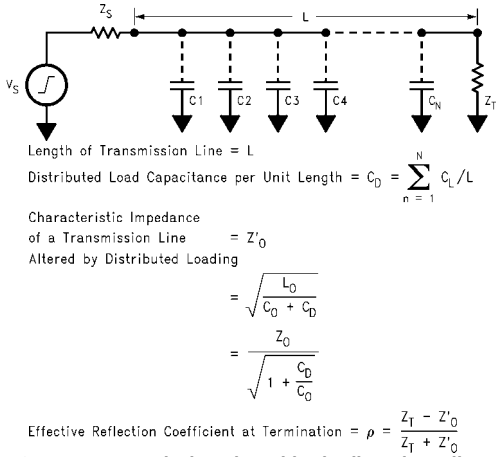


FIGURE 7. Transmission Line with Distributed Loading

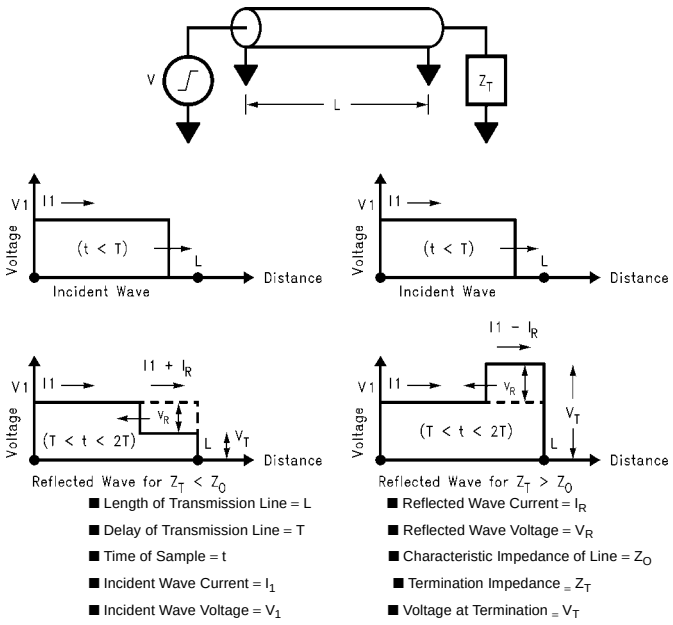


FIGURE 8. Reflections Due to Impedance Mismatching

There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave, V_i. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of the line according to the formula

$V_i = V_{DD} \bullet Z'_o/(Z'_o + R_S + Z_S)$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{DD} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

THEVENIN TERMINATION

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{DD} or ground, increasing power consumption.

- Parallel: Resistor = Z_0
- Thevenin: Resistor = 2 x Z_0
- Series: Resistor = $Z_0 - Z_{OUT}$
- AC: Resistor = Z_0, Capacitor = $C \geq \frac{3tr}{Z_0}$

FIGURE 9. Suggested Termination Values

74LCX245 I_{CC} vs Frequency for Various Terminations

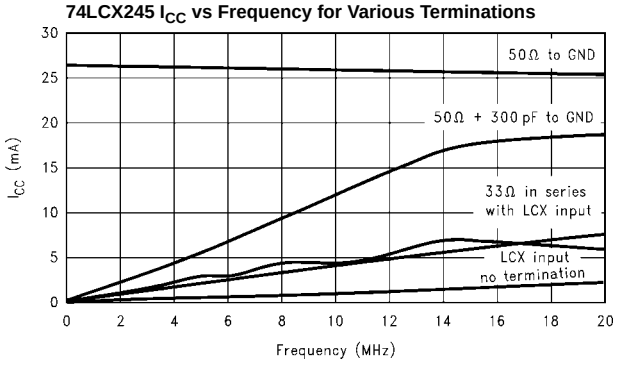


FIGURE 10. LCX I_{CC} vs. Termination

Line Driving and Termination (continued)

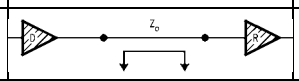
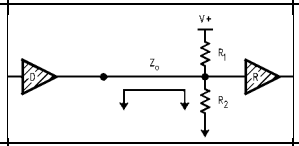
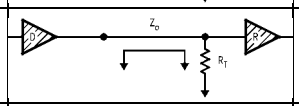
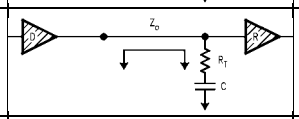
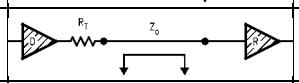
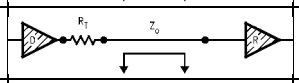
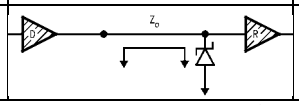
Type	Description	Extra Devices	Power Increase	t_{PD} Penalty	Ideal Value	Comments
NONE		1	NO	~0.0 ns		Low Power - Poor Long Line Performance
THEVENIN		2	YES	~0.0 ns	$R_1 = R_2 = 2Z_O$	High Power - Good for Backplanes
PARALLEL		1	YES	~0.0 ns	$R_T = Z_O$	High Power - Low DC Noise Margin
AC		2	YES	~0.0 ns	$R_T = Z_O$60 <C <330 pF	Medium Power - Increases with Frequency
On-Chip SERIES		0	NO	~0.7 ns	$R_T = Z_O - Z_D$	Low Power - Low Noise
Discrete SERIES		1	NO	~1.0 ns	$R = Z_O - Z_D$	Low Power - Low Noise
DIODE		1	NO	~0.0 ns		Compliments standard backplane terminators

FIGURE 11. Termination Circuits

Fairchild's *CROSSVOLT*™ circuits have been designed to drive 75Ω transmission lines over the full commercial temperature range. This is guaranteed by the specified dynamic drive capability of 36 mA source and 25 mA sink current. This ensures incident wave switching on 75Ω transmission lines and is consistent with the 3 ns rated edge transition time.

Fairchild's *CROSSVOLT* product inputs take advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 2.0V and 0.8V respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50 µA or less. These noise margins are outlined in Figure 12.

FIGURE 12. LCX Input Threshold

Noise Effects

Fairchild's *CROSSVOLT* families offers excellent noise immunity. With input thresholds specified at 2.0V and 0.8V and outputs that drive to within 100 mV of the rails, *CROSSVOLT* devices offer noise margins approaching 30% of V_{DD}. At 3.3V V_{DD}, *CROSSVOLT* specified input and output levels give almost 1.0V of noise margin for both ground- and V_{DD}-born noise. With realistic input thresholds closer to 50% of V_{DD}, the actual margins approach 1.5V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the performance of *CROSSVOLT* circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

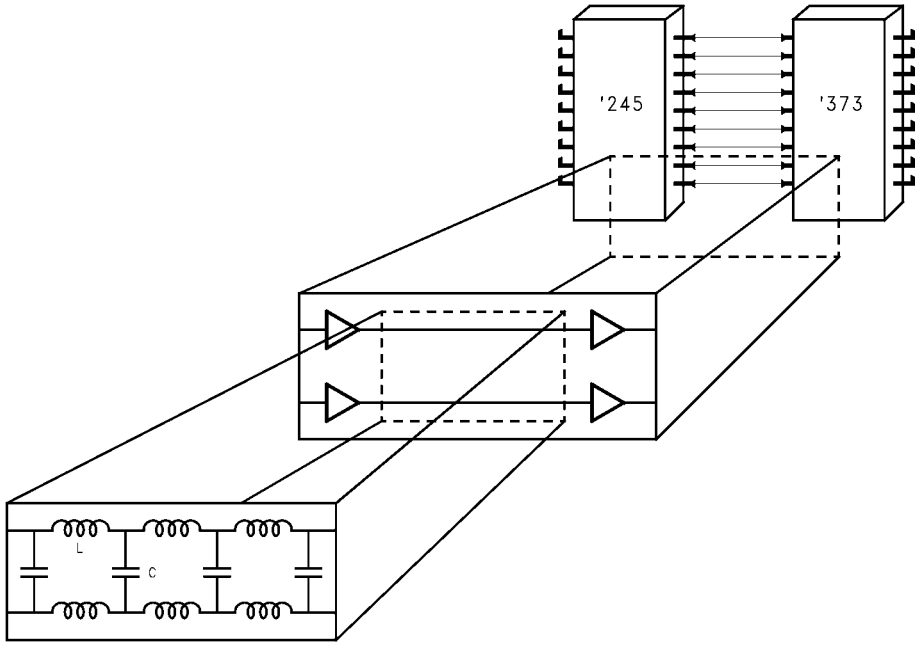
The problem of crosstalk and how to deal with it has become more important as system performance and board densities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent (Figure 13).

Crosstalk has two basic causes. Forward crosstalk, Figure 14 and Figure 16, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (ϵ_r = 1.0) and epoxy glass (ϵ_r = 4.7).

As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figure 15 and Figure 17, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

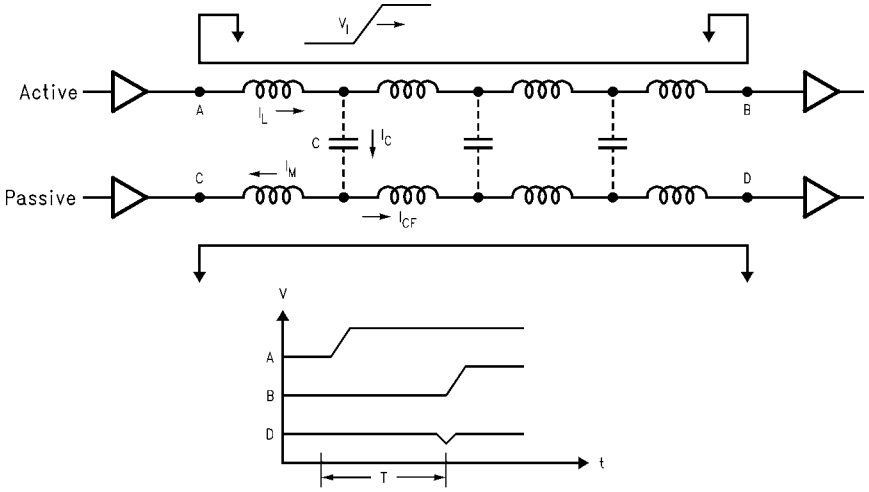
Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. *CROSSVOLT*'s AC noise margins, shown in Figure 20, show the immunity to everyday noise which can effect system reliability.



■ Two parallel signal lines provide mutual inductance and shunt capacitance.

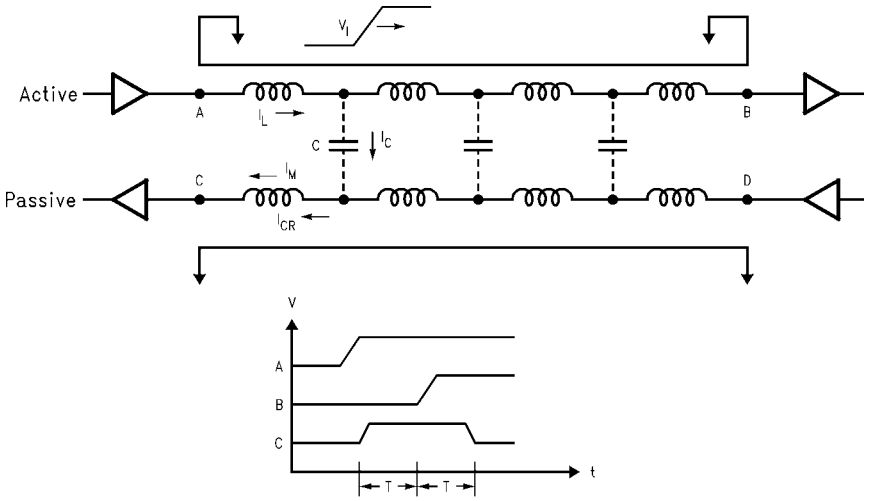
FIGURE 13. Where Does Crosstalk Take Place?

Crosstalk (continued)



- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = $I_C = -C\,\Delta V_I/\Delta t$
- Mutually Induced Current = $I_M = mI_L$
- Forward Crosstalk Current = I_{CF}
- As the active signal, V_i, propagates from A to B a negative-going spike, V_f, propagates fro C to D, coincident with V_i

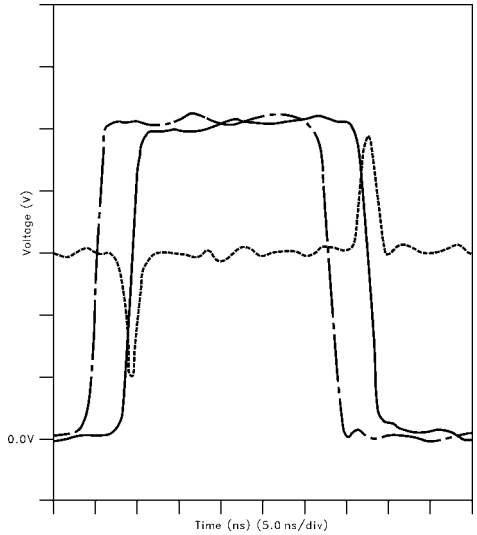
FIGURE 14. Forward Crosstalk



- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = $I_C = -C\,\Delta V_I/\Delta t$
- Mutually Induced Current = $I_M = mI_L$
- Forward Crosstalk Current = I_{CR}
- As the active signal, V_i, propagates from A to B a positive pulse appears at C for a duration twice the coupled line delay T.

FIGURE 15. Reverse Crosstalk

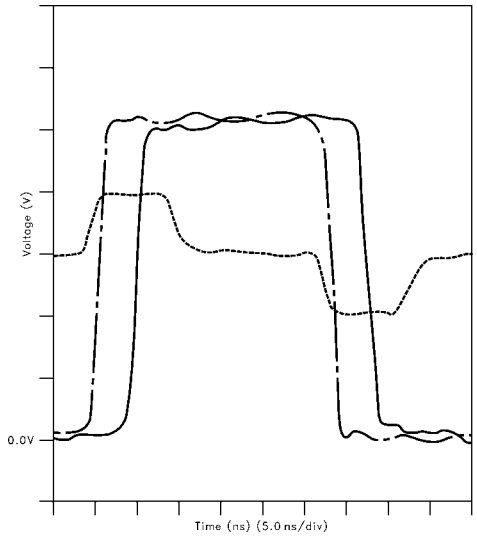
Crosstalk (continued)



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude or crosstalk pulses.

FIGURE 16. Forward Crosstalk on PCB Traces

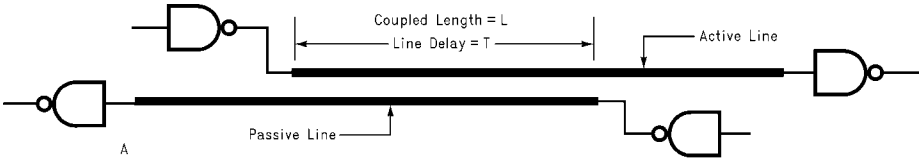


Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

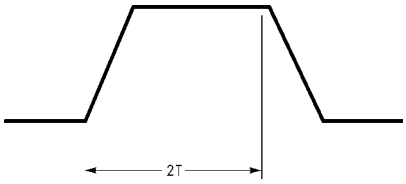
This figure shows traces taken on a test fixture designed to exaggerate the amplitude or crosstalk pulses.

FIGURE 17. Reverse Crosstalk on PCB Traces

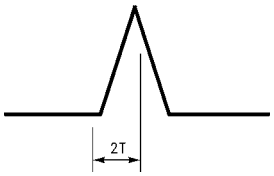
Crosstalk (continued)



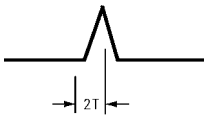
Noise Pulses at A:



For $T > t_r$ Noise Reaches Max Amplitude



For $T = 0.5\ t_r$ Noise Just Reaches Max at Peak



For $T < 0.5\ t_r$ Noise Never Reaches Full Amplitude

FIGURE 18. Partially Coupled Lines

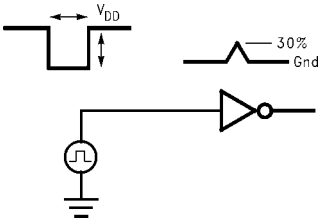


FIGURE 19. High Noise Margin

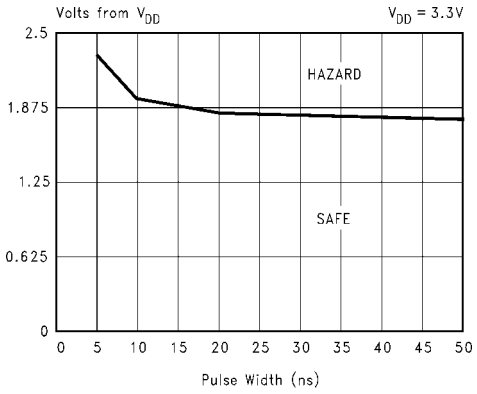


FIGURE 20. LCX High Noise Margin

Crosstalk (continued)

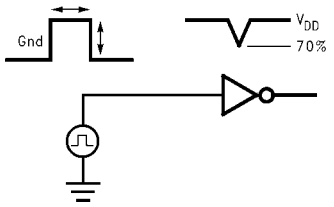


FIGURE 21. Low Noise Margin

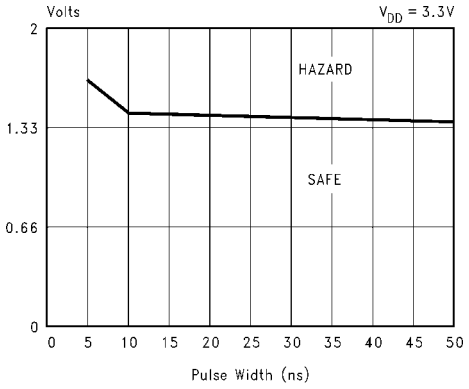


FIGURE 22.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

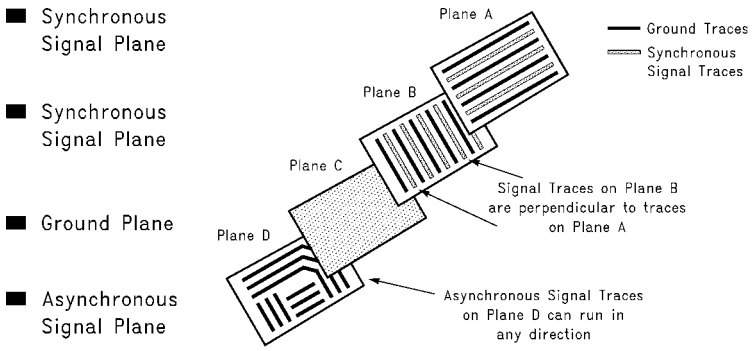
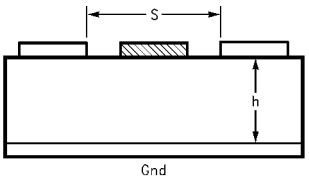


FIGURE 23. Recommended Crosstalk-Avoidance Structure



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace between signal traces
- Minimize distance h to keep line impedance low

FIGURE 24. PCB Layout Tips for Crosstalk Avoidance

Decoupling Requirements

Fairchild Semiconductor's *CROSSVOLT* families, as with other high-performance, high-drive logic families, have special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with these products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 26 displays various V_{DD} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 100Ω and 150Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{DD} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 25 to calculate the amount of decoupling necessary. This circuit utilizes an LCX244 driving a 150Ω bus from a point somewhere in the middle.

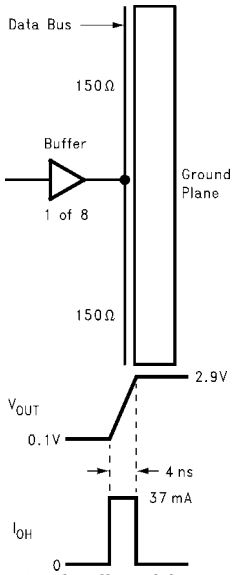


FIGURE 25. Octal Buffer Driving a 150Ω Bus

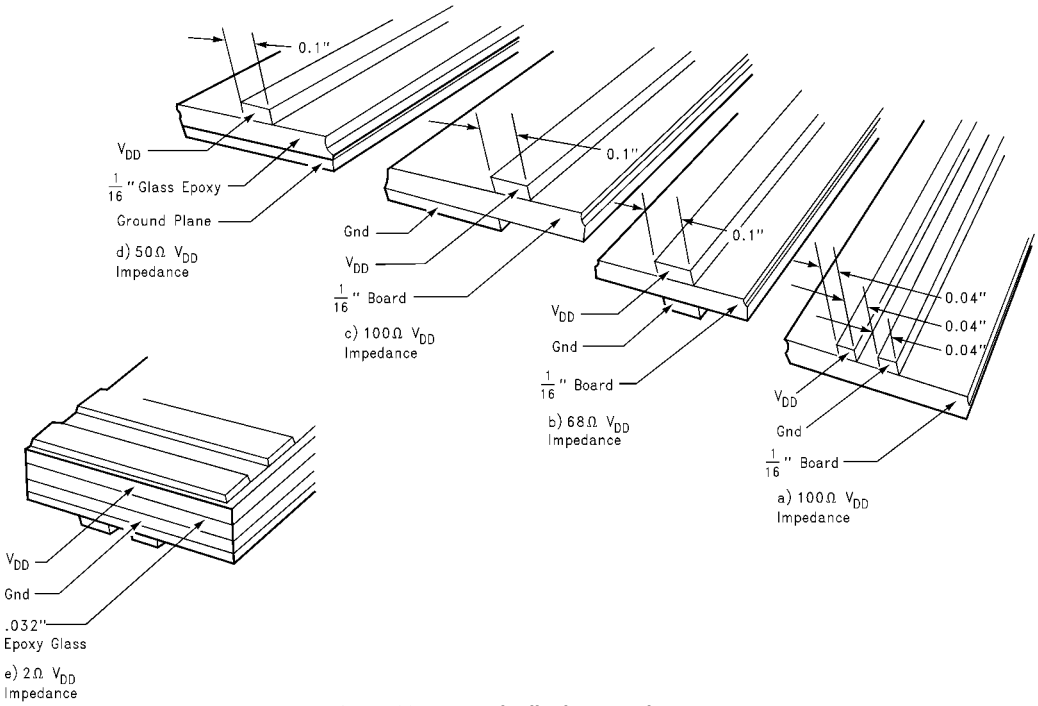


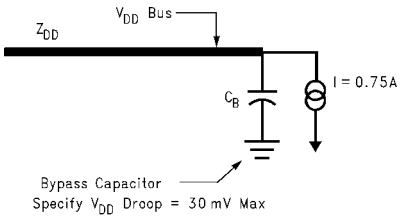
FIGURE 26. Power Distribution Impedances

Decoupling Requirements (continued)

Being in the middle of the bus, the driver will see two 150Ω loads in parallel, or an effective impedance of 75Ω. To switch the line from rail to rail, a drive of 37 mA is needed; more than 300 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{DD} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 27.

In this example, if the V_{DD} droop is to be kept below 20 mV and the edge rate equals 4 ns, a 0.10 µF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



$Q = CV$

$I = C\Delta V/\Delta t$

$C = I\Delta t/\Delta V$

$\Delta t = 4 \times 10^{-9}$

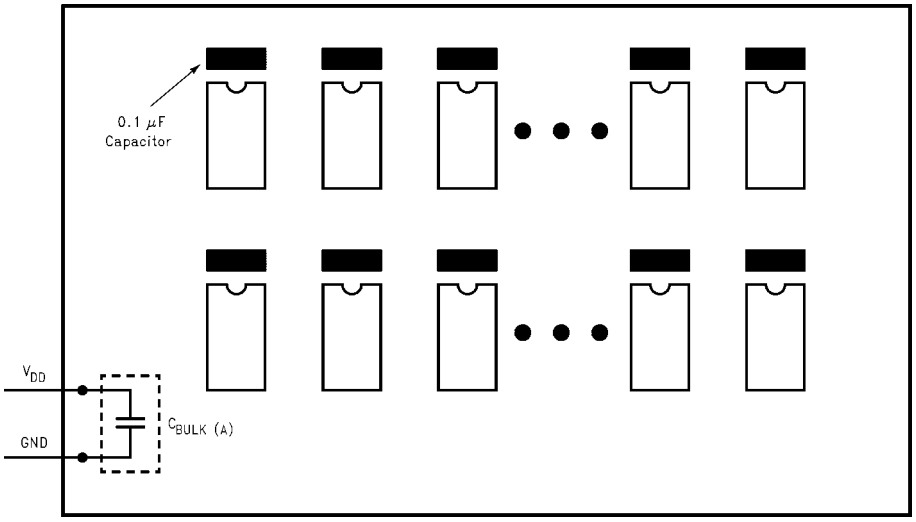
$$C = \frac{0.3 \times 4 \times 10^{-9}}{0.02} = 60 \times 10^{-9} = 0.06\ \mu F$$

Select $C_B \geq 0.10\ \mu F$

FIGURE 27. Formula for Calculating Decoupling Capacitors

CAPACITOR TYPES

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



- Need to decouple board at the point of power supply entry.
- This capacitor (A) will smooth low frequency bulk switching noise.
- A large value electrolytic capacitor is typically used (50 µF – 100 µF)

FIGURE 28. Board-Level Decoupling Capacitor

Electromagnetic Interference

One of the features of advanced CMOS is its fast output edge rates. Advanced CMOS outputs swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted.

EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibility.

SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

As Figure 29 illustrates, EMI in a typical electronic circuit is generated by a current flowing in some current path configured within the circuit. These paths can be either V_{DD}-to-GND loops or output transmission lines. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The current path material itself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. Figure 30 illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the frequency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

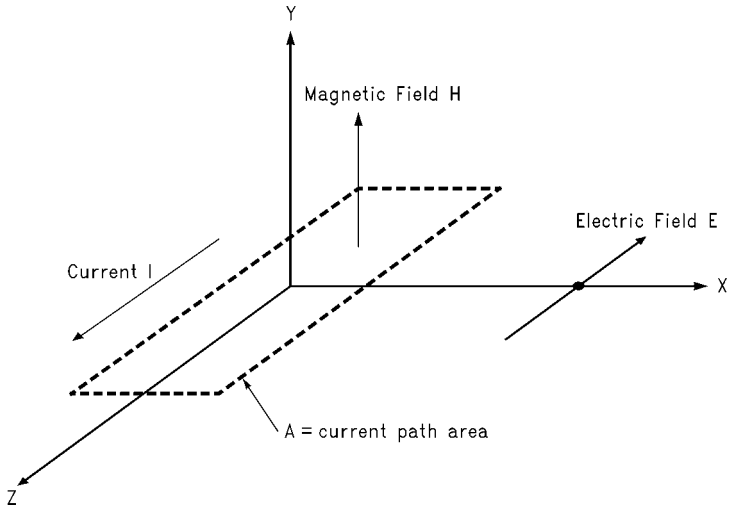
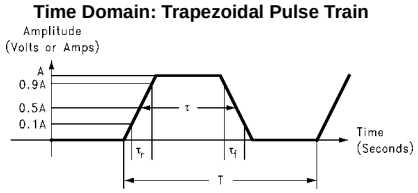


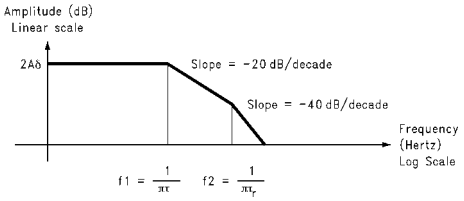
FIGURE 29. EMI is Generated by a Current Flowing along Some Path (Loop)

Time Domain: Trapezoidal Pulse Train



- τ = Pulse Width HIGH
- τ_r = Rise Time
- τ_f = Fall Time
- T = Period
- A = Amplitude

Frequency Domain: Worst-Case Upper Bound Approximation



- f_1 = 1st Breakpoint
- f_2 = 2nd Breakpoint
- δ = Duty Cycle = τ/T

FIGURE 30. Time Domain to Frequency Domain Conversion

OVERALL SYSTEM EMI

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—V_{DD}-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components.

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \bullet |I| \bullet A \bullet Freq^2}{D} \left[1 + \left(\frac{\lambda}{2} \pi D\right)^2\right]^{1/2} \frac{\mu V}{m}$$

where,

$|E|_{Max}$ is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the antenna area in square cm

λ s the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop $P \ll \lambda$.

Figure 31 illustrates lab measurements of radiated emissions from a test board populated with FACT and LCX logic. The device under test is driving a similar device across 26 cm of printed circuit board trace.

At higher frequencies where, for example, quarter wavelengths approach the lengths of transmission lines common in typical backplanes and plug-in cards, LCX radiates substantially less EMI than other ACMOS logic.

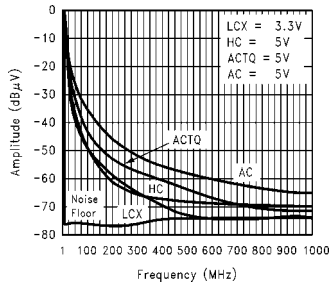


FIGURE 31. Low Voltage Logic as a Solution

POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undesirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

- On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.
- Decoupling the power supply at the point of entry onto the printed circuit board is also highly recommended. The use of a low equivalent series inductance, or ESL, multilayer ceramic capacitor, 50 μF to 100 μF, provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10 μF chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data transmission or unreliable system operation. Therefore, good EMC design techniques at the circuit board level are just as necessary.

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.
- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplings or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 8 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

BACKPLANE CONSIDERATIONS

The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used.

- Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC.
- Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors.

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.

Bushold

Increased levels of logic integration and portable system space constraints have led to the widespread use of "bus-hold" input latches to keep 3-state buses and other system interfaces from floating to invalid voltage levels. A conceptual drawing is shown in the Figure 32

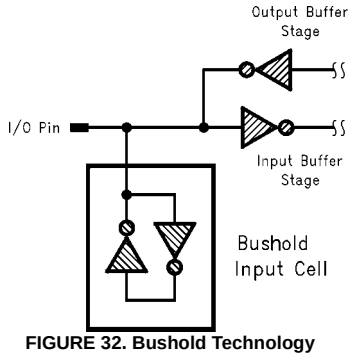


FIGURE 32. Bushold Technology

This type of 3-state bus termination works very well in synchronous systems. The bus-hold cell can act as a memory element in a synchronous pipeline easing the timing constraints placed on adjacent LSI devices.

First introduced on the LVT family of products, bus-hold has become a feature of several low voltage logic families. This feature does have it's drawbacks in mixed voltage systems and must be used with caution in battery powered systems. Here are some examples:

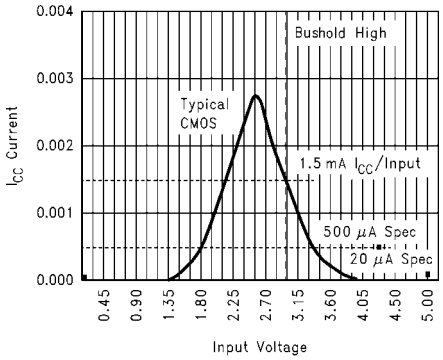


FIGURE 33.

Superimposed onto a typical CMOS V_{IN} vs I_{CC} plot for a 5V CMOS device is the "bus-hold" voltage attained by an LVT device. Although clearly high enough to present a logic high to the CMOS input, a significant amount of I_{CCT} current will be flowing though each input of the CMOS device.

Another potential source of trouble is modular low drive applications.

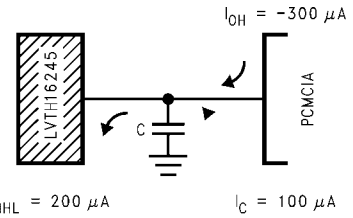


FIGURE 34. Bushold AC Performance Impact

Even the "small" input latch on LVT products requires a significant amount of current to override it's latched state. Given a PCMCIA specification of –300uA and a typical "bushold" current of 200uA, a sizable degradation in AC switching performance will result. A PCMCIA card, with it's drive capability reduced by 2/3's, will have a much harder time driving the PCMCIA connector and bus.

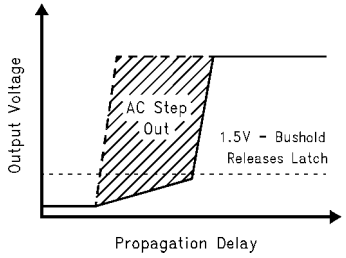


FIGURE 35. Bushold AC Performance Impact

Hot Insertion and Power Cycling

Fairchild Semiconductor's Low Voltage CMOS and BiCMOS Technology can be used to provide a high speed fault tolerant solution for interface needs. Some of the targeted interface environments include computer servers, mainframes and central office switches.

Each of these interface environments suffer from glitching or level degradation on their backplane or bus, generated from either live insertion of a board or a power up and down cycle used when performing maintenance on a system. Board designers need to address live insertion and power cycling requirements when designing a fault tolerant system. Definitions and applications of live insertion and power cycling change based on the product that interfaces with a backplane environment.

Discussion of fault tolerance benefits from a review of definitions and solutions for fault tolerant interfacing and a review of device specs and how they contribute to a fault tolerant environment.

Definition of Terms

Live Insertion

Boards like those seen in a telephone company's central office switch are often removed and inserted while the backplane remains active. Insertion and removal generates glitches and voltage level changes on the backplane. The level of isolation that a board mounted interface device provides the backplane can be broken down into three major groups.

- **1st Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board to which it is mounted without having to power the system down. Requirements include a method of suspending the bus activity to prevent glitch or level corruption of bus data.
- **2nd Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board without the need to power the system down or suspend bus activity. Requirements include a method by which the bus can check for, and correct, faults introduced on the backplane during board insertion or a method for providing proper biasing of the board interface devices with a staggered pin arrangement on the board-backplane connector. Precondition biasing circuitry for the interface device may also provide the required isolation.
- **3rd Level of Isolation** is defined as the ability of the interface devices to allow board insertion without any limitations, restrictions or requirements of other circuits on the preservation of bus data.

The level of isolation that an interface device mounted on a board provides for the backplane has a direct impact on system uptime. Increasing levels of isolation allow for increased serviceability without system interruption. Board isolation provided by an interface device gives more freedom to the designer for focusing on purpose built board functions, reducing board design complexity and ultimately, board cost. Fairchild LVCMOS or BiCMOS product rewards the board designer and the board user these benefits with a 2nd Level isolation solution.

Power Up/Down 3-STATE

When the devices that interface with the backplane power up or down, their connection to the bus will ideally maintain a high impedance state. With respect to the LVT, LCX and VCX™ product families, the output enable circuitry has control of the output state of the interface device during power up and down so as to prevent intermittent low impedance loading or glitch generation commonly associated with conventional CMOS and Bipolar devices.

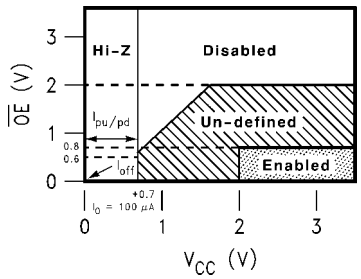


FIGURE 36. Power Up/Down Output State

Partial System Power Down

Partial system power down implies that a system comprised of a combination of hardware and firmware provides power switching control of a backplane slot to allow for insertion, or removal of a board. Partial system power down facilitates system serviceability. Board mounted LVT, LCX or VCX interface products enhance serviceability for permitting backplane slot power cycling while maintaining high impedance, glitch free isolation with the board and its backplane.

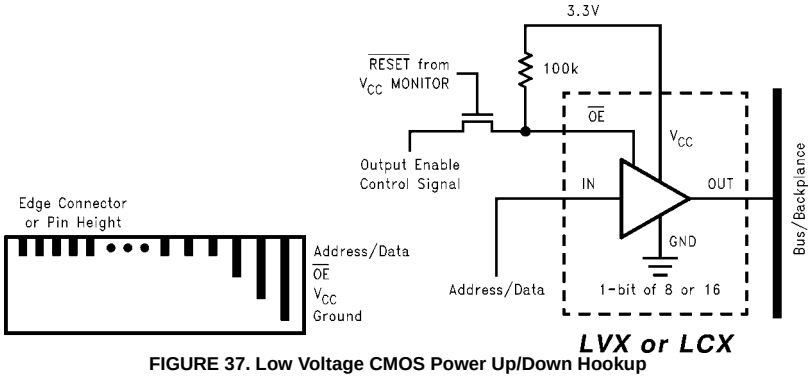


FIGURE 37. Low Voltage CMOS Power Up/Down Hookup

Hot Insertion and Power Cycling (continued)

The achievement of a fault tolerant system solution with live insertion capabilities begins with a review of some of the bus protection solutions available. Options available to the LVT, LCX, and VCX product families include:

- Staggered Pin Arrangement

  For a PC edge connector arrangement, the solution above can be adopted to provide proper biasing of the output enable pin ($\overline{OE}$) to ensure high impedance on the backplane. It will satisfy both insert and removal requirements. While this configuration provides an ideal connector, constraints often limit the number of different pin lengths to two. By offsetting the $\overline{OE}$ pin, we want to ensure that it will either reach a high level of ≥ 2.0V, before V_{CC} is applied, or the $\overline{OE}$ will maintain a ≥ 50% V_{CC} level during the V_{CC} ramp.

- Isolation Circuitry

  Isolation circuitry provides another option for board and backplane isolation. Again, this solution will provide the necessary $\overline{OE}$ pin biasing to assure a level of 2.0V or to assure $\overline{OE}$ maintains >50% of V_{CC} as V_{CC} powers up or down for guaranteed high impedance interface to the backplane.

The design of the circuit Figure 37 pulls the $\overline{OE}$ pin to V_{CC} throughout the V_{CC} ramp then switches to a voltage level determined by the control logic once the board level $\overline{RESET}$ signal is released to logic high. Obviously, additional maintenance and PWRGOOD signals can be multiplexed into the control of the isolation N-Channel pass gate.

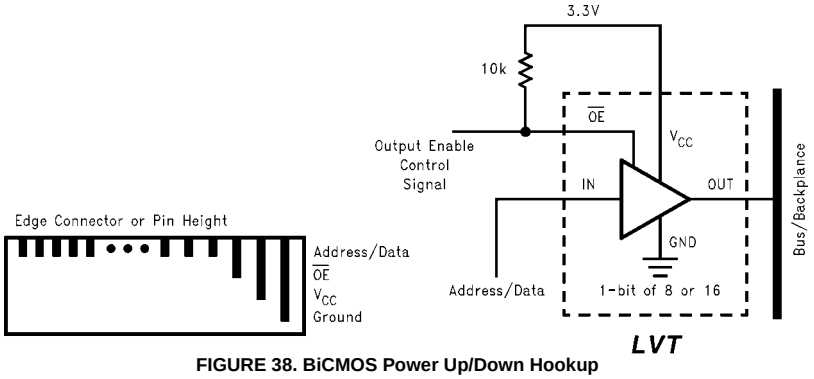


FIGURE 38. BiCMOS Power Up/Down Hookup

Power Dissipation

One advantage to using CMOS logic is it's extremely low power consumption. During quiescent conditions, CMOS logic will consume several orders of magnitude less current than its Bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or Bipolar technologies. Total power dissipation of CMOS devices under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, a CMOS device will dissipate power in the quiescent or static condition. This can be calculated using the formula:

Note: In many datasheets I_{DD}, ΔI_{DD}, I_{DDT}, and V_{DD} are referred to as I_{CC}, ΔI_{CC}, I_{CCT}, and V_{CC}, respectively. There are no differences.

Equation 1

$PD_q = I_{DD} * V_{DD}$

PD_q = Quiescent Power Dissipation

I_{DD} = Quiescent Power Supply Current Drain

V_{DD} = Power Supply Voltage

Secondly, a CMOS device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using one of the following two formulas:

Equation 2A (CMOS input swings)

$PDINT = (C_{PD} * V_S * f) * V_{DD}$

PDINT = Internal Dynamic Power Dissipation

C_{PD} = Device Power Dissipation Capacitance

V_S = Output Voltage Swing

f = Internal Frequency of Operation

V_{DD} = Power Supply Voltage

C_{PD} values are specified for each CMOS device and are measured per JEDEC standards. On CMOS device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. (See Section 2.) For CMOS devices, V_S and V_{DD} are the same value and can be replaced by V_{DD2} in the above formula.

Equation 2B (TTL input swings)

$PD_{INT} = [I_{DDT} * D_H * N_T * V_{DD}] + [(C_{PD} * V_S * 1) * V_{DD}]$

PD_{INT} Internal Dynamic Power Dissipation

I_{DDT} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs HIGH

N_T = Number of TTL Inputs at D_H

V_{DD} = Power Supply Voltage

C_{PD} = Device Power Dissipation Capacitance

V_S = Output Voltage Swing

f = Internal Frequency of Operation

Thirdly, a CMOS device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Equation 3

$PD_{OUT} = (C_L * V_S * f) * V_{DD}$

PD_{OUT} = Output Power Dissipation

C_L = Load Capacitance

V_S = Output Voltage Swing

f = Output Operating Frequency

V_{DD} = Power Supply Voltage

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{DD} and can be replaced by $V_{DD} * V_{DD}$. In the case of internal and output frequencies being identical Equation 2A and Equation 3 may be combined as follows:

Equation 4

$P_D = (C_L + C_{PD}) * V_{DD} * V_{DD} * f$

The total CMOS device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Equation 5

$PD_{TOTAL} = PD_q + PD_{DYNAMIC}$ or

$PD_{TOTAL} = PD_q + PD_{INT} + PD_{OUT}$

The following is an exercise in calculating total dynamic I_{DD} for the LVX Advanced CMOS family of translators. The device used as an example is the LVX3245. Static I_{DD}, and IDDT and C_{PD} numbers can be found in the LVX3245 data sheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst case calculations.

The following assumptions have been made:

1. I_{DD} will be calculated per input/output (as per JEDEC C_{PD} calculations). The total for the LVX3245 will be calculated I_{DD} x 8.
2. Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate (1/2 CP).
3. All data and control input signals are derived from CMOS level drivers (0V to 3.3V or 5.0V swing) at 50% duty cycle.
4. The data rate is 8 MHz, the device transfers data 50% from A > B and 50% B > A.
5. I_{DD} will be calculated for C_L = 50 pF on the A and B ports.
6. V_{DDA} = 3.3V V_{DDB} = 5.0V.
7. Total POWER dissipation can be obtained by multiplying the total I_{DDA} by V_{DDA} (3.3V) + the total I_{DDB} by V_{DDB} (5.0V).
8. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
9. There is no DC load on the outputs, i.e., outputs are either unterminated or terminated with series damping or diode termination.

Power Dissipation (continued)

The I_{DD} calculations are as follows:

A > B

I_{DDB} Total = Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Internal $I_{DDB} = (V_{DDB}) \times (C_{PD}) \times$ (Data frequency)
(5.0) x (55 x 10–12) x (8 x 10+6)
2.2 mA per input toggled at 8 MHz

Output $I_{DDB} = (V_{SWING}) \times (C_L) \times$ (Data frequency)
(5.0) x (50 x 10–12) x (8 x 10+6)
2 mA per output toggled at 8 MHz

B > A

I_{DDA} Total = Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Internal $I_{DDA} = (V_{DDA}) \times (C_{PD}) \times$ (Data frequency)
(3.3) x (40 x 10–12) x (8 x 10+6)
1.06 mA per input toggled at 8 MHz

Output $I_{DDA} = (V_{SWING}) \times (C_L) \times$ (Data frequency)
(3.3) x (50 x 10–12) x (8 x 10+6)
1.32 mA per output toggled at 8 MHz

Adding Internal and Output I_{DD} together and multiplying each by 50% duty cycle and *I/O per LVX3245, the approximate worst-case I_{DD} calculations are as follows:

C_L = 50 pF

I_{DDB} total = 4.4 mA * 0.5 * 8 I/O
17.6 mA

C_L = 50 pF

I_{DDA} total = 2.38 mA * 0.5 * 8 I/O
9.52 mA

(*Power is obtained by multiplying I_{DD} by V_{DD})

PD_{TOTAL} = $I_{DDA} * V_{DDA} + I_{DDA} * V_{DDA}$
9.52 * 3.3 + 17.6 * 5.0
119.5 mW

The following is an exercise in calculating total dynamic I_{DD} for the LVX Advanced CMOS family. The device used as an example is the LVX163. Static I_{DD}, IDDT and C_{PD} numbers can be found in the LVX163 data sheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst case calculations.

The following assumptions have been made:

1. I_{DD} will be calculated for entire device (as per JEDEC C_{PD} calculations). The total for the LVX163 will be the calculated I_{DD}.
2. All data and control input signals are derived from CMOS level drivers (0V to 3.3V or 5.0V swing) at 50% duty cycle.
3. The clock rate is 10 MHz.
4. I_{DD} will be calculated for C_L = 50 pF on Q_0–Q_3 and C_L = 10 pF on C_{TC}.
5. V_{DD} = 3.3V.
6. Total POWER dissipation can be obtained by multiplying the total I_{DD} by V_{DD} (3.3V).
7. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
8. There is no DC load on the outputs, i.e., outputs are either unterminated or terminated with series damping or diode termination.

The I_{DD} calculations are as follows:

I_{DD} Total = Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Internal $I_{DD} = (V_{DD}) \times (C_{PD}) \times$ (Clock frequency)
(3.3) x (23 x 10–12) x (10 x 10+6)
0.76 mA

Output $I_{DD} = (V_{SWING}) \times$ (Clock frequency) x $[(C_{LQ0}/2) + C_{LQ1}/4) + (C_{LQ2}/8) + (C_{LQ3}/16) + (C_{LTC}/16)]$
(3.3) x (10 x 10+6) x (25 x 10–12 + 12.5 x 10–12 +6.25 x 10–12 + 3.125 x 10–12 + 0.625 x 10–12)
1.57 mA

Adding Internal and Output I_{DD} together, the approximate worst-case I_{DD} calculations are as follows:

I_{DD} total = 0.76 mA + 1.57 mA
2.33 mA

P_D total = 2.33 mA * 3.3V
7.69 mW

(*Power is obtained by multiplying I_{DD} by V_{DD})

The following is an exercise in calculating total dynamic I_{DD} for the LCX Advanced CMOS family. The device used as an example is the LCX74. Static I_{DD}, IDDT and C_{PD} numbers can be found in the LCX74 data sheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst case calculations.

The following assumptions have been made:

1. I_{DD} will be calculated for 1/2 of the device (as per JEDEC C_{PD} calculations).
2. All data and control input signals are derived from CMOS level drivers (0V to 3.3V swing) at 50% duty cycle.
3. The clock rate is 48 MHz.
4. I_{DD} will be calculated for C_L = 10 pF on $/Q_0$ (3 pF wire Cap + 7 pF D_0 input Cap) and C_L = 50 pF on Q_0 (Generic test load Cap).
5. V_{DD} = 3.3V.
6. Total POWER dissipation can be obtained by multiplying the total I_{DD} by V_{DD} (3.3V).
7. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
8. There is no DC load on the outputs, i.e., outputs are either unterminated or terminated with series damping or diode termination.

Power Dissipation (continued)

The I_{DD} calculations are as follows:

I_{DD} Total = Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Internal I_{DD} = (V_{DD}) x (C_{PD}) x (Clock frequency)

(3.3) x (25 x 10–12) x (48 x 10+6)

3.96 mA

Output I_{DD} = (V_{SWING}) x (Clock frequency) x [(C_{LQ02}/2) + C_{LQ0}/2)]

(3.3) x (48 x 10+6) x (5 x 10–12 + 25 x 10–12)

4.75 mA

Adding Internal and Output I_{DD} together, the approximate worst-case I_{DD} calculations are as follows:

I_{DD} total = 3.96 mA + 4.75 mA

8.71 mA

P_D total = 8.71 mA * 3.3V

28.74 mW

(*Power is obtained by multiplying I_{DD} by V_{DD})