DLD601/D
Rev. 0, Jan-2000

One-Gate Logic

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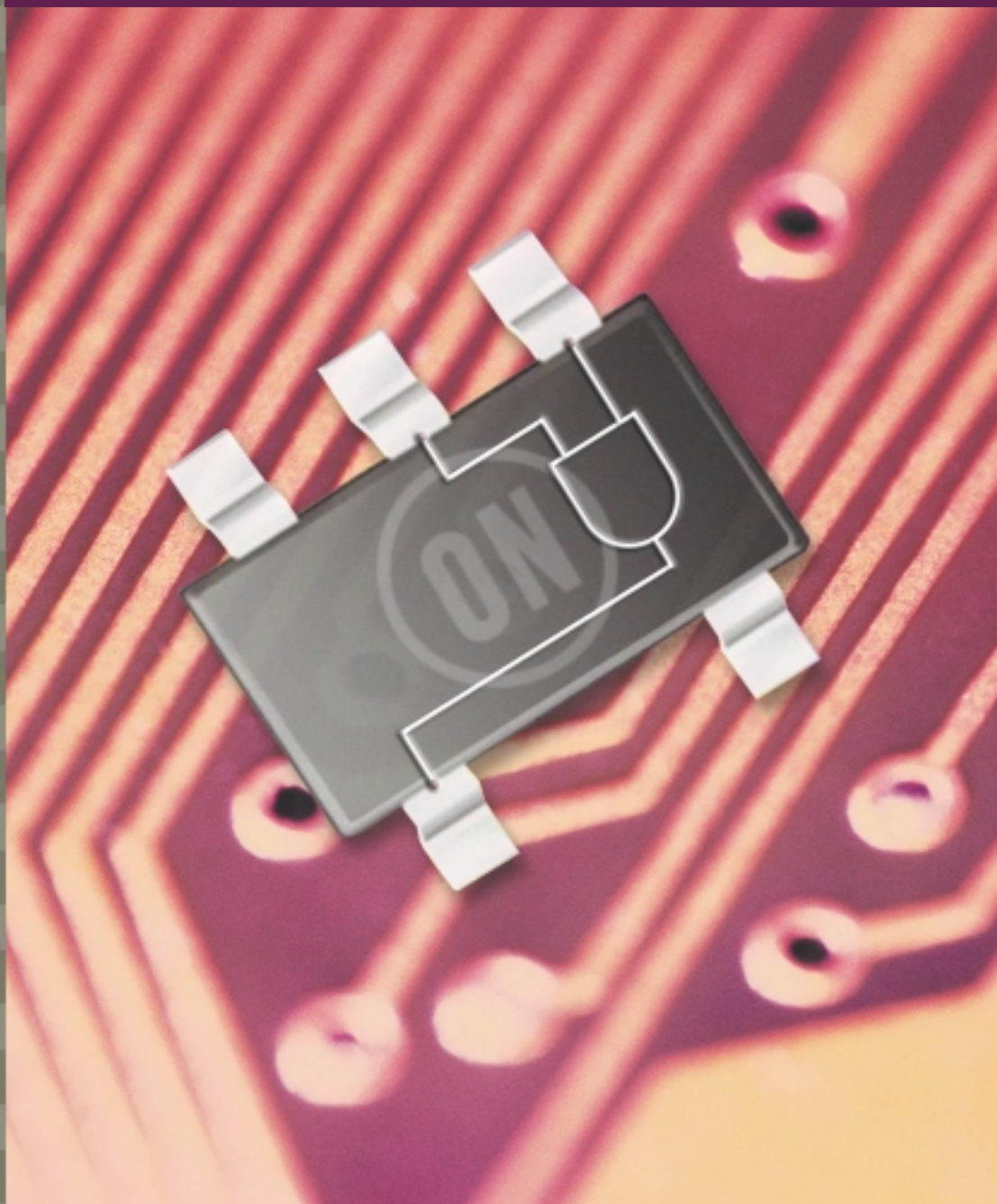

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An Introduction to One Gate Logic

Initially, One–Gate devices were popularized in Japan for use in hand held applications. They were originally designed to “fix” small, simple problems, either with the logic, for adding buffering between circuits, or to add signal drive. System designers outside of Japan never fully appreciated the value of these tiny devices, and the role they could play in reducing board area by applying logic signals, just where it was needed.

Although several package variations exist, today, the most current One Gate devices are packaged in the industry standard SC–88A/SOT353 package. This package measures approximately 2.0 X 2.1 mm, or less than 4.5 mm^2. By comparison, a standard 14 lead SOIC is over 50 mm^2. 4 one–gate devices take up about 1/3 the area of a conventional SOIC package. Even more importantly, because of the small package size, one–gate functions allow the designer significant flexibility in signal line routing.

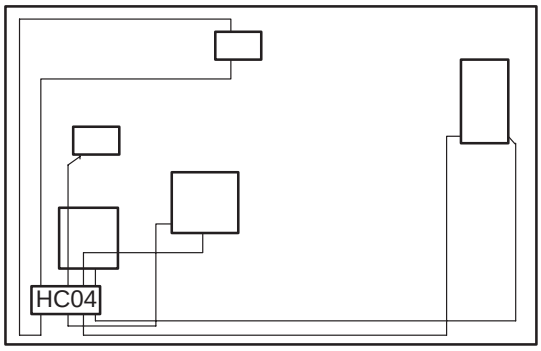
In general, the simpler the board layout, the more likely the circuit will function properly the first time. If a designer is using an ordinary four–gate, TSSOP, logic IC and needs all four gates he must first find the board space to place a 14–pin package (32 mm^2). He will then begin the task of routing to and from the device. In the event that the inputs are coming from different places around the board, the routing becomes difficult. In addition, the longer the signal lines, the higher the chances for EMI type of problems. In cases where logic functions are required in 2 or 3 different locations, the routing issue becomes even more complex. In a second case, a standard logic device has 4 gates, but the designer needs 2 or more different logic forms, i.e. AND, NAND, XOR etc. Of course the designer could use several gates to create the correct logic, but that would defeat the purpose of a multi–gate logic device. With One Gates, the designer can have a 2–Input NAND gate in one corner and a 2 –Input XOR in another corner. The inputs can be close to the source, so routing is simplified.

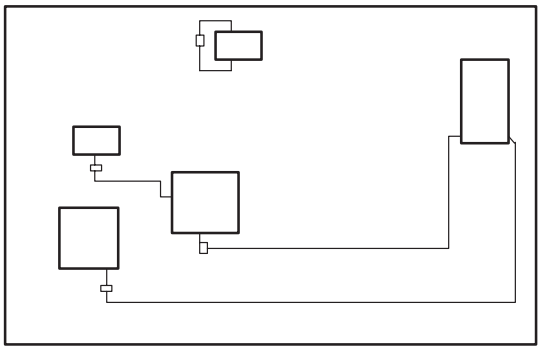
One–Gate logic products can be derived from almost any standard multi–gate family of products. ON Semiconductor, has selected the 74VHC CMOS logic family as the preferred technology for One Gate. VHC has extremely desirable characteristics to make it ideal for One Gates. It is usable over a wide range of voltages, with fully guaranteed operation from 2.0 to 6.0 volts. Like other CMOS logic families, VHC slows down somewhat at the lower voltages, but non the less, still remains one of the faster logic families. VHC is over–voltage tolerant (OVT), at its inputs, which permits the designer to operate the device at a low voltage, say 2.5 volts, but yet interface with 5.0 volt logic. Typical propagation delays of less than 5.0 nsecs, along with extremely low quiescent power, make the VHC technology very attractive for many applications.

Open drain: In addition to the offering of traditional, standard logic functions, On Semiconductor will be offering a broad portfolio of open drain devices, allowing logic level translation to or from almost any logic level. The designer only needs to operate the One Gate from the input Vcc voltage to be translated, and connect the output to a pull–up resistor to the output voltage. The output will be translated to the new voltage. This voltage may be any level between 1.5 and 7.0 volts. Complex logic may also be created using a few open drain one gates. Two or more devices may be wire OR’d by simply connecting their O.D. outputs together, creating more complex logic, without taking up much space. Complex logic can be created very simply and at very low power consumption. This can be especially useful when trying to use a standard circuit in a special application. Since the one gate devices may each be different, the possibilities are nearly limitless.

Conclusion: One–gate logic devices offer the designer several new options that allow for cleaner simpler board layout, interfacing different voltage levels, and unique combinational logic forms taking up almost no board space and drawing very small amounts of power. ON Semiconductor has a wide offering of unique One–gate logic devices, with more than 20 unique devices being offered in the early part of the year 2000. All the devices are available in the industry standard SC–88A/SOT353 package. Most device types are available as both Standard CMOS level or TTL compatible input, many with Open Drain options, and all offering over–voltage tolerance (OVT) at the input.

Simplified Routing





Data Sheets

MC74VHC1G00

2-Input NAND Gate

The MC74VHC1G00 is an advanced high speed CMOS 2–input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G00 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G00 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 3.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

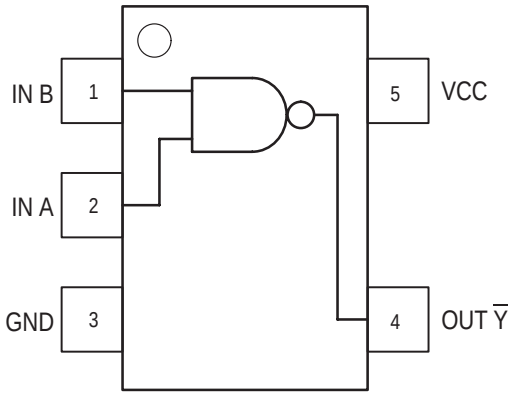
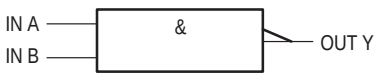


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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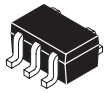
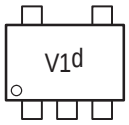


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	$\overline{\mathbf{Y}}$
L	L	H
L	H	H
H	L	H
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.5 5.6	7.9 11.4		9.5 13.0		11.0 15.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.0 3.8	5.5 7.5		6.5 8.5		8.0 10.0	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	10	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

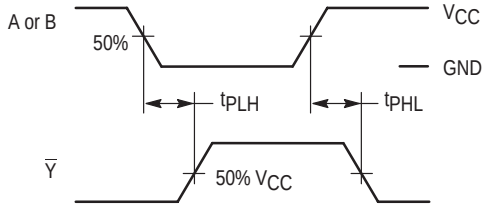
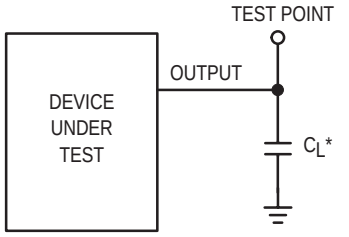


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G00DFT1	MC	74	VHC1G	00	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G01

Product Preview

2-Input NAND Gate with Open Drain Output

The MC74VHC1G01 is an advanced high speed CMOS 2–input NAND gate with an open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the ability to set output switching level. This allows the MC74VHC1G01 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G01 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

- High Speed: t_{PD} = 3.7ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

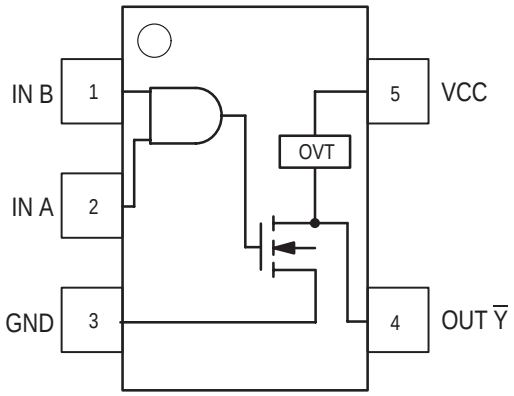
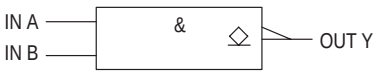


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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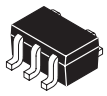
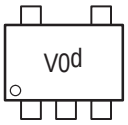


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	$\overline{\mathbf{Y}}$
L	L	Z
L	H	Z
H	L	Z
H	H	L

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MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	7.0	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	V_{OUT} = 5.5V	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PZL}	Maximum Output Enable Time, Input A or B to Y	V_{CC} = 3.0 ± 0.3V, R_L = 1KΩ, C_L = 15 pF		5.5	7.9		9.5		11.0	ns
		V_{CC} = 3.0 ± 0.3V, R_L = 1KΩ, C_L = 50 pF		8.0	11.4		13.0		15.5	
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 15 pF		3.7	5.5		6.5		8.0	
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 50 pF		5.2	7.5		8.5		10.0	
t_{PLZ}	Maximum Output Disable Time	V_{CC} = 3.0 ± 0.3V, R_L = 1KΩ, C_L = 50 pF		8.0	11.4		13.0		15.5	ns
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 50 pF		5.2	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

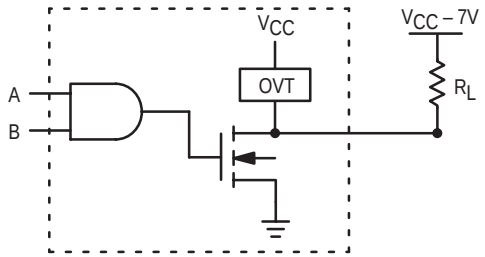


Figure 2. Output Voltage Mismatch Application

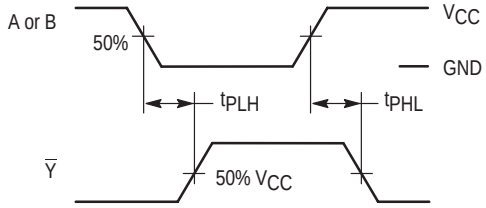
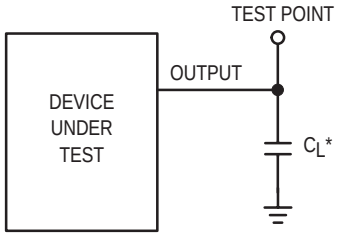


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G01DFT1	MC	74	VHC1G	01	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G02

2-Input NOR Gate

The MC74VHC1G02 is an advanced high speed CMOS 2–input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G02 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G02 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 3.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

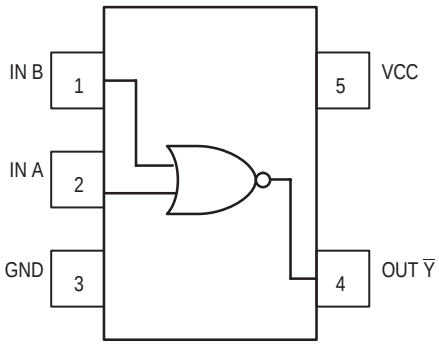
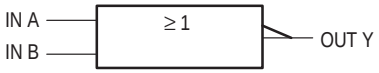


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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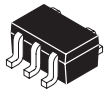
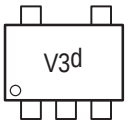


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	$\overline{\mathbf{Y}}$
L	L	H
L	H	L
H	L	L
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.0 5.4	7.9 11.4		9.5 13.0		11.0 15.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.0 3.8	5.5 7.5		6.5 8.5		8.0 10.0	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

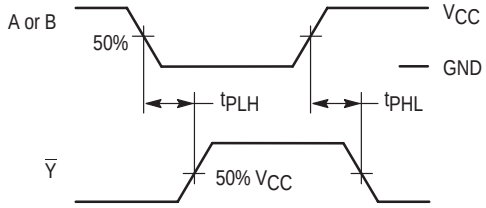
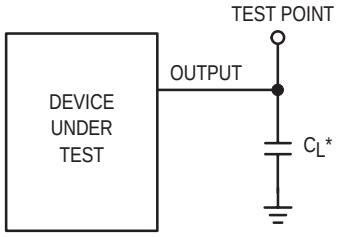


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G02DFT1	MC	74	VHC1G	02	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G03

Product Preview

2-Input NOR Gate with Open Drain Output

The MC74VHC1G03 is an advanced high speed CMOS 2–input NOR gate with an open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the capability to set output switching level. This allows the MC74VHC1G03 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G03 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

- High Speed: t_{PD} = 3.6ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

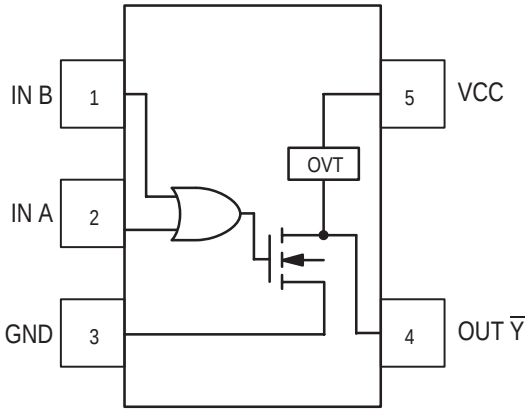
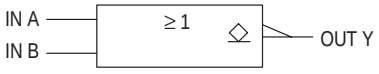


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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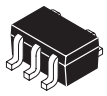
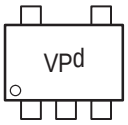


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**$\overline{Y}$**
L	L	Z
L	H	L
H	L	L
H	H	L

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MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	7.0	V
Operating Temperature Range	T_A	–55	+85	°C
Input Rise and Fall Time V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	$V_{OUT} = 5.5V$	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PZL}	Maximum Output Enable Time, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$, C_L = 15 pF $R_L = 1K\Omega$, C_L = 50 pF		5.6 8.1	7.9 11.4		9.5 13.0		11.0 15.5	ns
		$V_{CC} = 5.0 \pm 0.5V$, C_L = 15 pF $R_L = 1K\Omega$, C_L = 50 pF		3.6 5.1	5.5 7.5		6.5 8.5		8.0 10.0	
t_{PLZ}	Maximum Output Disable Time	$V_{CC} = 3.0 \pm 0.3V$, $R_L = 1K\Omega$, C_L = 50 pF		8.1	11.4		13.0		15.5	ns
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1K\Omega$, C_L = 50 pF		5.1	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

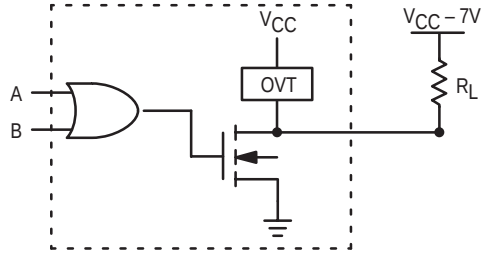


Figure 2. Output Voltage Mismatch Application

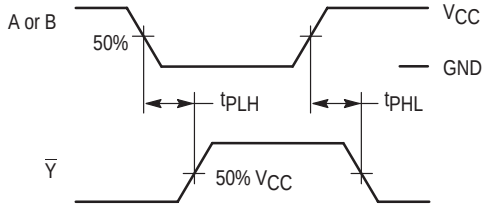
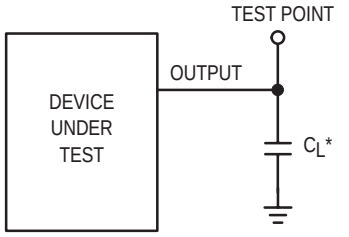


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G03DFT1	MC	74	VHC1G	03	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G04

Inverter

The MC74VHC1G04 is an advanced high speed CMOS inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G04 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G04 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 3.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 1500V; MM > 200V

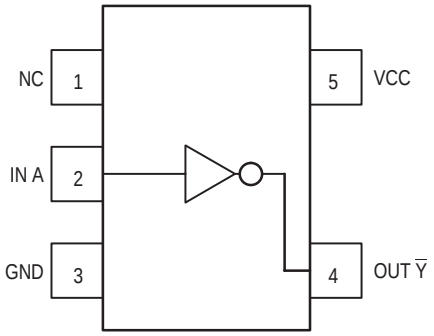
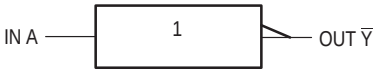


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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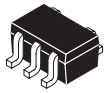
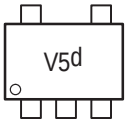


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

FUNCTION TABLE

A Input	Y Output
L	H
H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A to $\overline{Y}$	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.5 6.4	7.1 10.6		8.5 12.0		10.0 14.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.5 4.5	5.5 7.5		6.5 8.5		8.0 10.0	
C_{IN}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	8.0	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

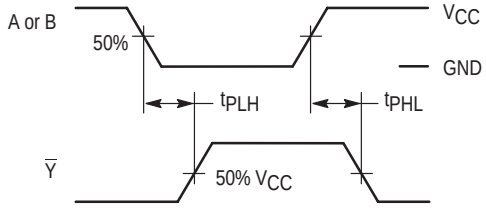
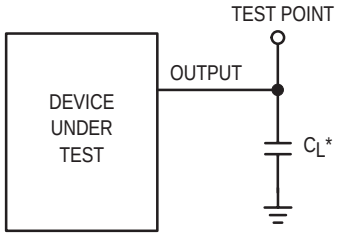


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G04DFT1	MC	74	VHC1G	04	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G05

Product Preview

Inverter with Open Drain Output

The MC74VHC1G05 is an advanced high speed CMOS inverter with open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the capability to set output switching level. This allows the MC74VHC1G05 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G05 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2µA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

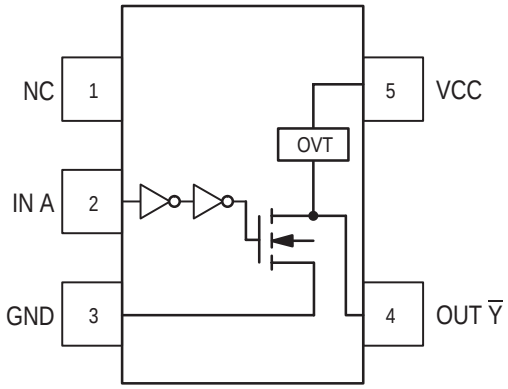
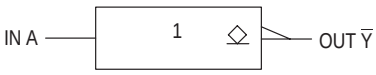


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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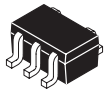
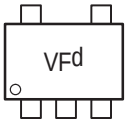


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

FUNCTION TABLE

A Input	$\overline{Y}$ Output
L	Z
H	L

MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	7.0	V
Operating Temperature Range	T_A	–55	+85	°C
Input Rise and Fall Time V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	$V_{OUT} = 5.5V$	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PZL}	Maximum Output Enable Time, Input A to $\overline{Y}$	$V_{CC} = 3.0 \pm 0.3V$ C_L = 15 pF $V_{CC} = 3.0 \pm 0.3V$ C_L = 50 pF		5.0 7.5	7.1 10.6		8.5 12.0		10.0 14.5	ns
		$V_{CC} = 5.0 \pm 0.5V$ C_L = 15 pF $V_{CC} = 5.0 \pm 0.5V$ C_L = 50 pF		3.8 5.3	5.5 7.5		6.5 8.5		8.0 10.0	
t_{PLZ}	Maximum Output Disable Time	$V_{CC} = 3.0 \pm 0.3V$, $R_L = 1K\Omega$, C_L = 50 pF		7.5	10.6		12.0		14.5	ns
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1K\Omega$, C_L = 50 pF		5.3	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

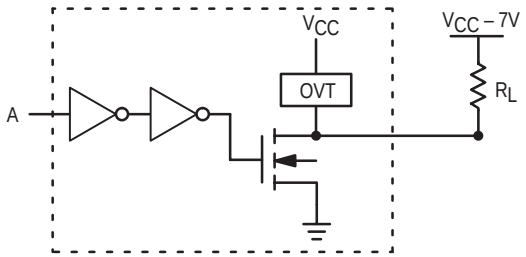


Figure 2. Output Voltage Mismatch Application

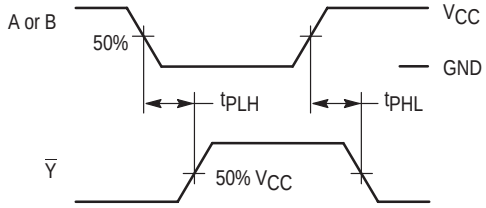
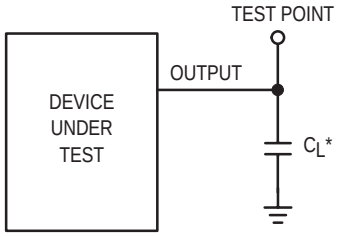


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G05DFT1	MC	74	VHC1G	05	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G07

Product Preview

Noninverting Buffer with Open Drain Output

The MC74VHC1G07 is an advanced high speed CMOS buffer with open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer and an open drain output which provides the capability to set the output switching level. This allows the MC74VHC1G07 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G07 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

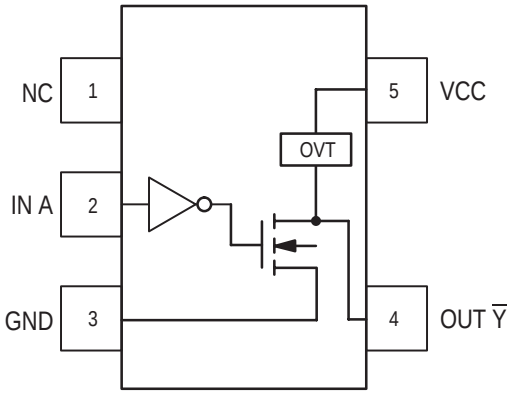
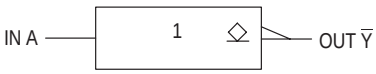


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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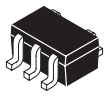
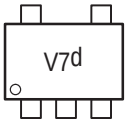


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 33 of this data sheet.

FUNCTION TABLE

A Input	$\overline{Y}$ Output
L	Z
H	L

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MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	7.0	V
Operating Temperature Range	T_A	–55	+85	°C
Input Rise and Fall Time V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	$V_{OUT} = 5.5V$	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PZL}	Maximum Output Enable Time, Input A to $\overline{Y}$	$V_{CC} = 3.0 \pm 0.3V$ C_L = 15 pF $R_L = 1K\Omega$ C_L = 50 pF		5.0 7.5	7.1 10.6		8.5 12.0		10.0 14.5	ns
		$V_{CC} = 5.0 \pm 0.5V$ C_L = 15 pF $R_L = 1K\Omega$ C_L = 50 pF		3.8 5.3	5.5 7.5		6.5 8.5		8.0 10.0	
t_{PLZ}	Maximum Output Disable Time	$V_{CC} = 3.0 \pm 0.3V$, $R_L = 1K\Omega$, C_L = 50 pF		7.5	10.6		12.0		14.5	ns
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1K\Omega$, C_L = 50 pF		5.3	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

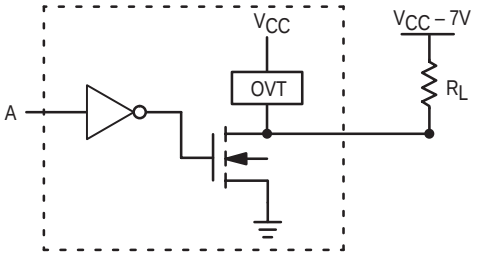


Figure 2. Output Voltage Mismatch Application

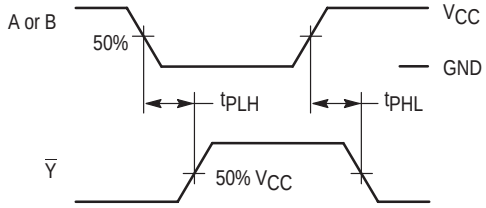
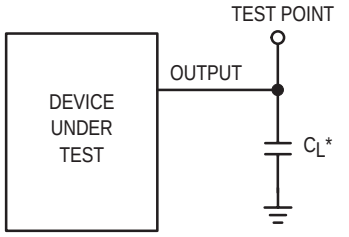


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G07DFT1	MC	74	VHC1G	07	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G08

2-Input AND Gate

The MC74VHC1G08 is an advanced high speed CMOS 2–input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G08 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G08 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 3.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

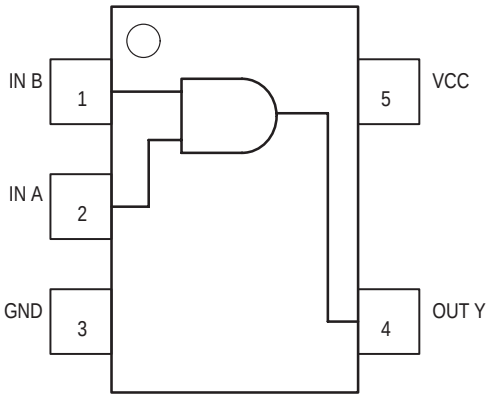
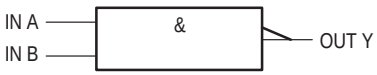


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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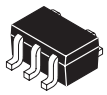
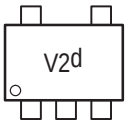


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 37 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	I
L	H	L
H	L	L
H	H	H

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.1 5.9	8.8 12.3		10.5 14.0		12.5 16.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.5 4.2	5.9 7.9		7.0 9.0		9.0 11.0	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

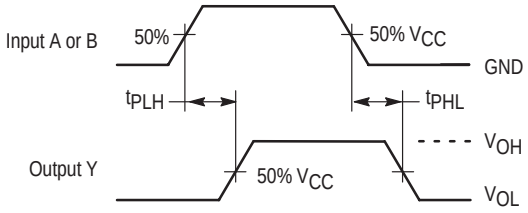
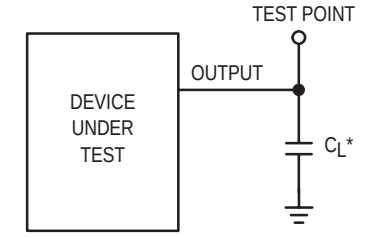


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

	Device Nomenclature							
Device Order Number	**Circuit Indicator**	**Temp Range Identifier**	**Technology**	**Device Function**	**Package Suffix**	**Tape & Reel Suffix**	**Package Type**	**Tape and Reel Size**
MC74VHC1G08DFT1	MC	74	VHC1G	08	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G09

Product Preview

2-Input AND Gate with Open Drain Output

The MC74VHC1G09 is an advanced high speed CMOS 2–input AND gate with open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the capability to set output switching level. This allows the MC74VHC1G09 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G09 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

- High Speed: t_{PD} = 4.3ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

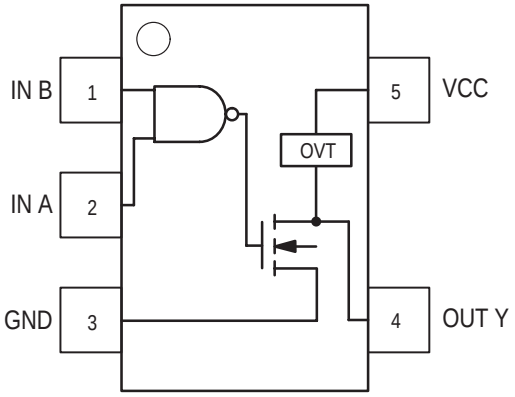
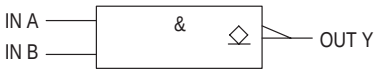


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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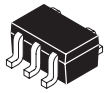
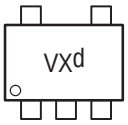


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 41 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	Z

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MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	±50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	7.0	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	$V_{OUT} = 5.5V$	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PZL}	Maximum Output Enable Time, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$, $R_L = 1K\Omega$, $C_L = 15$ pF		6.2	8.8		10.5		12.5	ns
		$V_{CC} = 3.0 \pm 0.3V$, $R_L = 1K\Omega$, $C_L = 50$ pF		8.7	12.3		14.0		16.5	
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1K\Omega$, $C_L = 15$ pF		4.3	5.9		7.0		9.0	
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1K\Omega$, $C_L = 50$ pF		5.8	7.9		9.0		11.0	
t_{PLZ}	Maximum Output Disable Time	$V_{CC} = 3.0 \pm 0.3V$, $R_L = 1K\Omega$, $C_L = 50$ pF		8.7	12.3		14.0		16.5	ns
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1K\Omega$, $C_L = 50$ pF		5.8	7.9		9.0		11.0	
C_{IN}	Maximum Input Capacitance			6.0	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

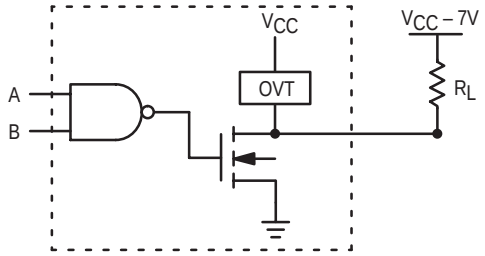


Figure 2. Output Voltage Mismatch Application

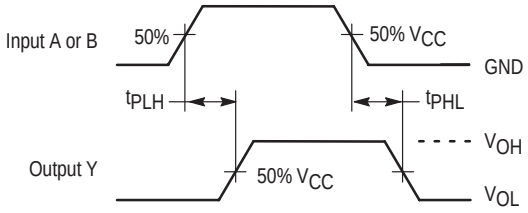
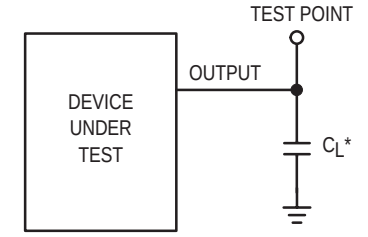


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G09DFT1	MC	74	VHC1G	09	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G132

2-Input NAND Schmitt-Trigger

The MC74VHC1G132 is a single gate CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G132 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G132 to be used to interface 5V circuits to 3V circuits.

The MC74VHC1G132 can be used to enhance noise immunity or to square up slowly changing waveforms.

- High Speed: t_{PD} = 3.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V

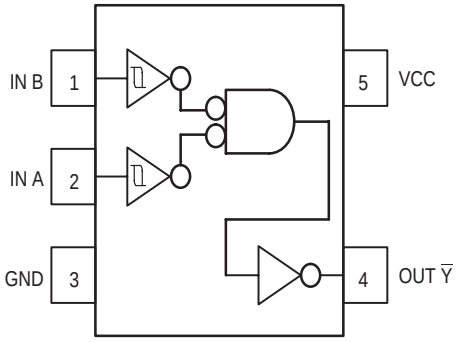


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL

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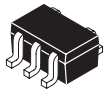
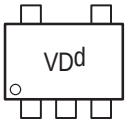


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 45 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	$\overline{\mathbf{Y}}$
L	L	H
L	H	H
H	L	H
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range	T_A	–55	+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5			2.20 3.15 3.85		2.20 3.15 3.85		2.20 3.15 3.85	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.9 1.35 1.65			0.9 1.35 1.65		0.9 1.35 1.65		V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50		1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage I_{OH} = –50μA	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, A or B to $\overline{Y}$	V_{CC} = 3.3 ± 0.3V	C_L = 15 pF C_L = 50 pF		4.6 6.1	11.9 15.4	1.0 1.0	14.0 17.5	1.0 1.0	16.1 19.6	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15 pF C_L = 50 pF		3.6 4.3	7.7 9.7	1.0 1.0	9.0 11.0	1.0 1.0	10.3 12.3	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

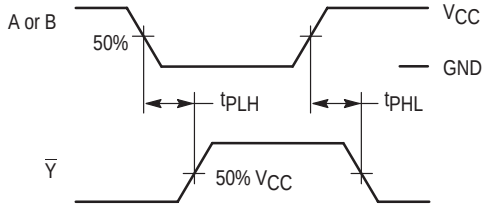
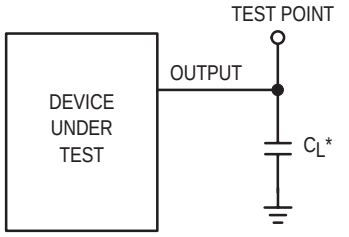


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G132DFT1	MC	74	VHC1G	132	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G135

Product Preview

2-Input NAND Schmitt-Trigger with Open Drain Output

The MC74VHC1G135 is a single gate CMOS Schmitt NAND trigger with an open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including an open drain output which provides the capability to set the output switching level. This allows the MC74VHC1G135 to be used to interface 5V circuits to circuits of any voltage between V_{CC} and 7V using an external resistor and power supply.

The MC74VHC1G135 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage.

The MC74VHC1G135 can be used to enhance noise immunity or to square up slowly changing waveforms.

- High Speed: t_{PD} = 4.9ns (Typ) at V_{CC} = 5V
- Low Internal Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

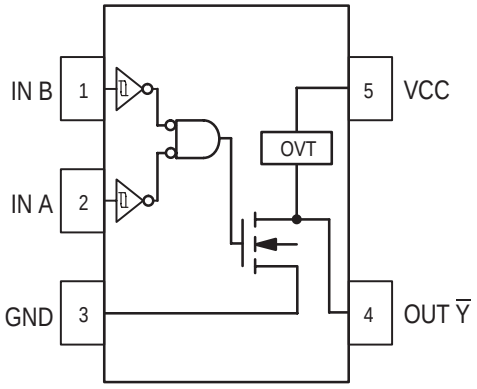


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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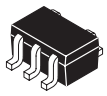
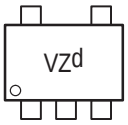


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 49 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	$\overline{\mathbf{Y}}$
L	L	Z
L	H	Z
H	L	Z
H	H	L

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MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
DC Input Voltage	V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{OUT}	–0.5 to 7.0	V
Input Diode Current	I_{IK}	–20	mA
Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	7.0	V
Operating Temperature Range	T_A	–55	+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5			2.20 3.15 3.85		2.20 3.15 3.85		2.20 3.15 3.85	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.9 1.35 1.65			0.9 1.35 1.65		0.9 1.35 1.65		V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50		1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage I_{OH} = –50μA	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{OPD}	Maximum Off–state Leakage Current	V_{OUT} = 5.5V	0			0.25		2.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PZL}	Maximum Output Enable Time, A or B to $\overline{Y}$	V_{CC} = 3.3 ± 0.3V, R_L = 1KΩ, C_L = 15 pF		7.6	11.9	1.0	14.0	1.0	16.1	ns
		V_{CC} = 3.3 ± 0.3V, R_L = 1KΩ, C_L = 50 pF		10.1	15.4	1.0	17.5	1.0	19.6	
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 15 pF		4.9	7.7	1.0	9.0	1.0	10.3	
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 50 pF		6.4	9.7	1.0	11.0	1.0	12.3	
t_{PLZ}	Maximum Output Disable Time	V_{CC} = 3.0 ± 0.3V, R_L = 1KΩ, C_L = 50 pF		10.1	15.4		17.5		19.6	ns
		V_{CC} = 5.0 ± 0.5V, R_L = 1KΩ, C_L = 50 pF		6.4	9.7		11.0		12.3	
C_{IN}	Maximum Input Capacitance			5.0	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	16	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

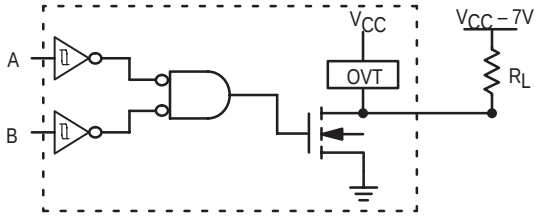


Figure 2. Output Voltage Mismatch Application

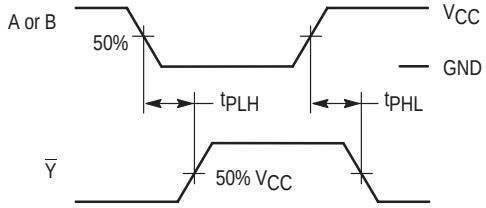
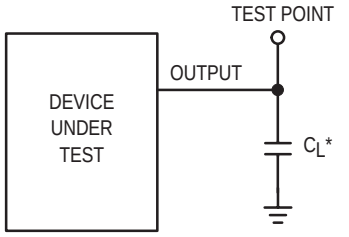


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G135DFT1	MC	74	VHC1G	135	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G14

Schmitt–Trigger Inverter

The MC74VHC1G14 is a single gate CMOS Schmitt–trigger inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G14 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G14 to be used to interface 5V circuits to 3V circuits.

The MC74VHC1G14 can be used to enhance noise immunity or to square up slowly changing waveforms.

- High Speed: t_{PD} = 4.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA

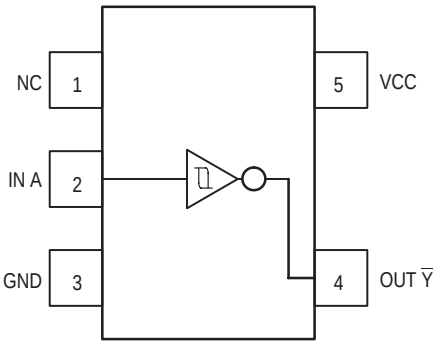
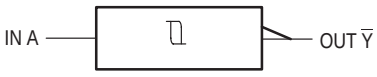


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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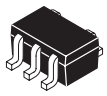
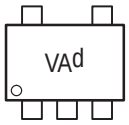


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 53 of this data sheet.

FUNCTION TABLE

A Input	Y Output
L	H
H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range	T_A	–55	+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5	1.85 2.86 3.50	2.0 3.0 3.6	2.20 3.15 3.85		2.20 3.15 3.85		2.20 3.15 3.85	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.9 1.35 1.65	1.5 2.3 2.9	1.65 2.46 3.05	0.9 1.35 1.65		0.9 1.35 1.65		V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50	0.57 0.67 0.74	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage I_{OH} = –50μA	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, A to $\overline{Y}$	V_{CC} = 3.3 ± 0.3V	C_L = 15 pF C_L = 50 pF		7.0 8.5	12.8 16.3	1.0 1.0	15.0 18.5	1.0 1.0	17.0 20.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15 pF C_L = 50 pF		4.0 5.5	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	11.5 13.5	
C_{IN}	Maximum Input Capacitance				5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	7.0	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

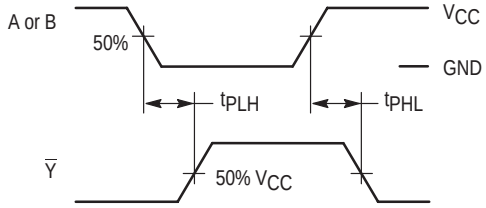
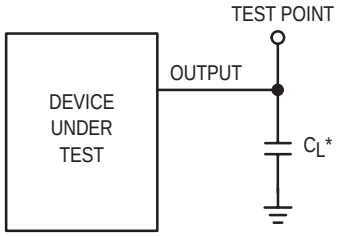


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G14DFT1	MC	74	VHC1G	14	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G32

2-Input OR Gate

The MC74VHC1G32 is an advanced high speed CMOS 2–input OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G32 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G32 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 3.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

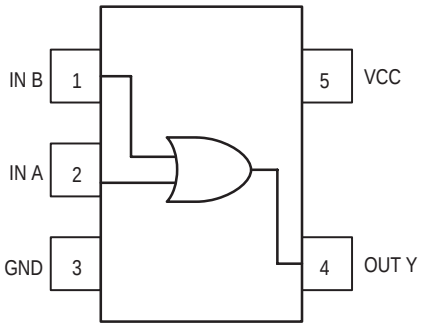
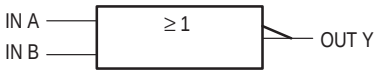


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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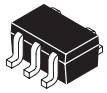
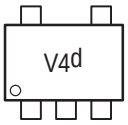


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 57 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.8 6.1	7.9 11.4		9.5 13.0		11.5 15.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.7 4.4	5.5 7.5		6.5 8.5		8.0 10.0	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

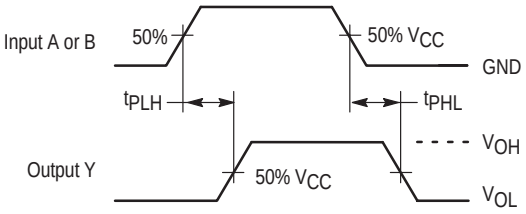
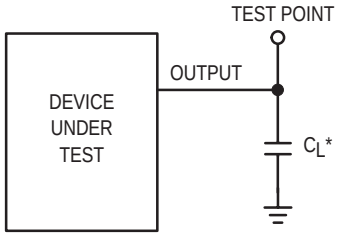


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

	Device Nomenclature							
Device Order Number	**Circuit Indicator**	**Temp Range Identifier**	**Technology**	**Device Function**	**Package Suffix**	**Tape & Reel Suffix**	**Package Type**	**Tape and Reel Size**
MC74VHC1G32DFT1	MC	74	VHC1G	32	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G66

Advance Information

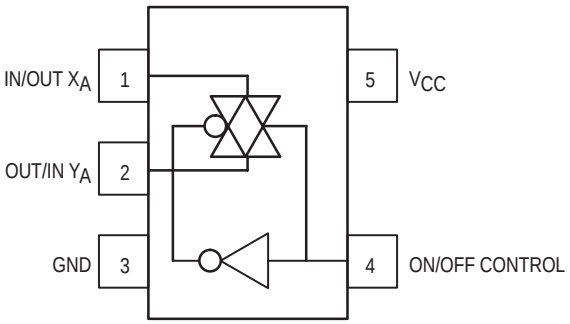
Analog Switch

The MC74VHC1G66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1G66 is compatible in function to a single gate of the High Speed CMOS MC74VHC4066 and the metal–gate CMOS MC14066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal–gate CMOS or High Speed CMOS analog switches.

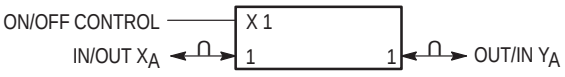
The ON/OFF control inputs are compatible with standard CMOS outputs; with pull–up resistors, it is compatible with LSTTL outputs.

- High Speed: t_{PD} = **TBD** (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14066 or the HC4066
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V
- Chip Complexity: 11 FETs or 3 Equivalent Gates



5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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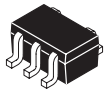
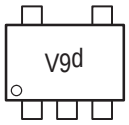


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 64 of this data sheet.

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

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ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Analog Output Voltage	V_{IS}	–0.5 to V_{CC} + 0.5	V
Digital Input Diode Current	I_{IK}	–20	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+25	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
Digital Input Voltage		V_{IN}	GND	V_{CC}	V
Analog Input Voltage		V_{IS}	GND	V_{CC}	V
Static or Dynamic Voltage Across Switch		V_{IO}*		1.2	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time ON/OFF Control Input		t_r , t_f			ns/V
	V_{CC} = 3.3V ± 0.3V		0	100	
	V_{CC} = 5.0V ± 0.5V		0	20	

* For voltage drops across the switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e. the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{IO} = 0V	5.5			2.0		20		40	μA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		30 20 15	50 30 20		70 40 35		100 50 45	Ω
		Endpoints V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		25 12 8	50 20 15		65 26 23		90 40 32	Ω
I_{OFF}	Maximum Off–Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 2)	5.5			0.1		0.5		1.0	μA
I_{ON}	Maximum On–Channel Leakage Current	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND Switch On (Figure 3)	5.5			0.1		0.5		1.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input X to Y	Y_A = Open Figure 4	2.0 3.0 4.5 5.5		1 0 0 0	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
t_{PZL}, t_{PZH}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Contol Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note NO TAG)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response Figure 7	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3dB R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 200	MHz
ISO_{off}	Off–Channel Feedthrough Isolation Figure 8	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0 kHz, R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	–40 –40 –40	
$NOISE_{feed}$	Feedthrough Noise Control to Switch Figure 9	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 2ns) Adjust R_L at setup so that I_S = 0 A R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
		R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	25 30 60	
THD	Total Harmonic Distortion Figure 10	f_{in} = 1 kHz, R_L = 10kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 4.5 5.5	 0.20 0.10 0.06	%

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

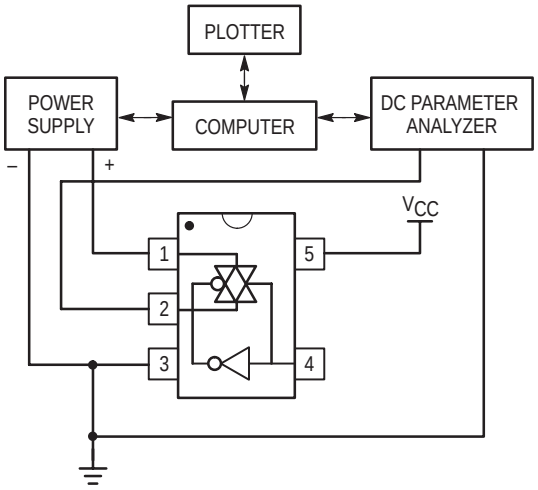


Figure 1. On Resistance Test Set–Up

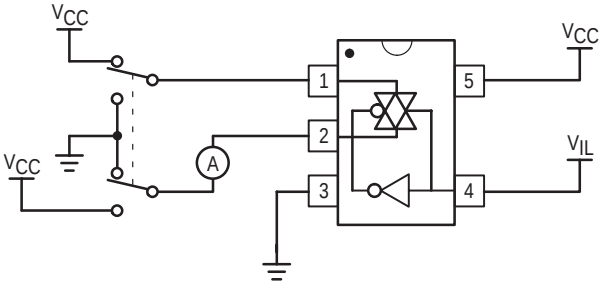


Figure 2. Maximum Off–Channel Leakage Current Test Set–Up

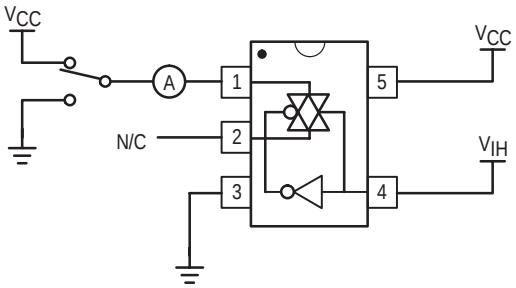


Figure 3. Maximum On–Channel Leakage Current Test Set–Up

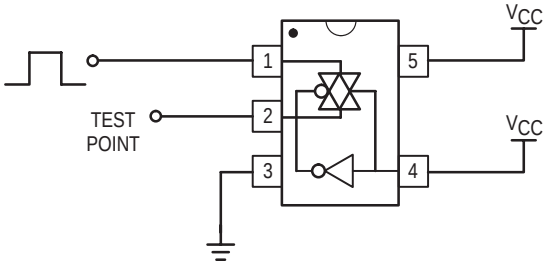


Figure 4. Propagation Delay Test Set–Up

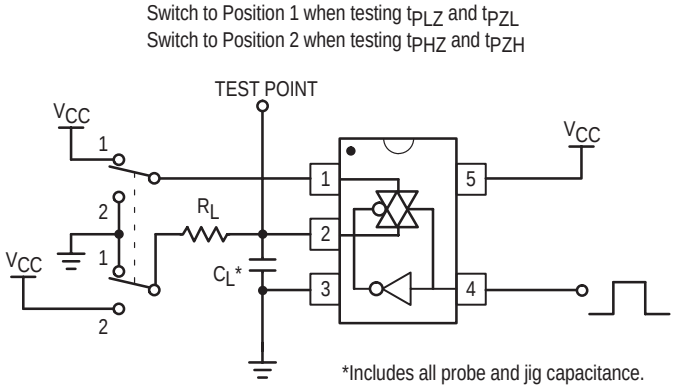


Figure 5. Propagation Delay Output Enable/Disable Test Set–Up

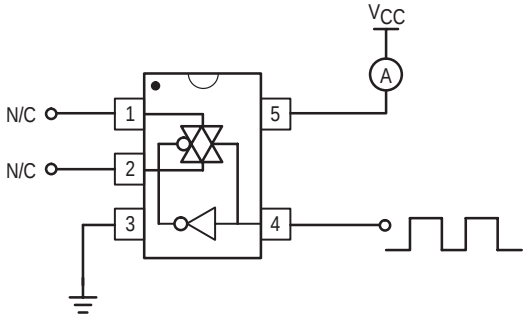


Figure 6. Power Dissipation Capacitance Test Set–Up

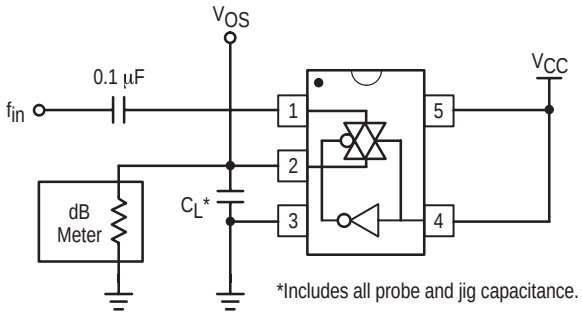


Figure 7. Maximum On–Channel Bandwidth Test Set–Up

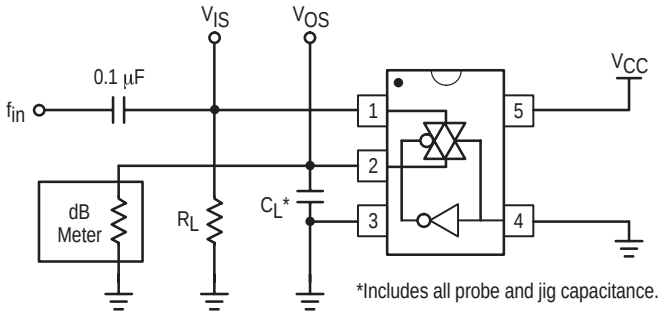


Figure 8. Off–Channel Feedthrough Isolation Test Set–Up

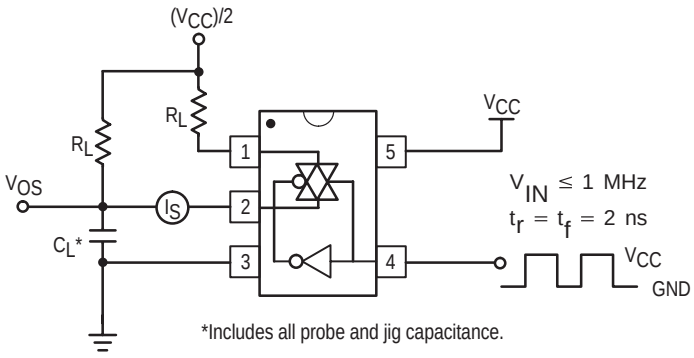


Figure 9. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

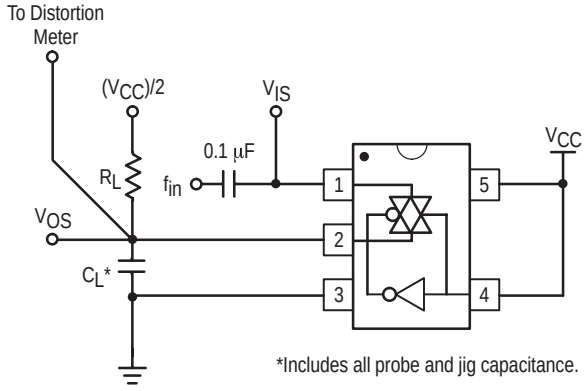


Figure 10. Total Harmonic Distortion Test Set–Up

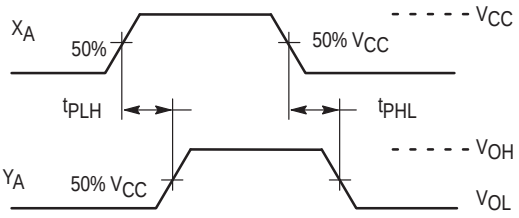


Figure 11. Propagation Delay, Analog In to Analog Out Waveforms

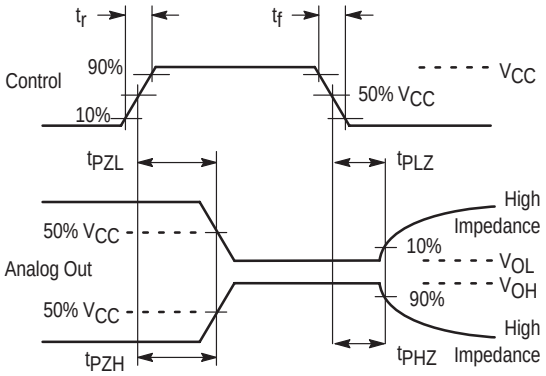


Figure 12. Propagation Delay, ON/OFF Control

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G66DFT1	MC	74	VHC1G	66	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1G86

2-Input Exclusive OR Gate

The MC74VHC1G86 is an advanced high speed CMOS 2–input Exclusive OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G86 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G86 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 3.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

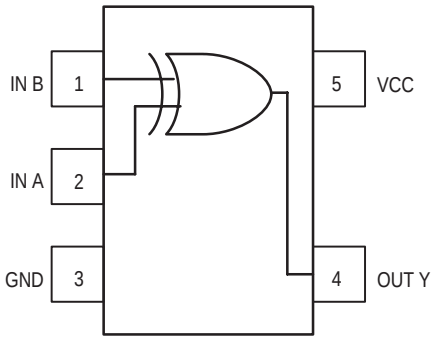
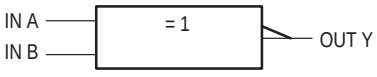


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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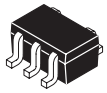
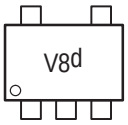


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 68 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.4 5.7	11.0 14.5		13.0 16.5		15.5 19.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.5 4.2	6.8 8.8		8.0 10.0		10.0 12.0	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	10	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

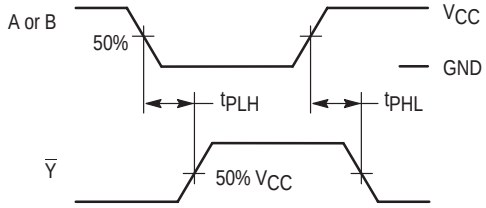
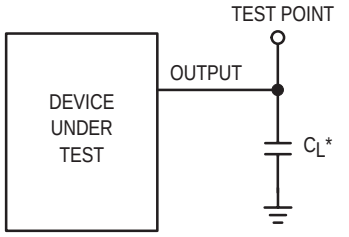


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G86DFT1	MC	74	VHC1G	86	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1GT00

2-Input NAND Gate / CMOS Logic Level Shifter

with LSTTL–Compatible Inputs

The MC74VHC1GT00 is a single gate 2–input NAND fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT00 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT00 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 3.1ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V

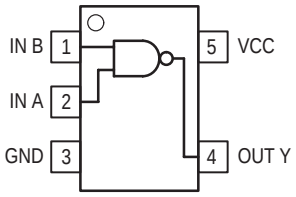
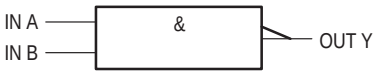


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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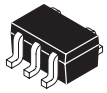
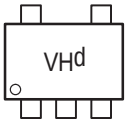


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 72 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –5 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4V$	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.1 5.5	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.1 3.6	6.9 7.9		8.0 9.0		9.5 10.5	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

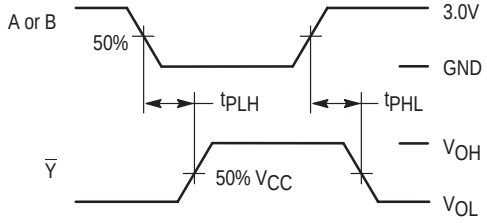
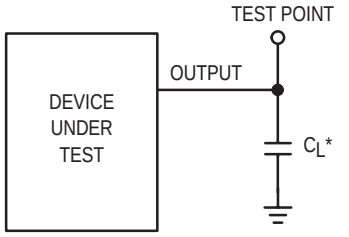


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech–nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT00DFT1	MC	74	VHC1G	T	00	DF	T1	SC–88A/ SOT–353	7–Inch/3000 Unit

MC74VHC1GT02

2-Input NOR Gate / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHC1GT02 is a single gate 2–input NOR fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT02 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT02 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 4.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V

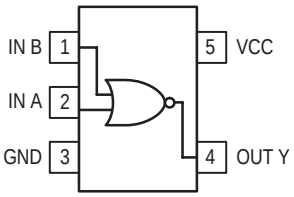
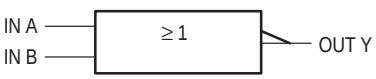


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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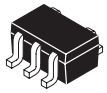
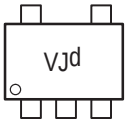


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 76 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –5 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Per Input: $V_{IN} = 3.4V$ Other Input: V_{CC} or GND	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.5 5.8	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.0 3.8	6.7 7.7		7.5 8.5		8.5 9.5	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

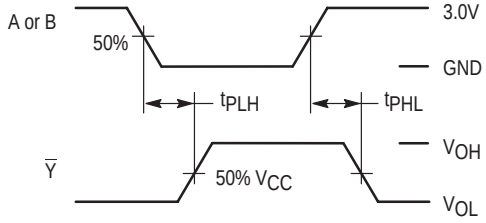
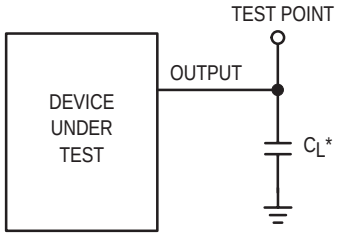


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech–nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT02DFT1	MC	74	VHC1G	T	02	DF	T1	SC–88A/ SOT–353	7–Inch/3000 Unit

MC74VHC1GT04

Inverting Buffer / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHC1GT04 is a single gate inverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT04 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT04 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 1500V; MM > 200V

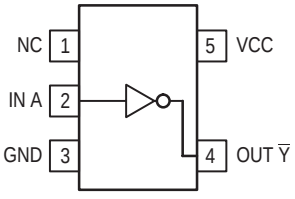
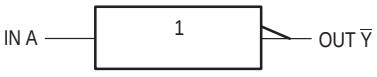


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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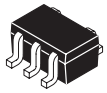
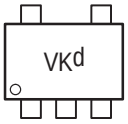


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 80 of this data sheet.

FUNCTION TABLE

A Input	Y Output
L	H
H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4V$	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A to $\overline{Y}$	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		5.0 6.2	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.8 4.2	6.7 7.7		7.5 8.5		8.5 9.5	
C_{IN}	Maximum Input Capacitance				5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	10	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

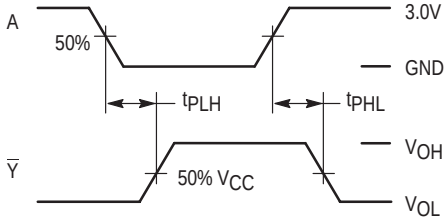
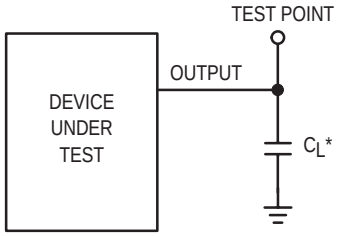


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech–nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT04DFT1	MC	74	VHC1G	T	04	DF	T1	SC–88A/ SOT–353	7–Inch/3000 Unit

MC74VHC1GT14

Schmitt-Trigger Inverter / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHC1GT14 is a single gate CMOS Schmitt–trigger inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT14 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT14 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc. The MC74VHC1GT14 can be used to enhance noise immunity or to square up slowly changing waveforms.

- High Speed: t_{PD} = 4.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA

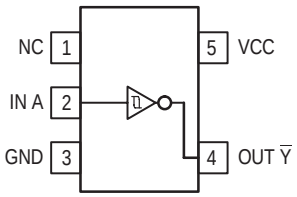
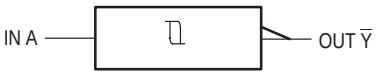


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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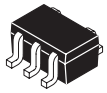
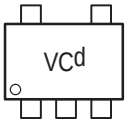


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT $\overline{Y}$
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 84 of this data sheet.

FUNCTION TABLE

A Input	$\overline{Y}$ Output
L	H
H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –5 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage	V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range	T_A	–55	+85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5	1.20 1.58 1.79	1.40 1.74 1.94	1.60 2.00 2.10		1.6 2.0 2.0		1.6 2.0 2.0	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.35 0.5 0.6	0.76 1.01 1.13	0.93 1.18 1.29	0.35 0.5 0.6		0.35 0.5 0.6		V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50	0.64 0.73 0.81	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage I_{OH} = –50μA	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, A to $\overline{Y}$	V_{CC} = 3.3 ± 0.3V	C_L = 15 pF C_L = 50 pF		7.0 8.4	12.8 16.3	1.0 1.0	15.0 18.5	1.0 1.0	17.0 20.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15 pF C_L = 50 pF		4.5 5.8	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	11.5 13.5	
C_{IN}	Maximum Input Capacitance				5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	10	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

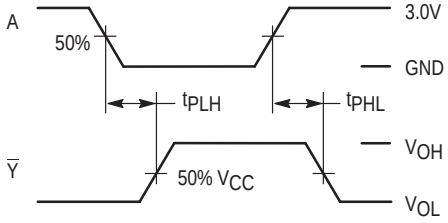
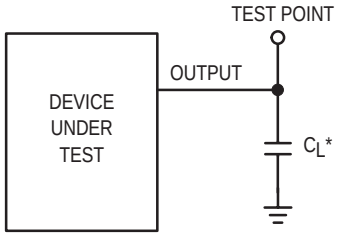


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech–nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT14DFT1	MC	74	VHC1G	T	14	DF	T1	SC–88A/ SOT–353	7–Inch/3000 Unit

MC74VHC1GT50

Noninverting Buffer / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHC1GT50 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT50 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT50 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 3.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 1500V; MM > 200V

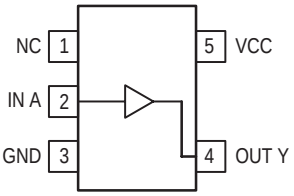
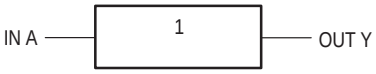


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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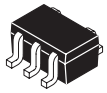
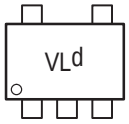


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 88 of this data sheet.

FUNCTION TABLE

A Input	Y Output
L	L
H	H

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4V$	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		4.5 6.3	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.5 4.3	6.7 7.7		7.5 8.5		8.5 9.5	
C_{IN}	Maximum Input Capacitance				5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	12	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

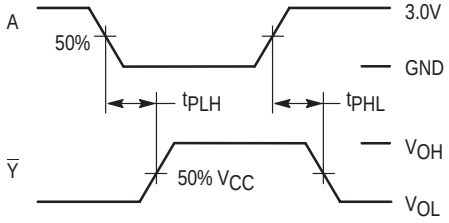
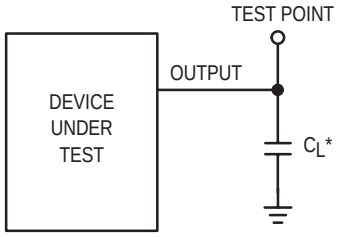


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech–nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT50DFT1	MC	74	VHC1G	T	50	DF	T1	SC–88A/ SOT–353	7–Inch/3000 Unit

MC74VHC1GT66

Advance Information

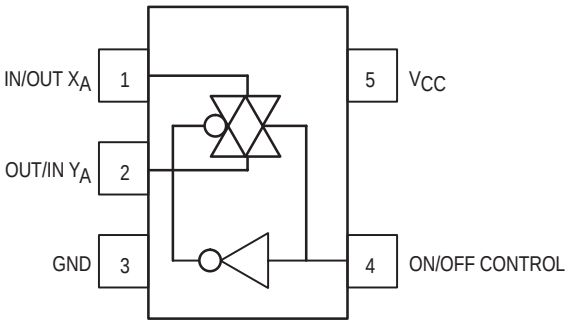
Analog Switch

The MC74VHC1GT66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1GT66 is compatible in function to a single gate of the very High Speed CMOS MC74VHCT4066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal–gate CMOS or High Speed CMOS analog switches.

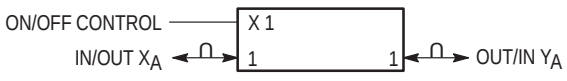
The ON/OFF Control input is compatible with TTL–type input thresholds allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS logic or from 1.8V CMOS logic to 3.0V CMOS logic while operating at the high–voltage power supply. The input protection circuitry on this device allows overvoltage tolerance on the input, which provides protection when voltages of up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT66 to be used to interface 5V circuits to 3V circuits.

- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V



5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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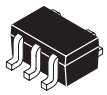
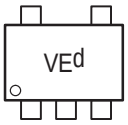


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 95 of this data sheet.

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

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ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Analog Output Voltage	V_{IS}	–0.5 to V_{CC} + 0.5	V
Digital Input Diode Current	I_{IK}	–20	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+25	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
Digital Input Voltage		V_{IN}	GND	V_{CC}	V
Analog Input Voltage		V_{IS}	GND	V_{CC}	V
Static or Dynamic Voltage Across Switch		V_{IO}*		1.2	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time ON/OFF Control Input		t_r , t_f			ns/V
	V_{CC} = 3.3V ± 0.3V		0	100	
	V_{CC} = 5.0V ± 0.5V		0	20	

* For voltage drops across the switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e. the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{IO} = 0V	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	ON/OFF Control at 3.4V	5.5			1.35		1.5		1.65	mA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		30 20 15	50 30 20		70 40 35		100 50 45	Ω
		Endpoints V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		25 12 8	50 20 15		65 26 23		90 40 32	Ω
I_{OFF}	Maximum Off–Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 2)	5.5			0.1		0.5		1.0	μA
I_{ON}	Maximum On–Channel Leakage Current	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND Switch On (Figure 3)	5.5			0.1		0.5		1.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input X to Y	Y_A = Open Figure 4	2.0 3.0 4.5 5.5		1 0 0 0	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
t_{PZL}, t_{PZH}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Contol Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note NO TAG)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response Figure 7	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3dB R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 200	MHz
ISO_{off}	Off–Channel Feedthrough Isolation Figure 8	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0 kHz, R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	–40 –40 –40	
$NOISE_{feed}$	Feedthrough Noise Control to Switch Figure 9	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 2ns) Adjust R_L at setup so that I_S = 0 A R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
		R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	25 30 60	
THD	Total Harmonic Distortion Figure 10	f_{in} = 1 kHz, R_L = 10kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 4.5 5.5	 0.20 0.10 0.06	%

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

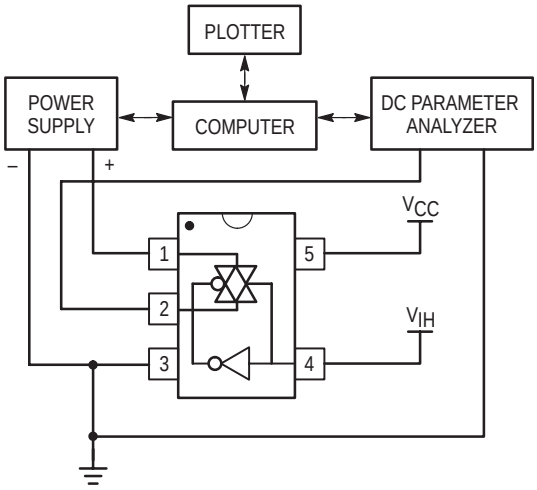


Figure 1. On Resistance Test Set–Up

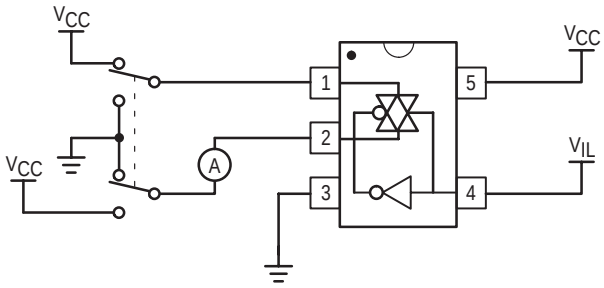


Figure 2. Maximum Off–Channel Leakage Current Test Set–Up

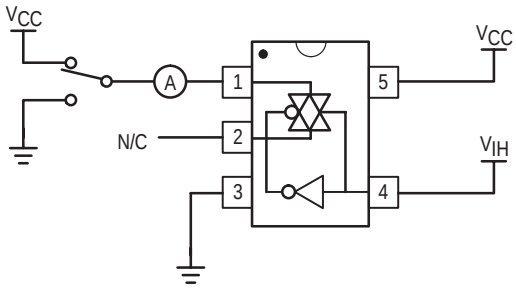


Figure 3. Maximum On–Channel Leakage Current Test Set–Up

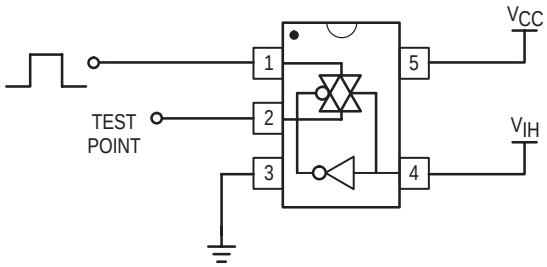


Figure 4. Propagation Delay Test Set–Up

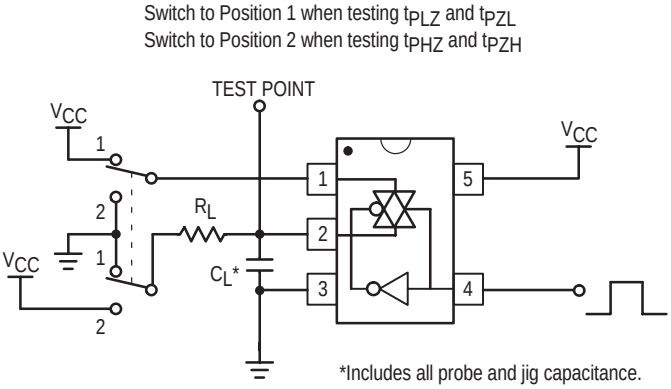


Figure 5. Propagation Delay Output Enable/Disable Test Set–Up

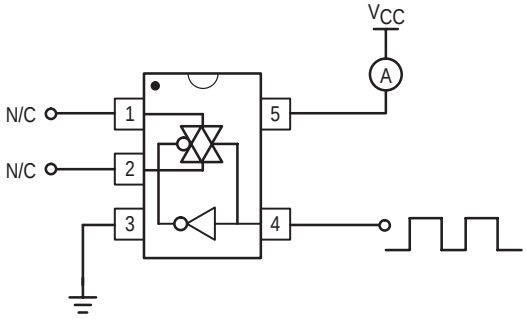


Figure 6. Power Dissipation Capacitance Test Set–Up

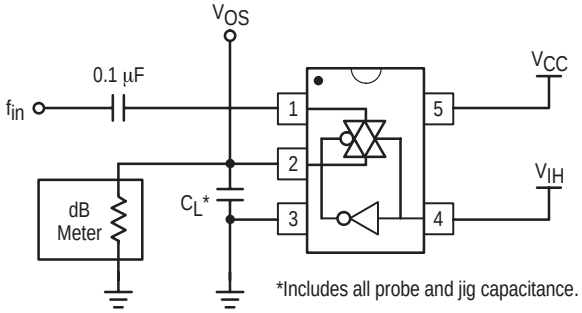


Figure 7. Maximum On–Channel Bandwidth Test Set–Up

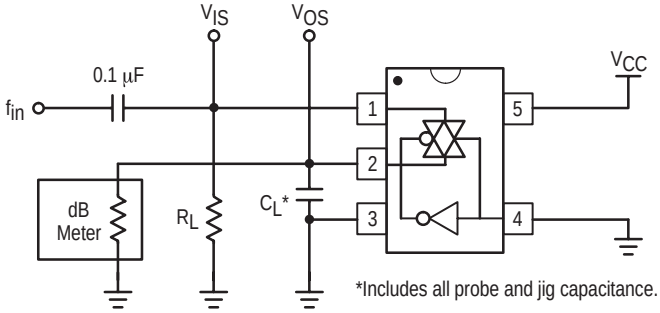


Figure 8. Off–Channel Feedthrough Isolation Test Set–Up

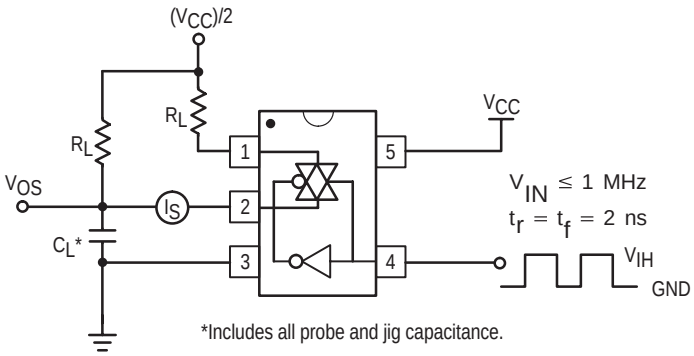


Figure 9. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

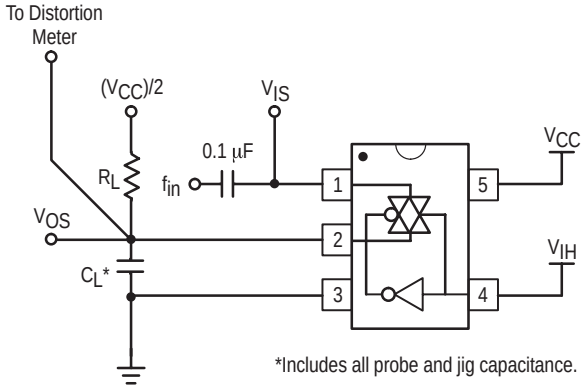


Figure 10. Total Harmonic Distortion Test Set–Up

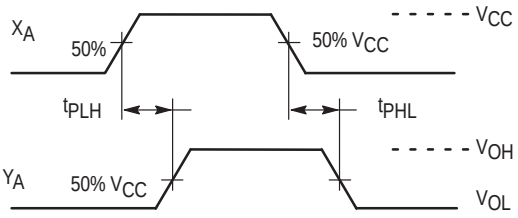


Figure 11. Propagation Delay, Analog In to Analog Out Waveforms

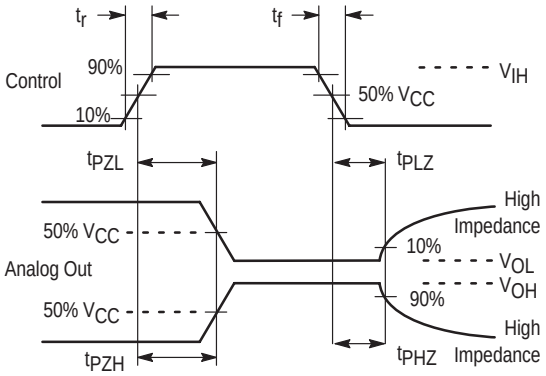


Figure 12. Propagation Delay, ON/OFF Control

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT66DFT1	MC	74	VHC1G	T66	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1GT86

2-Input Exclusive OR Gate / CMOS Logic Level Shifter
with LSTTL–Compatible Inputs

The MC74VHC1GT86 is an advanced high speed CMOS 2–input Exclusive OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL–type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high–voltage power supply.

The MC74VHC1GT86 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT86 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 4.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- CMOS–Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V

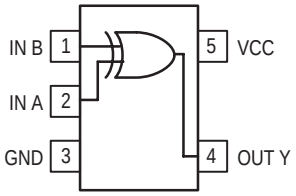
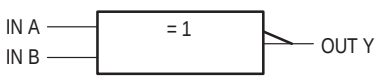


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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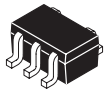
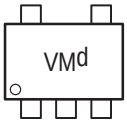


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 99 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4V$	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		5.0 6.2	11.0 14.5		13.0 16.5		15.5 19.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		3.1 4.2	6.8 8.8		8.0 10.0		10.0 12.0	
C_{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

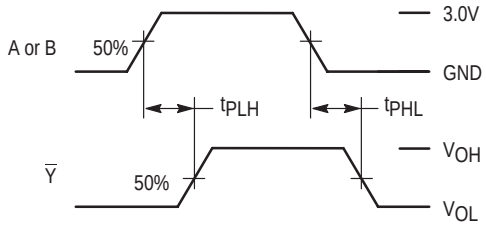
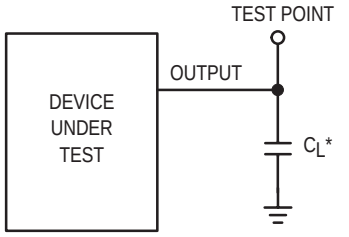


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech–nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT86DFT1	MC	74	VHC1G	T	86	DF	T1	SC–88A/ SOT–353	7–Inch/3000 Unit

MC74VHC1GU04

Unbuffered Inverter

The MC74VHC1GU04 is an advanced high speed CMOS Unbuffered inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This device consists of a single unbuffered inverter. In combination with others, or in the MC74VHCU04 Hex Unbuffered Inverter, these devices are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high–input impedance amplifier. For digital applications, the MC74VHC1G04 or the MC74VHC04 are recommended.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1GU04 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GU04 to be used to interface 5V circuits to 3V circuits.

- High Speed: t_{PD} = 2.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA

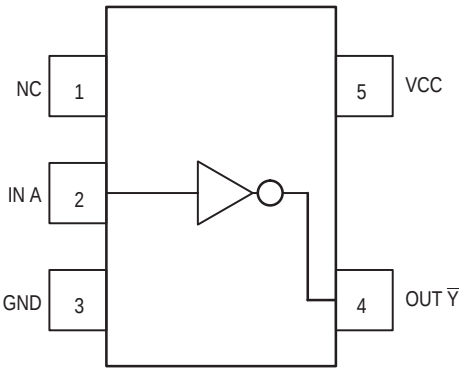
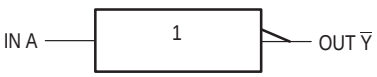


Figure 1. 5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



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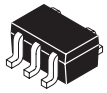
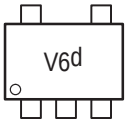


SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 103 of this data sheet.

FUNCTION TABLE

A Input	Y Output
L	H
H	L

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MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to +7.0	V
DC Output Voltage	V_{CC} = 0 High or Low State	V_{OUT}	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	–20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	+20	mA
DC Output Current, per Pin		I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND		I_{CC}	+50	mA
Power dissipation in still air, SC–88A †		P_D	200	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –5 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
DC Input Voltage		V_{IN}	0.0	5.5	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	0 0	No Limit No Limit	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.7 2.4 3.6 4.4			1.7 2.4 3.6 4.4		1.7 2.4 3.6 4.4		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.3 0.6 0.9 1.1		0.3 0.6 0.9 1.1		0.3 0.6 0.9 1.1	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5V$ or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A to $\overline{Y}$	$V_{CC} = 3.0 \pm 0.3V$	C_L = 15 pF C_L = 50 pF		3.5 4.8	8.9 11.4		10.5 13.0		12.0 15.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	C_L = 15 pF C_L = 50 pF		2.5 3.8	5.5 7.0		6.5 8.0		8.0 9.5	
C_{IN}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	22	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

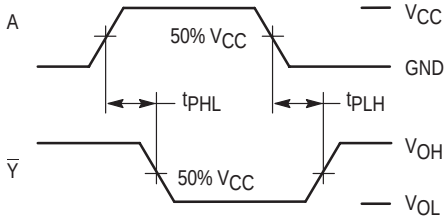
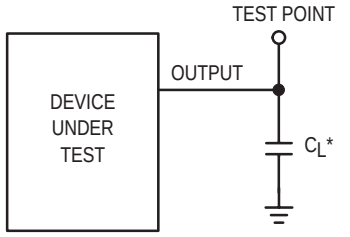


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GU04DFT1	MC	74	VHC1G	U04	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

Application Notes

AND8004/D

ON Semiconductor Logic Date Code and Traceability Marking

Douglas Buzard, Logic Product Engineering

ON Semiconductor
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APPLICATION NOTE

Introduction

This is a summary of ON Semiconductor Logic Device, Date Code, and Traceability Marking. We want to provide our customers with easy access to this information on the web. This applications note summarizes and explains the Date Code and Traceability Marking for Logic packages. This is not intended to replace the proper documentation. To properly decode the Logic marking you need 12MRH00191A ON Semiconductor marking spec and S.O.P. 7–19 ID of Products to Location of Test/Assy/Wafer Fab. Also, you need to know the abbreviations used for Logic products(see the appropriate Logic datasheet for the specific device naming/ordering information).

Device Marking

Logic Families

The standard Logic abbreviations are:

```
LS                  = Low Power Schottky Logic
14xxx               = Metal Gate CMOS Logic
HC, HCT             = High Speed CMOS Logic
AC, ACT, JLC        = FACT – Fairchild Advanced CMOS Technology
VHC, VHCT           = Very High Speed CMOS Logic
LVX, LVXT           = Low–Voltage Very High Speed CMOS
LCX                 = Low–Voltage CMOS Logic
ALVC, VCX           = Advanced Low–Voltage CMOS Logic
```

Logic Packages

The standard Logic package suffixes are:

```
N = Plastic Dual–In–Line
P = Metal Gate CMOS Plastic Dual–In–Line
D = SOIC Narrow Body
DW = SOIC Wide Body
F = EIAJ Plastic Mini Flat Pack
M = EIAJ Plastic Mini Flat Pack
DT = TSSOP
DF = SOT–353/363 or SC–88A/SC–88
```

All of the above except DF, F, and M can be combined with an R2 suffix for tape and reel. The tape and reel suffixes for EIAJ Plastic Mini Flat Pack include EL, L1, L2, F1, F2 depending upon the type of tape and the orientation of the part in the tape pocket. The DF package can be combined with a T1 or T2 tape and reel suffix that specifies the orientation of the part in the tape pocket.

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Device Marking

Typical Device naming in Logic consists of the following:

Brand	Temp rating	Logic family	Logic function	Package	Tape and reel
MC	74	VHC	T138A	DT	R2

Plastic dual–in–line packages and larger SOIC packages can accommodate the entire device name excluding the tape and reel suffix.

Smaller package types with limited space on package for marking are either truncated or abbreviated. The SOT packages use a code for the Logic family and device type.

On TSSOP and some SOIC, the device name will be truncated by removing the MC74 prefix, and any package suffixes.

Example:
Marking — Device
HC04A = MC74HC04ADR2

Marking — Device
LCX
244 = MC74LCX244DTR2

Marking — Device
VL = MC74VHC1GT50DFT1

PC/XC Device Marking

New Prototype ”PC” devices and new pre–production release, pre–reliability ”XC” devices:

P = PC
X = XC

The first character is the ”PC” or ”XC” identifier. For a variety of reasons, the remaining characters have not been standardized for different engineering devices. On these devices the date code will be the most important item.

Date and Traceability Code Markings

TSSOP Packages

8 ld TSSOP = ”YWW” front side and ”AWL” back side

```
”Y”  – The First code is 2 characters and indicates the Year Assembled.
”WW”  – The Second & Third code is 2 characters and indicates the Work Week Assembled.

XXXX = Part number
643 = ”YWW” front side
|||
6|| = 1996
 ||
 43 = WW43

”A”  – The First code is 1 or 2 characters indicating the Assembly Location
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.

XAA = ”AWL” back side
|||
X|| = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P.7–19)
 ||
 AA = First Lot Assembled for that Device Type in that (Work Week).
```

14/16/20/24 ld TSSOP = ”AWLYWW”

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”Y”  – The Fourth code is 2 characters and indicates the Year Assembled.
”WW”  – The Fifth & Sixth code is 2 characters and indicates the Work Week Assembled.

VHCT
244A   = MC74VHCT244ADT
XAA643 = ”AWLYWW”
||||||
X||||| = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P.7–19)
 |||||
 AA||| = First Lot Assembled for that Device Type in that (Work Week).
   |||
   6|| = 1996
    ||
    43 = WW43
```

48/56 ld TSSOP = ”AWLYYWW”

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location.
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”YY”  – The Fourth & Fifth code is 2 characters and indicates the Year Assembled.
”WW”  – The Sixth & Seventh code is 2 characters and indicates the Work Week Assembled.

MC74LCX16244    = MC74LCX16244DT
PAA9646 = ”AWLYYWW”
|||||||
P|||||| = ON Semiconductor Carmona, Philippines. Assy Location.(S.O.P.7–19)
 ||||||
 AA|||| = First Lot Assembled for that Device Type in that (Work Week).
   ||||
   96|| = 1996
     ||
     46 = WW46
```

SOT Packages

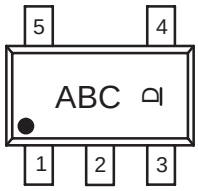
5 ld SOT–353/SC–88A

PACKAGE HEIGHT	DEVICE MARKING HEIGHT	DATE CODE HEIGHT	LOGO HEIGHT	POLARITY BAND
SMC	.040”–.060”	.040”–.060”	.040”–.060”	N/A

Figure 1 illustrates the marking format for SOT–353, and SC88A devices. The laser marking is to appear on the top of the package and be oriented per Figure 1A.

”ABC” illustrates toe location of the Device Code which is specified below and by the device 48A. ”D” illustrates the location of the Date Code.

Figure 1.



DATE CODES:

SOT–23, SC59, SC596L, TSOP6, SC70, SC706L, SC90, SOD123, SOD323, POWERMITE, SC88A, SOT–353, AND SOT143

MONTH	DATE CODE	MONTH	DATE CODE	MONTH	DATE CODE	MONTH	DATE CODE
1994		1995		1996		1997	
JAN	Y	JAN	M	JAN	E	JAN	1
FEB	Z	FEB	N	FEB	F	FEB	2
MAR	C	MAR	O	MAR	H	MAR	3
APR	D	APR	P	APR	J	APR	4
MAY	E	MAY	R	MAY	K	MAY	5
JUN	F	JUN	T	JUN	L	JUN	6
JUL	G	JUL	U	JUL	N	JUL	7
AUG	H	AUG	V	AUG	P	AUG	8
SEP	I	SEP	9	SEP	U	SEP	9
OCT	J	OCT	X	OCT	X	OCT	T
NOV	K	NOV	Y	NOV	Y	NOV	V
DEC	L	DEC	Z	DEC	Z	DEC	C
1998		1999		2000		2001	
JAN	E	JAN	1	JAN	E	JAN	1
FEB	F	FEB	2	FEB	F	FEB	2
MAR	H	MAR	3	MAR	H	MAR	3
APR	J	APR	4	APR	J	APR	4
MAY	K	MAY	5	MAY	K	MAY	5
JUN	L	JUN	6	JUN	L	JUN	6
JUL	N	JUL	7	JUL	N	JUL	7
AUG	P	AUG	8	AUG	P	AUG	8
SEP	U	SEP	9	SEP	U	SEP	9
OCT	X	OCT	T	OCT	X	OCT	T
NOV	Y	NOV	V	NOV	Y	NOV	V
DEC	Z	DEC	C	DEC	Z	DEC	C

DEVICE CODES:

SOT–23, SC59, SC88A, SOT–353

```
Family ID     HSL : H
              VHC : V & W
              LCX : L
             ALVC : C & D
```

Device Function

FUNC	ID	HSL	VHC	LCX	ALVC
00	1	H1	V1	L1	C1
T00	H	–	VH	–	–
01	0		V0		C0
02	3	H3	V3	L3	C3
T02	J	–	VJ	–	
03	P		VP		CP
04	5	H5	V5	L5	C5
T04	K	–	VK	–	
U04	6	H6	V6	L6	C6
05	F		VF		CF
07	7		V7		
08	2	H2	V2	L2	C2
T08	T	–	VT	–	
09	X		VX		CX
14	A	HA	VA	LA	CA
T14	C	–	VC	–	
32	4	H4	V4	L4	C4
T32	N	–	VN	–	
50	R	–	VR	–	CR
T50	L	–	VL	–	–
54	V	–	VV	–	
T54	W	–	VW	–	
66	9	–	V9	L9	C9
T66	E	–	VE	L9	
86	8	H8	V8	L8	C8
T86	M	–	VM	–	
132	D	–	VD	–	CD
T132	U	–	VU	–	
135	Z	–	VZ	–	CZ

SOIC Packages

8 ld SOIC = ”ALYW”

”A” – The First character indicates the location of Assembly Location.
”L” – The Second character indicates the Wafer Lot Tracking Code.
”Y” – The Third character indicate an ”ALPHA CODE” of the Year assembled.
”W” – The Fourth character indicate an ”ALPHA CODE” of the Work Week assembled.

The ”Y” YEAR Alpha Codes are:

A = 1989 First	6 months,	WW01 – WW26
B = 1989 Second	6 months,	WW27 – WW52
C = 1990 First	6 months,	WW01 – WW26
D = 1990 Second	6 months,	WW27 – WW52
E = 1991 First	6 months,	WW01 – WW26
F = 1991 Second	6 months,	WW27 – WW52
G = 1992 First	6 months,	WW01 – WW26
H = 1992 Second	6 months,	WW27 – WW52
I = 1993 First	6 months,	WW01 – WW26
J = 1993 Second	6 months,	WW27 – WW52
K = 1994 First	6 months,	WW01 – WW26
L = 1994 Second	6 months,	WW27 – WW52
M = 1995 First	6 months,	WW01 – WW26
N = 1995 Second	6 months,	WW27 – WW52
O = 1996 First	6 months,	WW01 – WW26
P = 1996 Second	6 months,	WW27 – WW52
Q = 1997 First	6 months,	WW01 – WW26
R = 1997 Second	6 months,	WW27 – WW52
S = 1998 First	6 months,	WW01 – WW26
T = 1998 Second	6 months,	WW27 – WW52
U = 1999 First	6 months,	WW01 – WW26
V = 1999 Second	6 months,	WW27 – WW52
W = 2000 First	6 months,	WW01 – WW26
X = 2000 Second	6 months,	WW27 – WW52
Y = 2001 First	6 months,	WW01 – WW26
Z = 2001 Second	6 months,	WW27 – WW52

The ”W” Work Week Alpha Codes are:

First 6 months WW01 – WW26	Second 6 months WW27 – WW52
A = 01	A = 27
B = 02	B = 28
C = 03	C = 29
D = 04	D = 30
E = 05	E = 31
F = 06	F = 32
G = 07	G = 33
H = 08	H = 34
I = 09	I = 35
J = 10	J = 36
K = 11	K = 37
L = 12	L = 38
M = 13	M = 39
N = 14	N = 40
O = 15	O = 41
P = 16	P = 42
Q = 17	Q = 43
R = 18	R = 44
S = 19	S = 45
T = 20	T = 46
U = 21	U = 47
V = 22	V = 48
W = 23	W = 49
X = 24	X = 50
Y = 25	Y = 51
Z = 26	Z = 52

From this information you can determine the date codes:
Examples:

```
PANS,
||||
P||| = ON Semiconductor Carmona, Philippines. Assy Location.(S.O.P.7–19)
 |||
 A|| = First Lot Assembled for that Device Type in that Alpha Code (Work Week).
  ||
  N| = 1995 Second 6 months, WW27 – WW52
   |
   S = WW45 (Y95 WW45)
```

```
XBST,
||||
X||| = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P. 7–19)
 |||
 B|| = Second Lot Assembled for that Device Type in that Alpha Code (Work Week).
  ||
  S| = 1998 First 6 months, WW01 – WW26
   |
   T = WW20 (Y98 WW20)
```

14/16 ld SOIC Narrow Body = ”AWLYWW”

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”Y”  – The Fourth code is 2 characters and indicates the Year Assembled.
”WW”  – The Fifth & Sixth code is 2 characters and indicates the Work Week Assembled.
```

```
LCX00 = MC74LCX00D
XAA643 = ”AWLYWW”
||||||
X|||||  = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P.7–19)
 |||||
 AA|||  = First Lot Assembled for that Device Type in that (Work Week).
   |||
   6||  = 1996
    ||
    43 = WW43
```

16/20/24 ld SOIC Wide Body = ”AWLYYWW”

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location.
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”YY”  – The Fourth & Fifth code is 2 characters and indicates the Year Assembled.
”WW”  – The Sixth & Seventh code is 2 characters and indicates the Work Week Assembled.
```

```
VHCT244A = MC74VHCT244ADW
PAA9646 = ”AWLYYWW”
|||||||
P||||||  = ON Semiconductor Carmona, Philippines. Assy Location.(S.O.P.7–19)
 ||||||
 AA||||  = First Lot Assembled for that Device Type in that (Work Week).
   ||||
   96||  = 1996
     ||
     46 = WW46
```

EIAJ Mini Flat Pack Packages

8/14/16 ld MFP = ”ALYW”

”A” – The First character indicates the location of Assembly Location.
”L” – The Second character indicates the Wafer Lot Tracking Code.
”Y” – The Third character indicate an ”ALPHA CODE” of the Year assembled.
”W” – The Fourth character indicate an ”ALPHA CODE” of the Work Week assembled.

The ”Y” YEAR Alpha Codes are:

A = 1989 First	6 months,	WW01 – WW26
B = 1989 Second	6 months,	WW27 – WW52
C = 1990 First	6 months,	WW01 – WW26
D = 1990 Second	6 months,	WW27 – WW52
E = 1991 First	6 months,	WW01 – WW26
F = 1991 Second	6 months,	WW27 – WW52
G = 1992 First	6 months,	WW01 – WW26
H = 1992 Second	6 months,	WW27 – WW52
I = 1993 First	6 months,	WW01 – WW26
J = 1993 Second	6 months,	WW27 – WW52
K = 1994 First	6 months,	WW01 – WW26
L = 1994 Second	6 months,	WW27 – WW52
M = 1995 First	6 months,	WW01 – WW26
N = 1995 Second	6 months,	WW27 – WW52
O = 1996 First	6 months,	WW01 – WW26
P = 1996 Second	6 months,	WW27 – WW52
Q = 1997 First	6 months,	WW01 – WW26
R = 1997 Second	6 months,	WW27 – WW52
S = 1998 First	6 months,	WW01 – WW26
T = 1998 Second	6 months,	WW27 – WW52
U = 1999 First	6 months,	WW01 – WW26
V = 1999 Second	6 months,	WW27 – WW52
W = 2000 First	6 months,	WW01 – WW26
X = 2000 Second	6 months,	WW27 – WW52
Y = 2001 First	6 months,	WW01 – WW26
Z = 2001 Second	6 months,	WW27 – WW52

The ”W” Work Week Alpha Codes are:

First 6 months WW01 – WW26	Second 6 months WW27 – WW52
A = 01	A = 27
B = 02	B = 28
C = 03	C = 29
D = 04	D = 30
E = 05	E = 31
F = 06	F = 32
G = 07	G = 33
H = 08	H = 34
I = 09	I = 35
J = 10	J = 36
K = 11	K = 37
L = 12	L = 38
M = 13	M = 39
N = 14	N = 40
O = 15	O = 41
P = 16	P = 42
Q = 17	Q = 43
R = 18	R = 44
S = 19	S = 45
T = 20	T = 46
U = 21	U = 47
V = 22	V = 48
W = 23	W = 49
X = 24	X = 50
Y = 25	Y = 51
Z = 26	Z = 52

From this information you can determine the date codes:
Examples:

```
PANS,
||||
P||| = ON Semiconductor Carmona, Philippines. Assy Location.(S.O.P.7–19)
 |||
 A|| = First Lot Assembled for that Device Type in that Alpha Code (Work Week).
  ||
  N| = 1995 Second 6 months, WW27 – WW52
   |
   S = WW45 (Y95 WW45)
```

```
XBST,
||||
X||| = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P. 7–19)
 |||
 B|| = Second Lot Assembled for that Device Type in that Alpha Code (Work Week).
  ||
  S| = 1998 First 6 months, WW01 – WW26
   |
   T = WW20 (Y98 WW20)
```

20 ld MFP = ”AWLYWW”

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”Y”  – The Fourth code is 2 characters and indicates the Year Assembled.
”WW”  – The Fifth & Sixth code is 2 characters and indicates the Work Week Assembled.

LVX240 = MC74LVX240M
XAA643 = ”AWLYWW”
||||||
X|||||  = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P.7–19)
 |||||
 AA|||  = First Lot Assembled for that Device Type in that (Work Week).
   |||
   6||  = 1996
    ||
    43  = WW43
```

Plastic Dual–In–Line(PDIP) Packages

8 ld PDIP = ”AWL” and ”YYWW”

```
XXXX = Part number
 XAA = ”AWL”
9643 = ”YYWW”
```

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”YY”  – The Fourth & Fifth code is 2 characters and indicates the Year Assembled.
”WW”  – The Sixth & Seventh code is 2 characters and indicates the Work Week Assembled.
```

```
XAA = ”AWL”
|||
X|| = ASE  Chung–Li, Taiwan. Assy Location.(S.O.P.7–19)
 ||
 AA = First Lot Assembled for that Device Type in that (Work Week).
```

```
9643 = ”YYWW”
||||
96|| = 1996
  ||
  43 = WW43
```

14/16/18/20/24 ld PDIP = ”AWLYYWW”

```
”A”  – The First code is 1 or 2 characters indicating the Assembly Location
”WL”  – The Second & Third code is 2 characters and indicates the Wafer Lot Tracking Code.
”YY”  – The Fourth & Fifth code is 2 characters and indicates the Year Assembled.
”WW”  – The Sixth & Seventh code is 2 characters and indicates the Work Week Assembled.
```

```
MC74HC00AN   = MC74HC00AN
CPAA9646 = ”AWLYYWW”
||||||||
ZR|||||| = AAPI Manila, Philippines. Assy Location.(S.O.P.7–19)
  ||||||
  DK|||| = Lot Assembled for that Device Type in that (Work Week).
    ||||
    99|| = 1998
      ||
      02 = WW02
```

```
MC74HCT244AN   = MC74HCT244AN
CPAA9646 = ”AWLYYWW”
||||||||
CP|||||| = Astra(AMT) Batam Island, Indonesia. Assy Location.(S.O.P.7–19)
  ||||||
  AA|||| = First Lot Assembled for that Device Type in that (Work Week).
    ||||
    98|| = 1998
      ||
      21 = WW21
```

APPENDIX 1 – Assembly Location Codes

Codes used in the previous pages to denote assembly site location.

B	ON SEMI PHX	PHOENIX, ARIZONA (52ND ST)	
BG	PANTRONIX, INC	SAN JOSE, CALIFORNIA	
C	CARSEM (M) (old plant)	IPOH, MALAYSIA	
CB	PHENITEC / TOREX (T/T)	IBARA, JAPAN	
CK	ASE (M) OR ASE	PENANG, MALAYSIA	or ”1” for SOIC 8 LD or smaller packages
CM	ON SEMI MSL	SINGAPORE	
CP	ASTRA (AMT)	BATAM ISLAND, INDONESIA	or ”2” for SOIC 8 LD or smaller packages
CV	MITSUI SHAH ALAM (MSA)	SHAH ALAM, MALAYSIA	
DJ	CARSEM (S) (new plant)	IPOH, MALAYSIA	or ”3” for SOIC 8 LD or smaller packages
DQ	SMP (SEMICONDUCTOR MINIATURE PRODUCTS)	SEREMBAN, MALAYSIA ON SEMI–PHILIPS JOINT VENTURE	
DX	ANAM K3 (BUPYUNG)	BUPYUNG, KOREA	
F	ON SEMI MPI	MANILA, PHILIPPINES	
I	ANAM K1 (HWAYANG–DONG)	SEOUL, KOREA	
J	ON SEMI NML	AIZU, JAPAN	
K	*ASE–MKL	SEOUL, KOREA	
MC	AMD (Assembly)	BANGKOK, THAILAND	
MD	AMD (Test)	PENANG, MALAYSIA	
MI	CHARTERED SEMICONDUCTORS	SINGAPORE	
MX	MITSUI–KUMAMOTO (formerly KIKUCHI–GUN, TAIWAN LITEON ELEC)	KUMAMOTOKEN, JAPAN	
ND	TOSHIBA IWATE	IWATE–KITAKAMI, JAPAN	
NL	TESLA–SEZAM	ROSNOV, CZECH REPUBLIC	
NP	TOSHIBA OHITA	OHITA–KITAKYUSHU, JAPAN	
NR	LANSDALE	TEMPE, ARIZONA	
P	ON SEMI MPC	CARMONA, PHILIPPINES	
PR	AAP3	LAGUNA, PHILIPPINES	
QW	ASE (P)	MANILA, PHILIPPINES	or ”1” for SOIC 8 LD or smaller packages
R	ON SEMI SBN	SEREMBAN, MALAYSIA	
SB	ANAM K4 (KWANG JU)	KWANG JU, KOREA	
SE	BEST ELECTRONICS (BECCI)	METRO MANILA, PHILIPPINES	
TE	STM	SINGAPORE	
TF	*SLOVAKIAN ELECTRONICS	PIESTANY, SLOVAKIA INC.	
V	ON SEMI SBN II	SEREMBAN, MALAYSIA	
W	ON SEMI GDL	GUADALAJARA, MEXICO	
X	*ASE–METL	CHUNG–LI, TAIWAN	
ZK	ASE (K) OR ASE	KAOHSIUNG, TAIWAN	
ZQ	ANAM K2 (BUCHON)	BUCHON, KOREA	
ZR	AAP1 (FORMERLY: AAPI)	MANILA PHILIPPINES	or ”5” for SOIC 8 LD or smaller packages
ZS	MITSUI HI–TECH (MHT)	FUKUOKA–KUROSAKI, JAPAN	
ZV	AAP2 (FORMERLY: AME)	MANILA, PHILIPPINES	

NOTE: THE SINGLE DIGIT NUMBER ASSIGNED TO SOME SUBCONTRACTORS IS TO BE USED FOR MARKING PURPOSES ONLY, WHEN PACKAGE SIZE IS VERY SMALL.

* Indicates an addition or a change

One–Gate Logic Tape & Reel and Package Specifications

TAPE & REEL SPECIFICATIONS

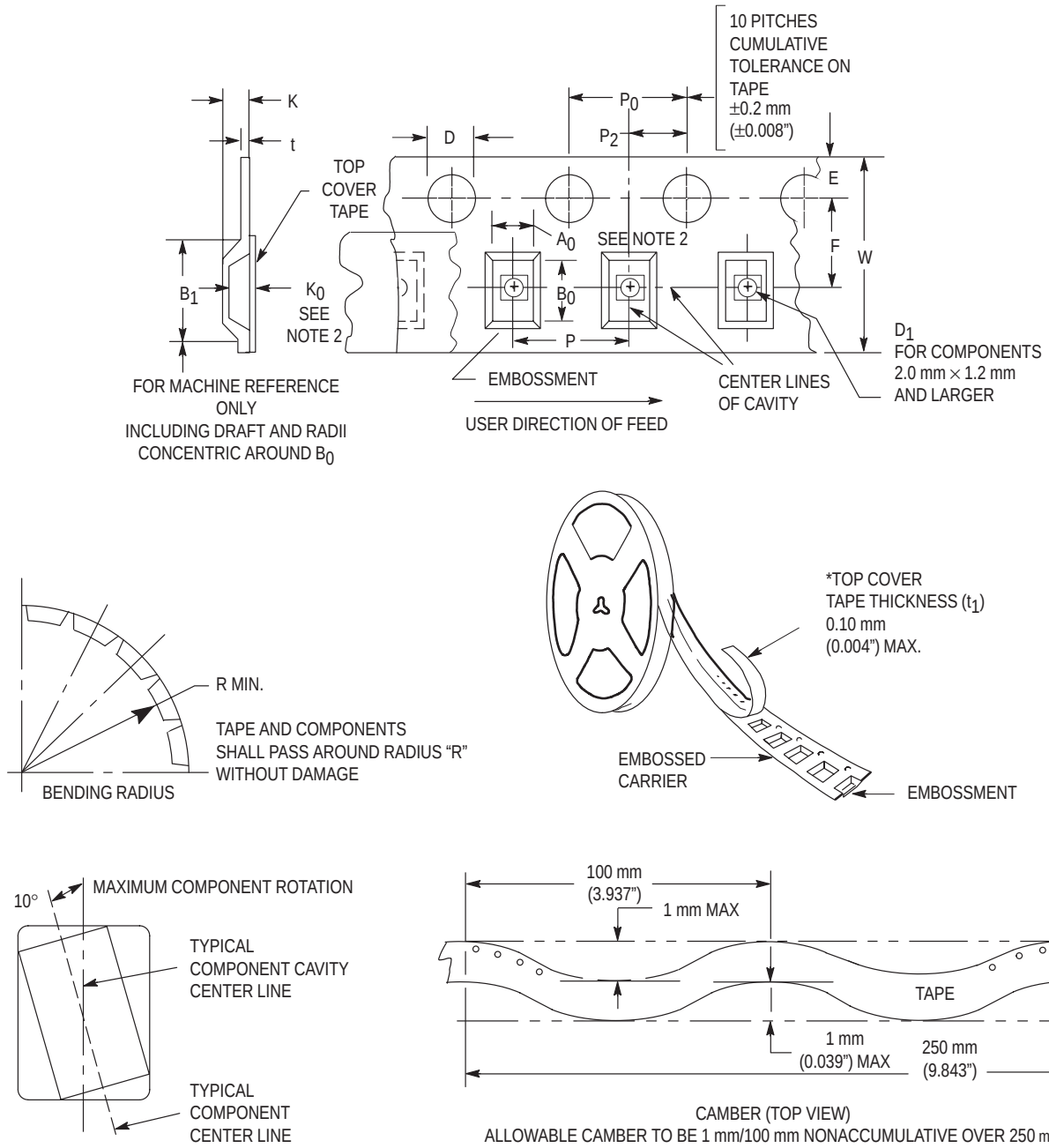


Figure 1. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ –0.0 mm (0.059 +0.004/ –0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ –0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

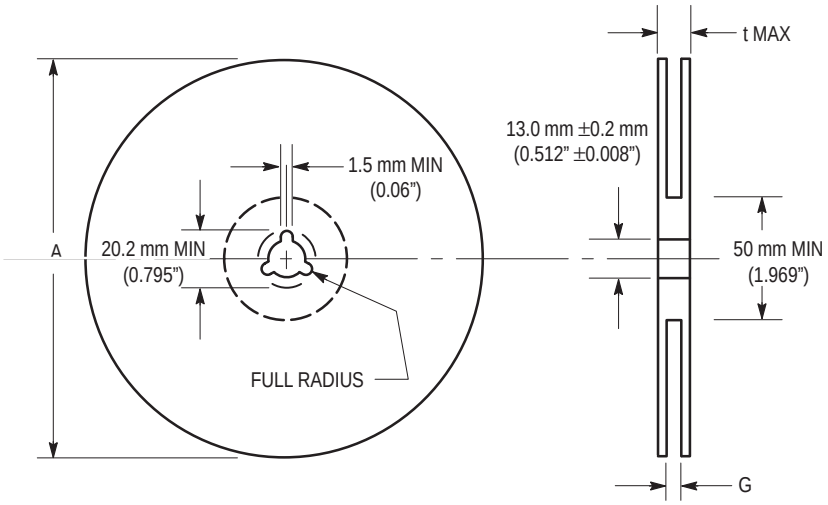


Figure 2. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
8 mm	330 mm (13")	8.400 mm, +1.5 mm, –0.0 (0.33", +0.059", –0.00)	14.4 mm (0.56")

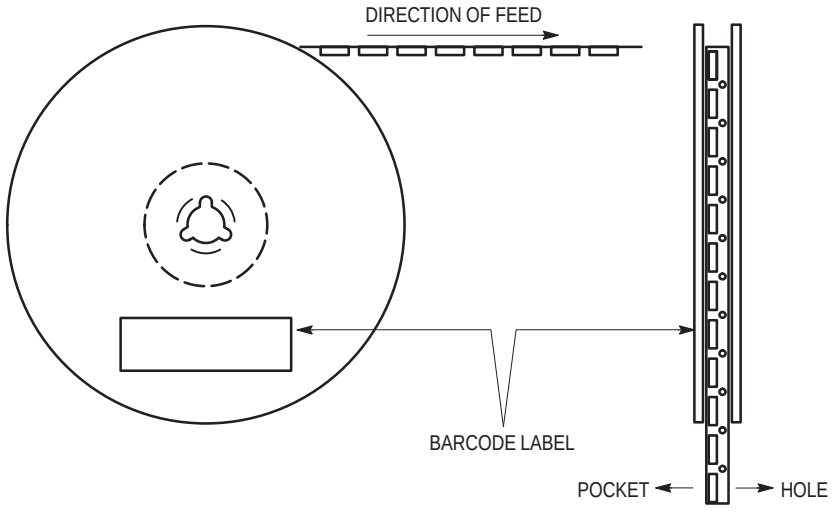


Figure 3. Reel Winding Direction

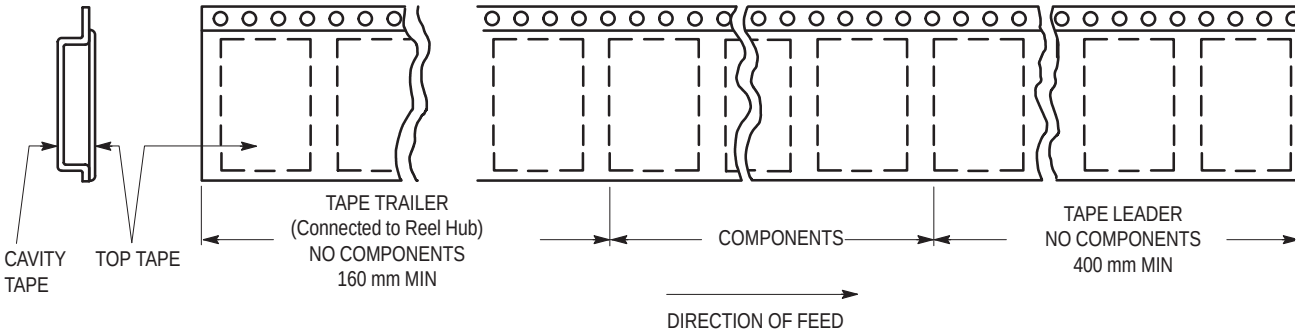


Figure 4. Tape Ends for Finished Goods

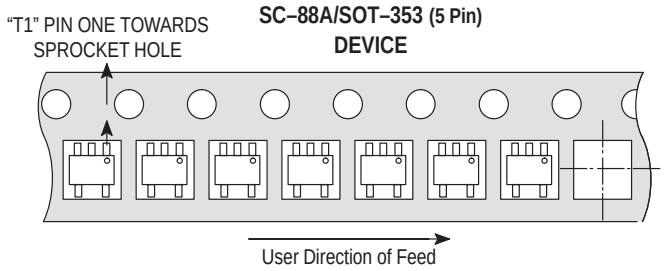
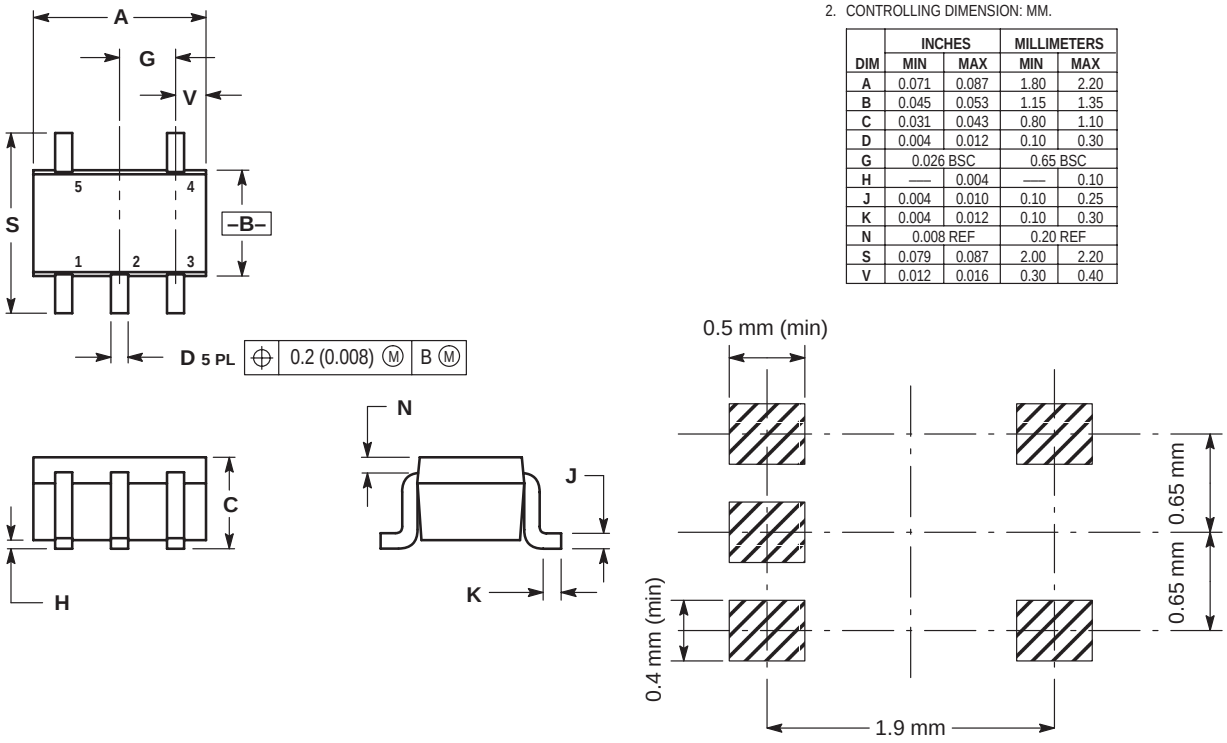


Figure 5. Reel Configuration

CASE OUTLINE AND PACKAGE DIMENSIONS

SC–88A / SOT–353
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

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