MOTOROLA

DL203/D
Rev 2

Very High-Speed CMOS Data

Formerly Titled "Advanced High-Speed CMOS Data"

DATA SHEET CLASSIFICATIONS

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: “This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.”

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Very High–Speed CMOS Data

Formerly Titled "Advanced High–Speed CMOS Data"

Printed in U.S.A.

Table of Contents

***** = Represents information that has not appeared in previous issues of this publication.

Italics represent documents that have been revised since the last issue of this publication.

An Introduction to VHC

Motorola's Very High-Speed CMOS Logic Family

The VHC (Very High–Speed CMOS) logic family is designed for operation from V_{CC} = 2V–5.5V. When operating at supply voltages less than the 5V range the VHC family features 5V–tolerant inputs to aid 3V–5V mixed system designs. Low power, low switching noise and fast switching speeds make this family perfect for low power, low cost portable applications.

The VHCT products offer TTL compatibility with CMOS low power performance. VHCT accepts TTL level inputs and delivers full swing (4.5V to 5.5V) outputs. The supply voltage range for VHCT is V_{CC} = 4.5V–5.5V.

The VHC/VHCT family pioneers a new "cost/performance" frontier. With typical speeds of less than 10ns, VHC/VHCT is the perfect logic family to take the low cost, low power designs well into the future. Excellent noise performance makes VHC/VHCT simple to use, with no need to sacrifice speed. VHC/VHCT can also improve system performance by drastically reducing static and dynamic power consumption which extends battery life for portable and handheld applications. Customers can also utilize VHC/VHCT to simplify system design in mixed voltage environments, as well as expedite development of low voltage systems. The 5V tolerant input capability helps simplify mixed system designs.

The Motorola VHC/VHCT family is available in industry standard JEDEC SOIC, EIAJ SOIC, and the popular TSSOP packages. VHC/VHCT temperature specifications range from –40°C to +85°C. The VHC/VHCT family is second sourced (specification compatible) by two other major semiconductor suppliers for ease of use and availability.

- Fastest propagation delays in their class — VHC244 T_{pd} = 8.5ns maximum compared to HC244A T_{pd} = 23ns max, and AC244 T_{pd} = 7.5ns max; at 4.5V, –40°C to +85°C operating temperature, 50pF loads
- VHC/VHCT also offers a "light load" 15pF specification for point–to–point applications
- Specified for 5V and 3V operation (VHC) — AC and DC tables ease design for either 3V or 5V systems
- Very low noise — guaranteed noise specifications (V_{olp}, V_{olv}, V_{ihd}, V_{ild})
- Inputs tolerate voltages from 0V to 7V — When the voltage on the input exceeds the supply voltage, no current path to the supply exists. Guaranteed not to exceed ±1μA. This feature facilitates 3V–5V interface. A 3V to 5V/5V to 3V level shifter can be easily designed by using a combination of VHC and VHCT product
- Low static ICC — 20μA maximum for gates, 40μA maximum for MSI and octals. Typical static current is in the tens of nanoamps
- Industry standard packaging — SOIC, EIAJ SOIC, TSSOP packages. The TSSOP package is footprint compatible with competitions SSOP type I package. The TSSOP package is thinner than the SSOP type I package
- 8mA sink/source current at V_{CC} = 4.5V; 4mA at V_{CC} = 3.0V (VHC) — Good drive capability
- Latch–up immunity >±300mA — Exceeds the industry standard
- ESD immunity > 2kV HBM; >200V MM — Reliable operation. Industry standard performance

Motorola plans to expand the VHC/VHCT family portfolio to around 80 popular functions. Customer input is always welcome.

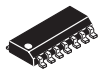
Quad 2-Input NAND Gate

MC74VHC00

The MC74VHC00 is an advanced high speed CMOS 2–input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

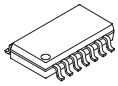
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 32 FETs or 8 Equivalent Gates



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

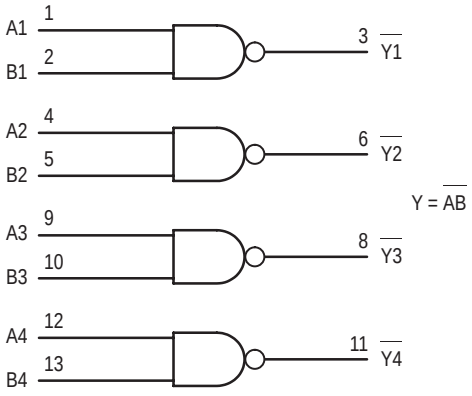


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

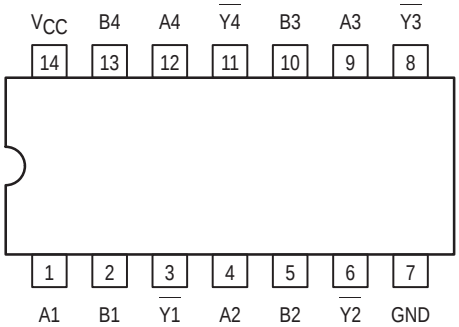
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	**B**	**$\overline{Y}$**
L	L	H
L	H	H
H	L	H
H	H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3V C_L = 15pF		5.5	7.9	1.0	9.5	ns
		V_{CC} = 3.3 ± 0.3V C_L = 50pF		8.0	11.4	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		3.7	5.5	1.0	6.5	
		V_{CC} = 5.0 ± 0.5V C_L = 50pF		5.2	7.5	1.0	8.5	
C_{in}	Input Capacitance			4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	19	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC} / 4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V, Measured in SOIC Package)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

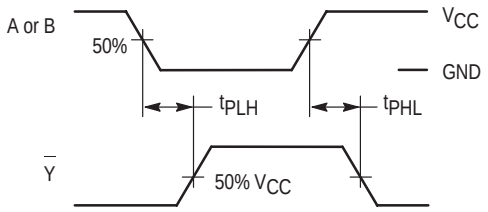
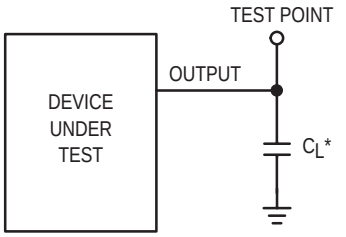


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

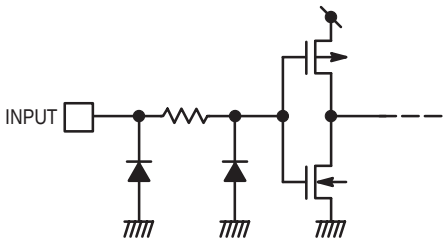


Figure 3. Input Equivalent Circuit

Quad 2-Input NAND Gate

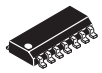
MC74VHCT00A

The MC74VHCT00A is an advanced high speed CMOS 2–input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

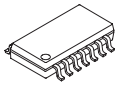
The VHCT00A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 5.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 48 FETs or 12 Equivalent Gates



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

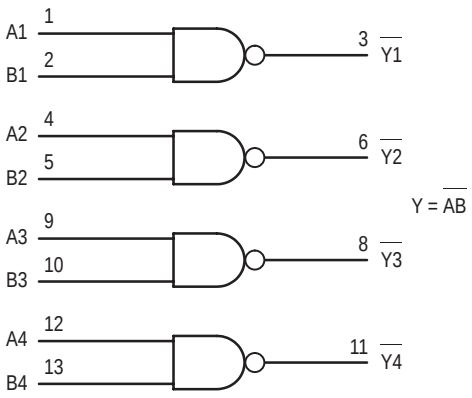


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCTXXAD	SOIC
MC74VHCTXXADT	TSSOP
MC74VHCTXXAM	SOIC EIAJ

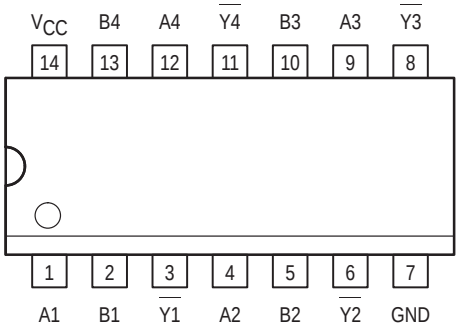
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	**B**	**$\overline{Y}$**
L	L	H
L	H	H
H	L	H
H	H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50µA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50µA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	µA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, A or B to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		5.0	6.9	1.0	8.0	ns
		$C_L = 50pF$		5.5	7.9	1.0	9.0	
C_{in}	Input Capacitance			4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 1.)	17	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0V$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.4	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

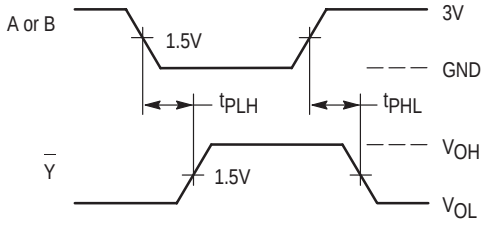
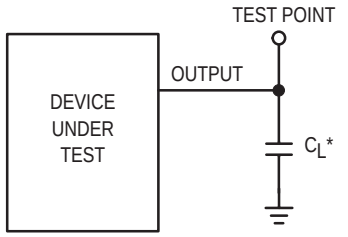


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

Quad 2-Input NOR Gate

MC74VHC02

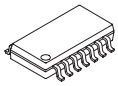
The MC74VHC02 is an advanced high speed CMOS 2–input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.6ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 40 FETs or 10 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

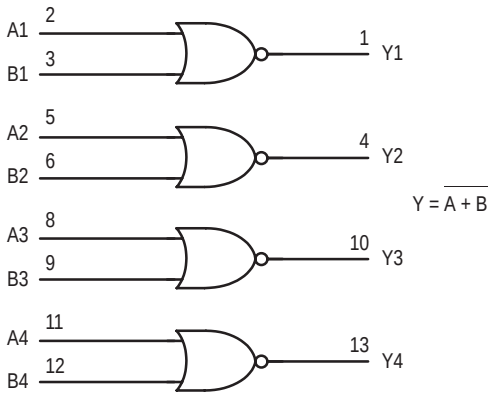


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

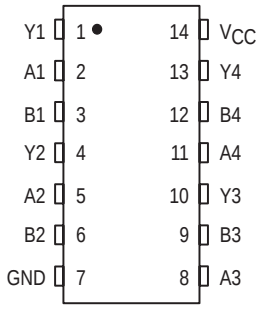
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

PIN ASSIGNMENT



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y	V_{CC} = 3.3 ± 0.3V C_L = 15pF		5.6	7.9	1.0	9.5	ns
		C_L = 50pF		8.1	11.4	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		3.6	5.5	1.0	6.5	
		C_L = 50pF		5.1	7.5	1.0	8.5	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	15	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

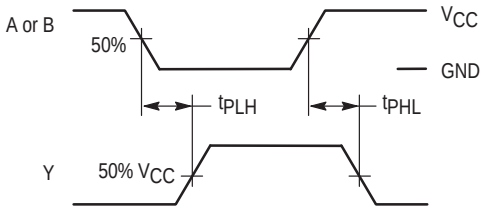
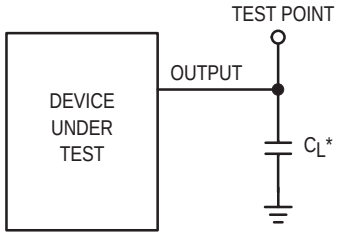


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

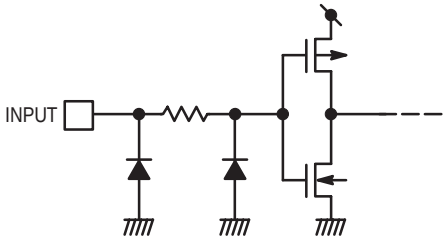


Figure 3. Input Equivalent Circuit

Hex Inverter

MC74VHC04

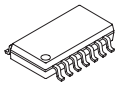
The MC74VHC04 is an advanced high speed CMOS inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2µA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 36 FETs or 9 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

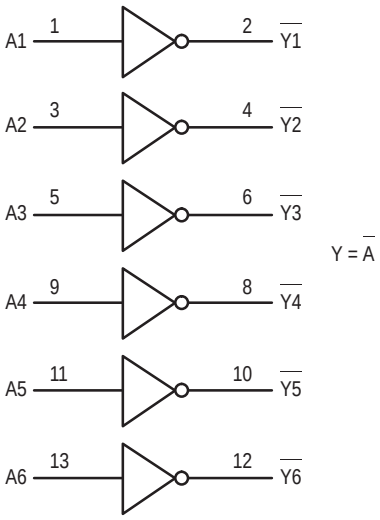


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

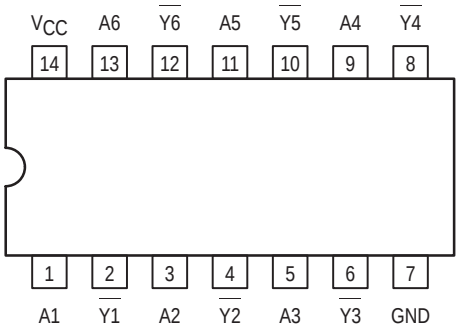
LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to + 7.0	V
V_{in}	DC Input Voltage	–0.5 to + 7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		–40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} = 5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = –40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = –4mA I_{OH} = –8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = –40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 or GND	0 to 5.5			± 0.1		± 0.1	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = –40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3V C_L = 15pF		5.0	7.1	1.0	8.5	ns
		C_L = 50pF		7.5	10.6	1.0	12.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		3.8	5.5	1.0	6.5	
		C_L = 50pF		5.3	7.5	1.0	8.5	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Per Inverter) (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.4	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

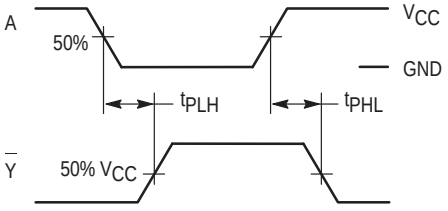
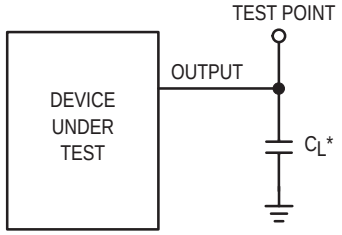


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

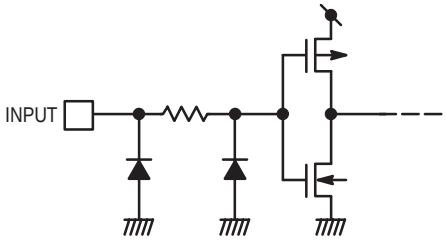


Figure 3. Input Equivalent Circuit

Hex Inverter
(Unbuffered)

MC74VHCU04

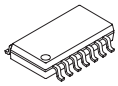
The MC74VHCU04 is an advanced high speed CMOS unbuffered inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2µA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 10% V_{CC} (Min.)
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 12 FETs or 3 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

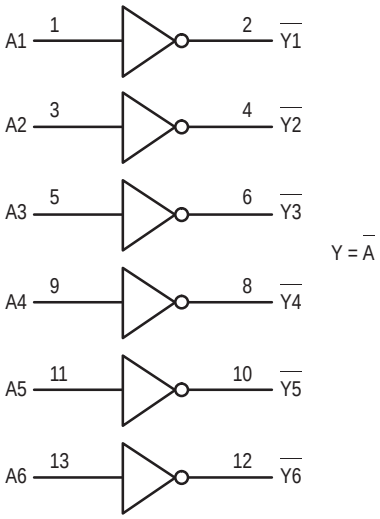


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCUXXD	SOIC
MC74VHCUXXDT	TSSOP
MC74VHCUXXM	SOIC EIAJ

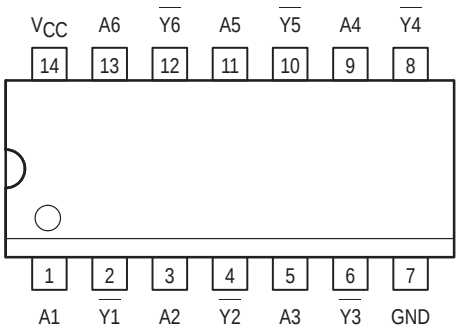
LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to + 7.0	V
V_{in}	DC Input Voltage	–0.5 to + 7.0	V
V_{out}	DC Output Voltage	–0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	–20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	–40	+ 85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = –40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.70 V_{CC} x 0.8			1.70 V_{CC} x 0.8		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.30 V_{CC} x 0.2		0.30 V_{CC} x 0.2	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} =V_{IL} I_{OH} = –50μA	2.0 3.0 4.5	1.8 2.7 4.0	2.0 3.0 4.5		1.8 2.7 4.0		V
		V_{in} = GND I_{OH} = –4mA I_{OH} = –8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.2 0.3 0.5		0.2 0.3 0.5	V
		V_{in} = V_{CC} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = –40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = –40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3V C_L = 15pF		5.0	8.9	1.0	10.5	ns
		V_{CC} = 3.3 ± 0.3V C_L = 50pF		7.5	11.4	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		3.5	5.5	1.0	6.5	
		V_{CC} = 5.0 ± 0.5V C_L = 50pF		5.0	7.0	1.0	8.0	
C_{in}	Maximum Input Capacitance			5	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Per Inverter) (Note 1.)	9	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		4.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.0	V

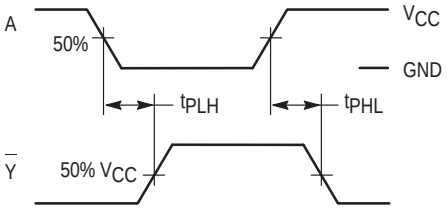
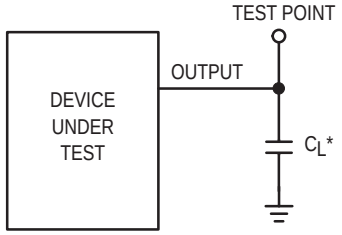


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

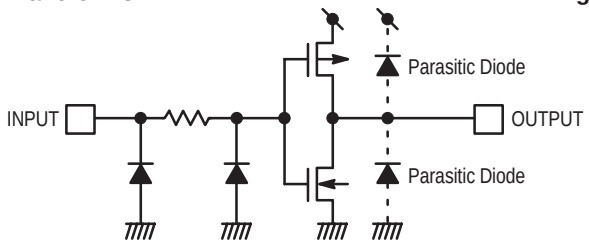


Figure 3. Input Equivalent Circuit

Hex Inverter

MC74VHCT04A

The MC74VHCT04A is an advanced high speed CMOS inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

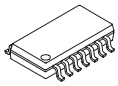
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT04A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 4.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.0V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 48 FETs or 12 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

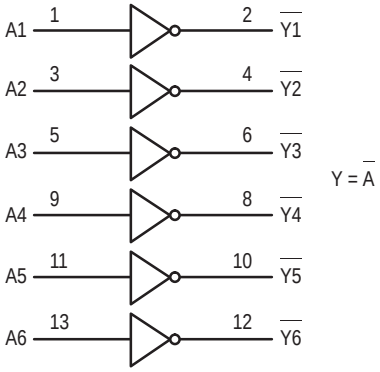


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCTXXAD	SOIC
MC74VHCTXXADT	TSSOP
MC74VHCTXXAM	SOIC EIAJ

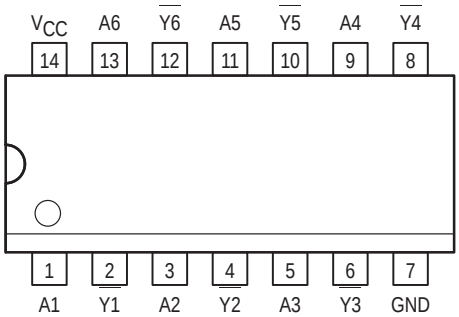
LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		4.7	6.7	1.0	7.5	ns
		$C_L = 50pF$		5.5	7.7	1.0	8.5	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 1.)	11	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50pF$, $V_{CC} = 5.0V$)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.8	–1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

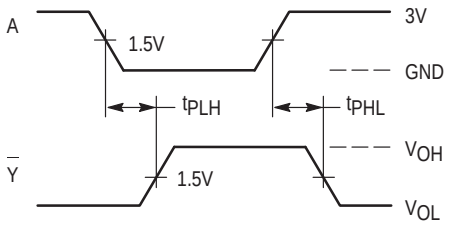
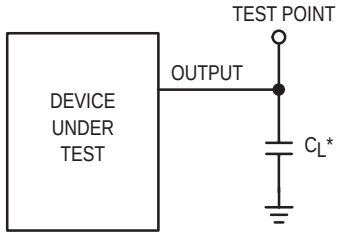


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

Quad 2-Input AND Gate

MC74VHC08

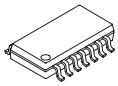
The MC74VHC08 is an advanced high speed CMOS 2–input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.3ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 24 FETs or 6 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

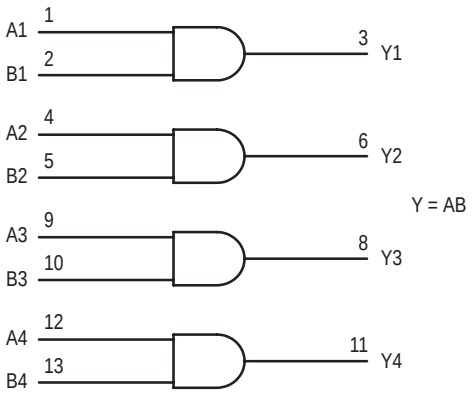


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

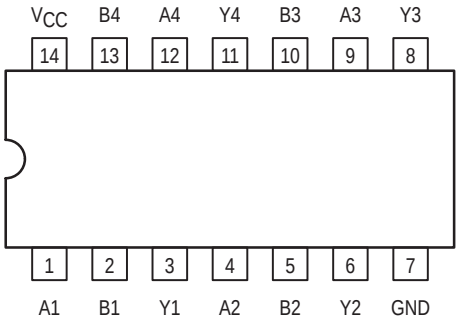
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} = 5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3V C_L = 15pF		6.2	8.8	1.0	10.5	ns
		V_{CC} = 3.3 ± 0.3V C_L = 50pF		8.7	12.3	1.0	14.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		4.3	5.9	1.0	7.0	
		V_{CC} = 5.0 ± 0.5V C_L = 50pF		5.8	7.9	1.0	9.0	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns, C_L = 50pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

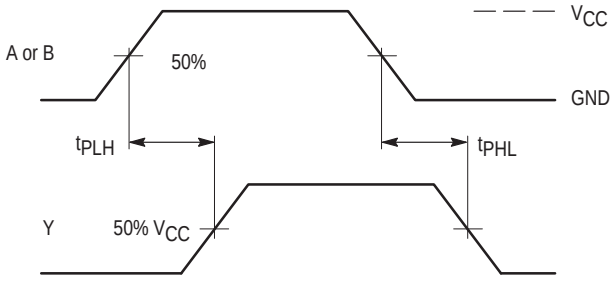
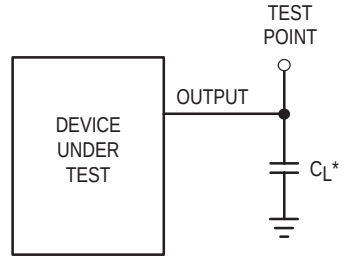


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

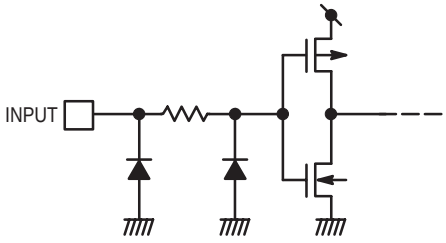


Figure 3. Input Equivalent Circuit

Hex Schmitt Inverter

MC74VHC14

The MC74VHC14 is an advanced high speed CMOS Schmitt inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

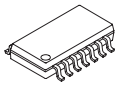
Pin configuration and function are the same as the MC74VHC04, but the inputs have hysteresis and, with its Schmitt trigger function, the VHC14 can be used as a line receiver which will receive slow input signals.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 5.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 60 FETs or 15 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

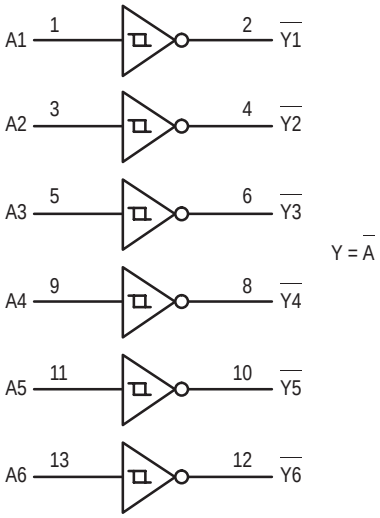


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

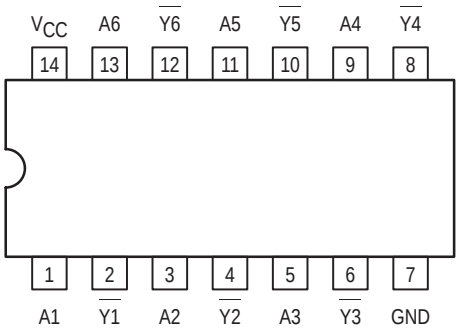
LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{T+}	Positive Threshold Voltage (Figure 3)		3.0 4.5 5.5			2.20 3.15 3.85		2.20 3.15 3.85	V
$V_{T–}$	Negative Threshold Voltage (Figure 3)		3.0 4.5 6.0	0.9 1.35 1.65			0.90 1.35 1.65		V
V_H	Hysteresis Voltage (Figure 3)		3.0 4.5 5.5	0.30 0.40 0.50		1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF		8.3	12.8	1.0	15.0	ns
			C_L = 50pF		10.8	16.3	1.0	18.5	
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF		5.5	8.6	1.0	10.0	
			C_L = 50pF		7.0	10.6	1.0	12.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	21	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.4	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

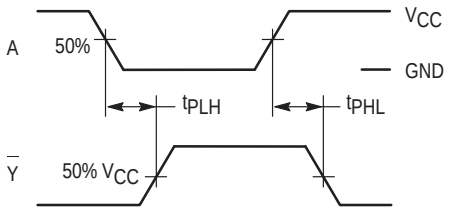
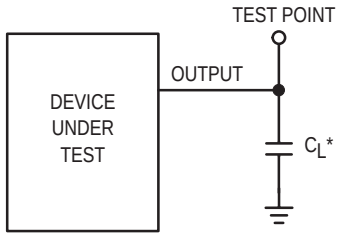


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

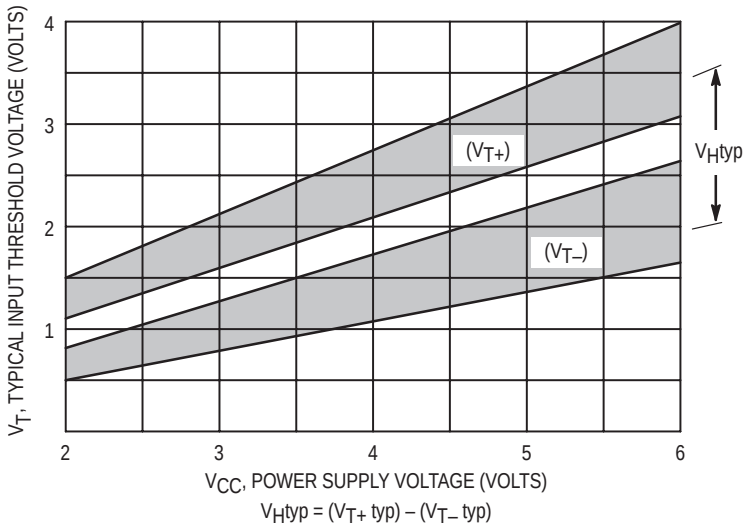


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

(a) A Schmitt–Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt–Trigger Offers Maximum Noise Immunity

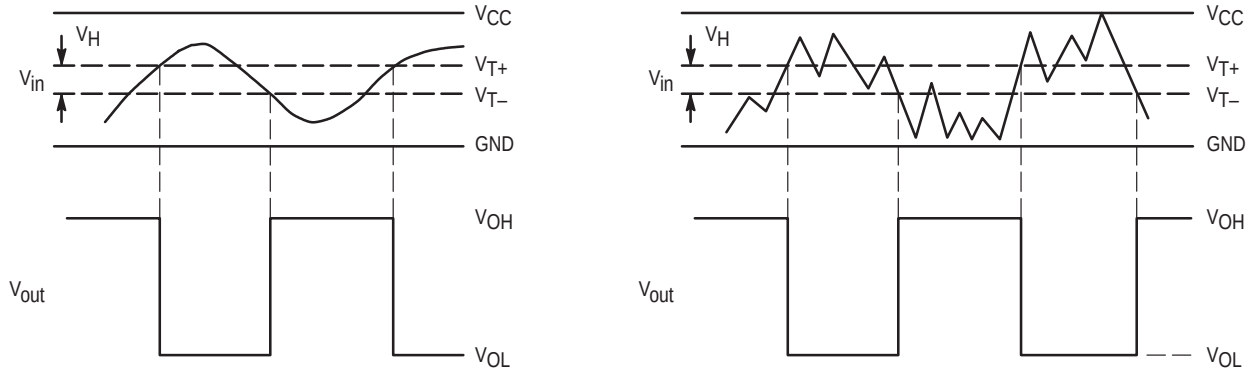


Figure 4. Typical Schmitt–Trigger Applications

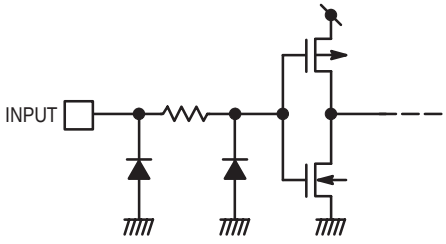


Figure 5. Input Equivalent Circuit

Quad 2-Input OR Gate

MC74VHC32

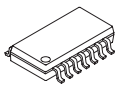
The MC74VHC32 is an advanced high speed CMOS 2–input OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 48 FETs or 12 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

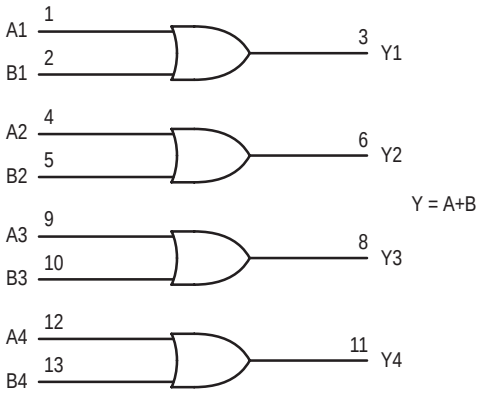


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

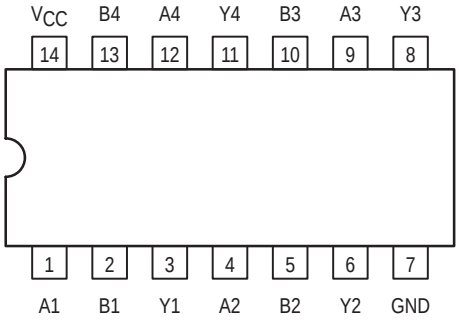
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V	0	100	ns/V
		V_{CC} =5.0V ±0.5V	0	20	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3V C_L = 15pF		5.5	7.9	1.0	9.5	ns
		C_L = 50pF		8.0	11.4	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		3.8	5.5	1.0	6.5	
		C_L = 50pF		5.3	7.5	1.0	8.5	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	14	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

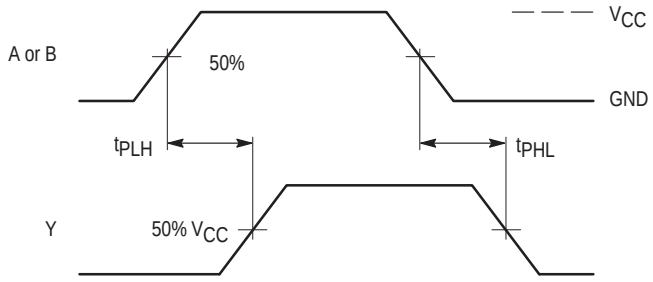
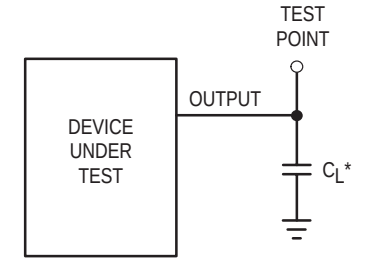


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

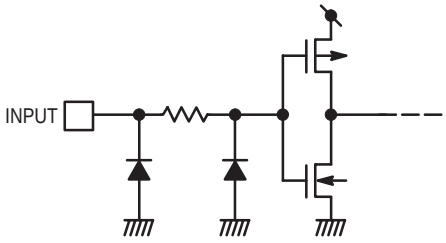


Figure 3. Input Equivalent Circuit

Dual D-Type Flip-Flop with Set and Reset

MC74VHC74

The MC74VHC74 is an advanced high speed CMOS D–type flip–flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

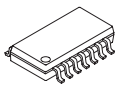
Reset (RD) and Set (SD) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: f_{max} = 170MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 128 FETs or 32 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

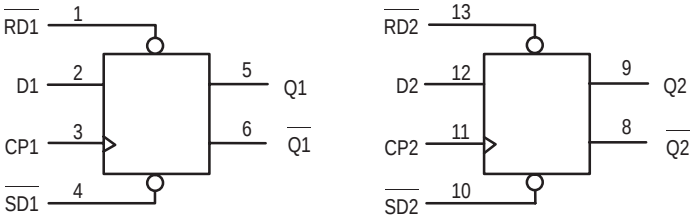


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

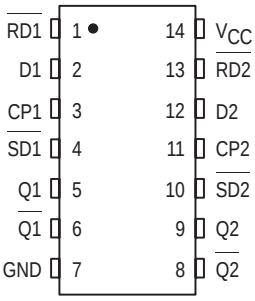
ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q or Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		6.7 9.2	11.9 15.4	1.0 1.0	14.0 17.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.6 6.1	7.3 9.3	1.0 1.0	8.5 10.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SD or RD to Q or Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		7.6 10.1	12.3 15.8	1.0 1.0	14.5 18.0	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.8 6.3	7.7 9.7	1.0 1.0	9.0 11.0	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF	80 50	125 75		70 45		MHz
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF	130 90	170 115		110 75		
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	25	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit		Unit
			T_A = 25°C	T_A = – 40 to 85°C	
t_w	Minimum Pulse Width, CP	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_w	Minimum Pulse Width, RD or SD	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_{su}	Minimum Setup Time, D to CP	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_h	Minimum Hold Time, D to CP	3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	ns
t_{rec}	Minimum Recovery Time, SD or RD to CP	3.3 ± 0.3 5.0 ± 0.5	5.0 3.0	5.0 3.0	ns

SWITCHING WAVEFORMS

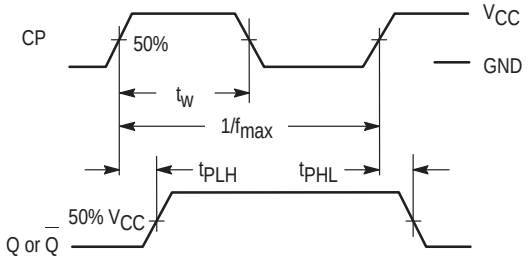


Figure 1.

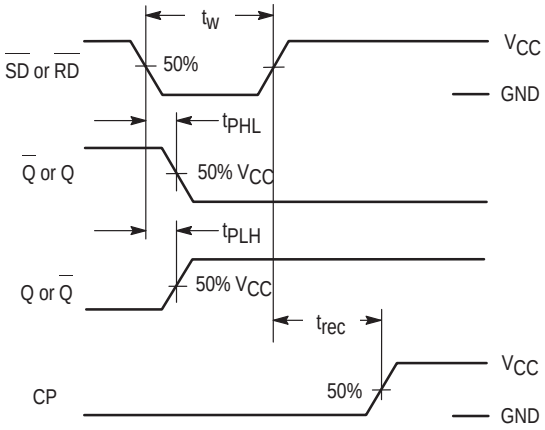


Figure 2.

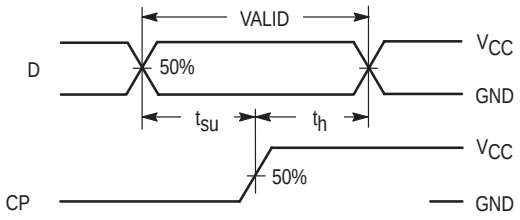
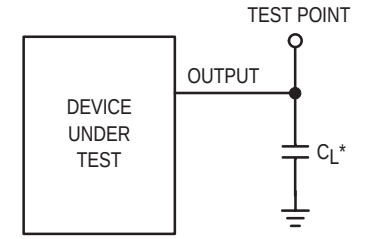


Figure 3.



* Includes all probe and jig capacitance

Figure 4.

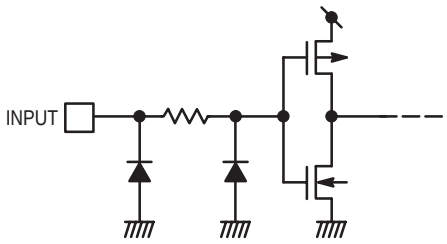


Figure 5. Input Equivalent Circuit

Dual D-Type Flip-Flop with Set and Reset

MC74VHCT74A

The MC74VHCT74A is an advanced high speed CMOS D–type flip–flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset (RD) and Set (SD) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

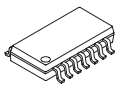
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT74A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when VCC=0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: f_{max} = 60MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 128 FETs or 32 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

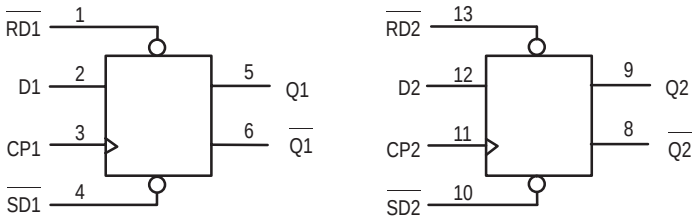


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

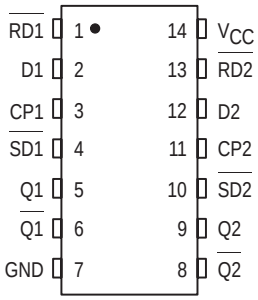
ORDERING INFORMATION

MC74VHCTXXAD	SOIC
MC74VHCTXXADT	TSSOP
MC74VHCTXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50µA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50µA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	µA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q or Q	$V_{CC} = 5.0 \pm 0.5$V $C_L = 15$pF $C_L = 50$pF		5.8 6.3	7.8 8.8	1.0 1.0	9.0 10.0	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SD or RD to Q or Q	$V_{CC} = 5.0 \pm 0.5$V $C_L = 15$pF $C_L = 50$pF		7.6 8.1	10.4 11.4	1.0 1.0	12.0 13.0	ns
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 \pm 0.5$V $C_L = 15$pF $C_L = 50$pF	100 80	160 140		80 65		MHz
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	24	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit $T_A = 25°C$	Guaranteed Limit $T_A = -40$ to $85°C$	Unit
t_w	Minimum Pulse Width, CP	5.0 ± 0.5	5.0	5.0	ns
t_w	Minimum Pulse Width, RD or SD	5.0 ± 0.5	5.0	5.0	ns
t_{su}	Minimum Setup Time, D to CP	5.0 ± 0.5	5.0	5.0	ns
t_h	Minimum Hold Time, D to CP	5.0 ± 0.5	0.0	0.0	ns
t_{rec}	Minimum Recovery Time, SD or RD to CP	5.0 ± 0.5	3.5	3.5	ns

SWITCHING WAVEFORMS

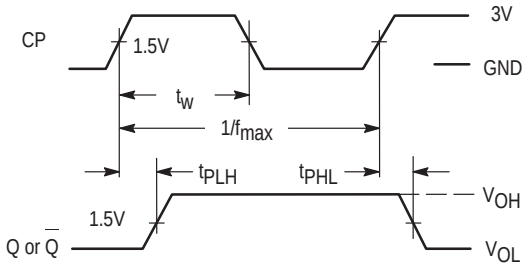


Figure 1.

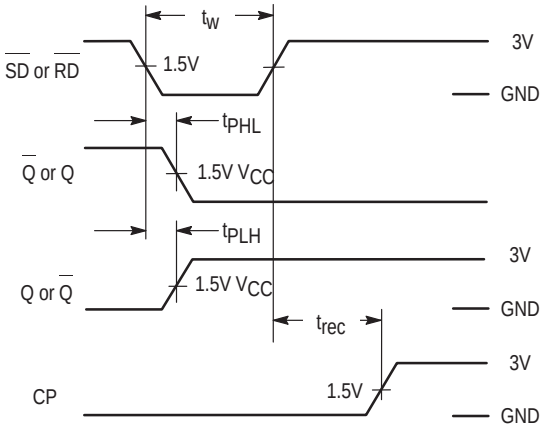


Figure 2.

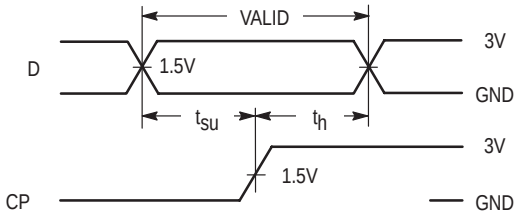
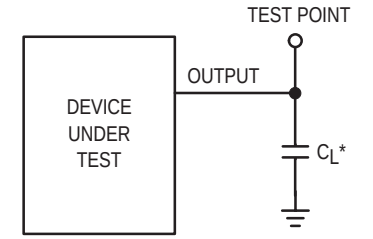


Figure 3.



* Includes all probe and jig capacitance

Figure 4.

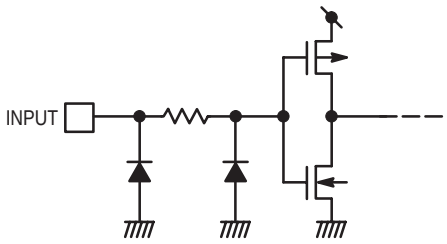


Figure 5. Input Equivalent Circuit

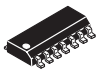
Quad 2-Input XOR Gate

MC74VHC86

The MC74VHC86 is an advanced high speed CMOS 2–input Exclusive–OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

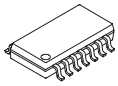
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 56 FETs or 14 Equivalent Gates



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

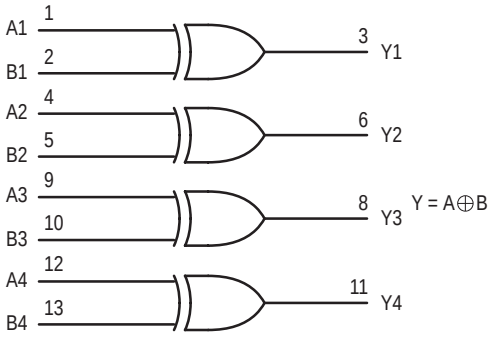


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

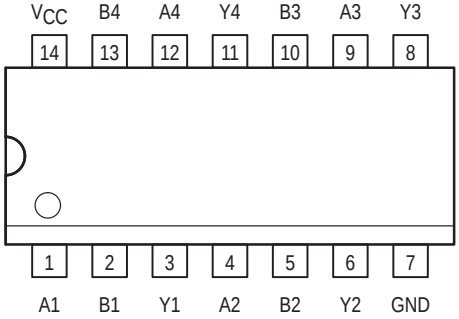
LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

Pinout: 14–Lead Packages (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, A or B to Y	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 15pF$		7.0	11.0	1.0	13.0	ns
		$C_L = 50pF$		9.5	14.5	1.0	16.5	
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		4.8	6.8	1.0	8.0	
		$C_L = 50pF$		6.3	8.8	1.0	10.0	
C_{in}	Input Capacitance			4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0V$, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

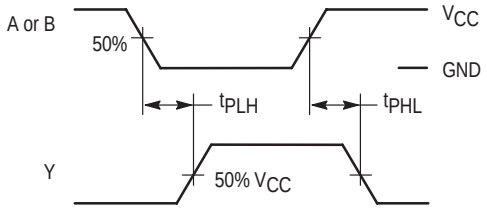
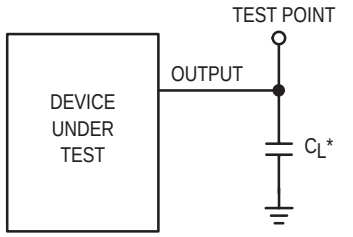


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

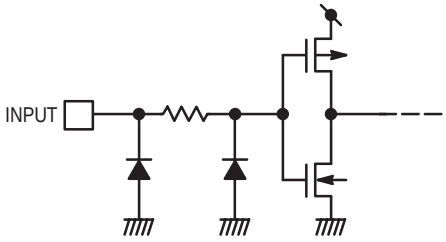


Figure 3. Input Equivalent Circuit

Quad Bus Buffer
with 3-State Control Inputs

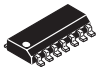
MC74VHC125

The MC74VHC125 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC125 requires the 3–state control input ($\overline{OE}$) to be set High to place the output into the high impedance state.

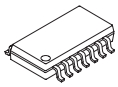
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 72 FETs or 18 Equivalent Gates



D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



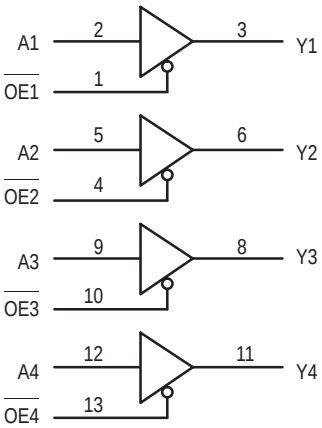
M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

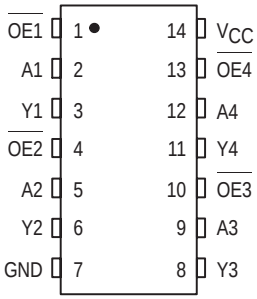
MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

LOGIC DIAGRAM

Active–Low Output Enables



PIN ASSIGNMENT



FUNCTION TABLE

VHC125		
Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IH} or V_{IL} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.50	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.6	8.0	1.0	9.5	ns
			C_L = 50pF		8.1	11.5	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		3.8	5.5	1.0	6.5	
			C_L = 50pF		5.3	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	Maximum Output Enable TIme, OE to Y	V_{CC} = 3.3 ± 0.3V, R_L = 1kΩ	C_L = 15pF		5.4	8.0	1.0	9.5	ns
			C_L = 50pF		7.9	11.5	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V, R_L = 1kΩ	C_L = 15pF		3.6	5.1	1.0	6.0	
			C_L = 50pF		5.1	7.1	1.0	8.0	
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time, OE to Y	V_{CC} = 3.3 ± 0.3V, R_L = 1kΩ	C_L = 50pF		9.5	13.2	1.0	15.0	ns
		V_{CC} = 5.0 ± 0.5V, R_L = 1kΩ	C_L = 50pF		6.1	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output–to–Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	14	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

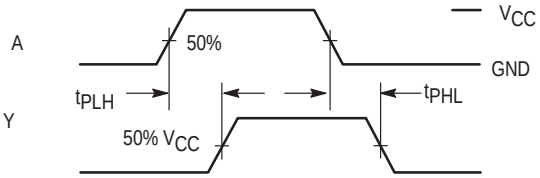


Figure 1.

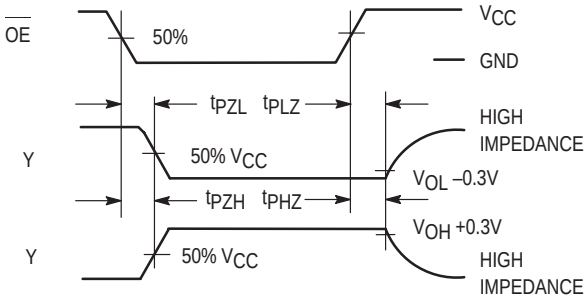
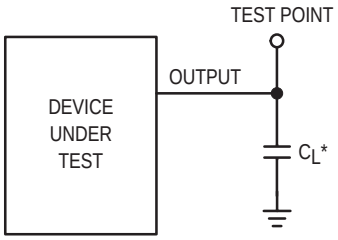
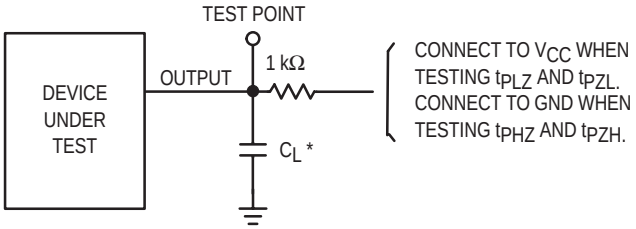


Figure 2.



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

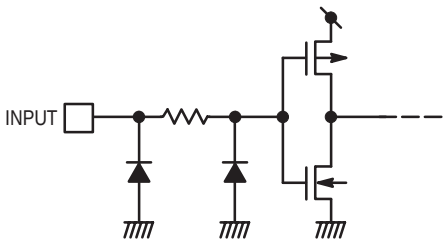


Figure 5. Input Equivalent Circuit

Quad Bus Buffer
with 3-State Control Inputs

MC74VHC126

The MC74VHC126 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves noninverting high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

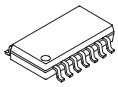
The MC74VHC126 requires the 3–state control input (OE) to be set Low to place the output into high impedance.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 72 FETs or 18 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01



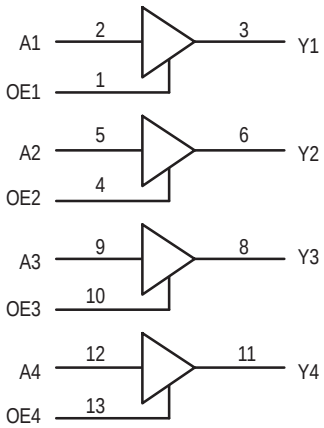
M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

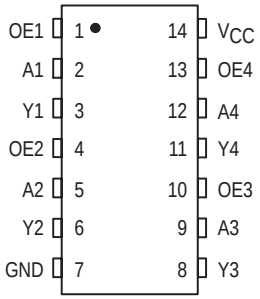
MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

LOGIC DIAGRAM

Active–High Output Enables



PIN ASSIGNMENT



FUNCTION TABLE

VHC126		
Inputs		Output
A	OE	Y
H	H	H
L	H	L
X	L	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IH} or V_{IL} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.50	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.6	8.0	1.0	9.5	ns
			C_L = 50pF		8.1	11.5	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		3.8	5.5	1.0	6.5	
			C_L = 50pF		5.3	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	Maximum Output Enable TIme, OE to Y	V_{CC} = 3.3 ± 0.3V, R_L = 1kΩ	C_L = 15pF		5.4	8.0	1.0	9.5	ns
			C_L = 50pF		7.9	11.5	1.0	13.0	
		V_{CC} = 5.0 ± 0.5V, R_L = 1kΩ	C_L = 15pF		3.6	5.1	1.0	6.0	
			C_L = 50pF		5.1	7.1	1.0	8.0	
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time, OE to Y	V_{CC} = 3.3 ± 0.3V, R_L = 1kΩ	C_L = 50pF		9.5	13.2	1.0	15.0	ns
		V_{CC} = 5.0 ± 0.5V, R_L = 1kΩ	C_L = 50pF		6.1	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output–to–Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	15	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

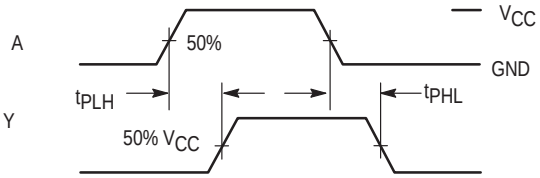


Figure 1.

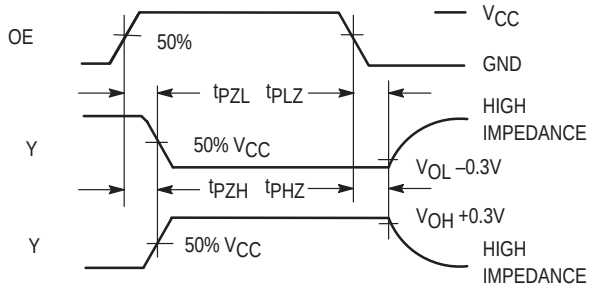
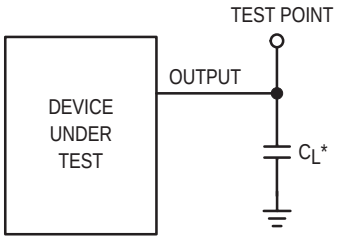
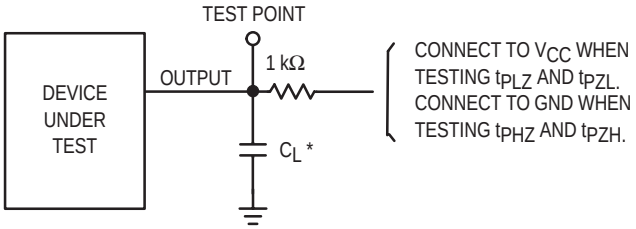


Figure 2.



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

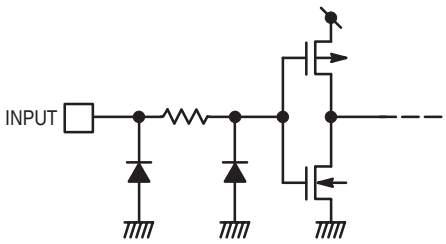


Figure 5. Input Equivalent Circuit

Quad 2-Input NAND Schmitt Trigger

MC74VHC132

The MC74VHC132 is an advanced high speed CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

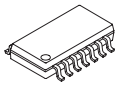
Pin configuration and function are the same as the MC74VHC00, but the inputs have hysteresis and, with its Schmitt trigger function, the VHC132 can be used as a line receiver which will receive slow input signals.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.9ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2µA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 72 FETs or 18 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

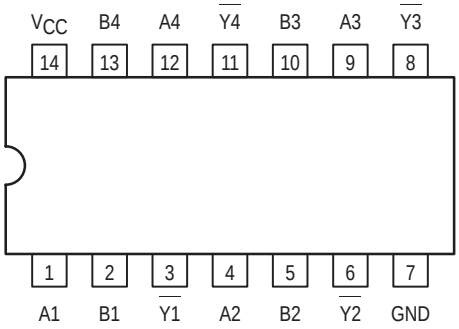


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

ORDERING INFORMATION

MC74VHCXXD	SOIC
MC74VHCXXDT	TSSOP
MC74VHCXXM	SOIC EIAJ

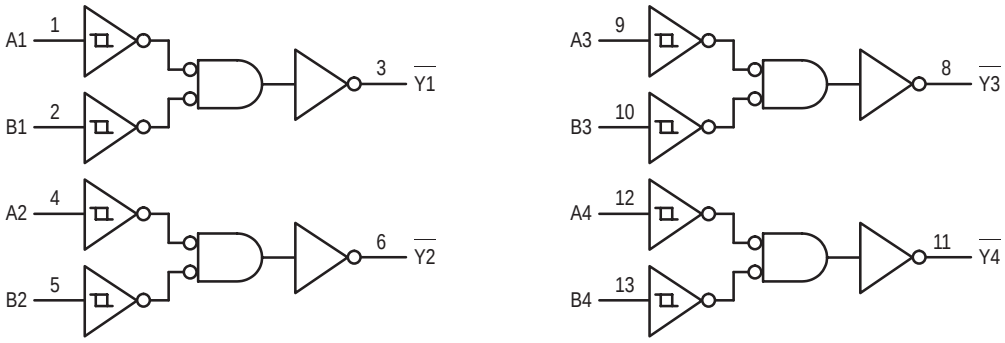
Pinout: 14–Lead Packages (Top View)



FUNCTION TABLE

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{T+}	Positive Threshold Voltage (Figure 3)		3.0 4.5 5.5			2.20 3.15 3.85		2.20 3.15 3.85	V
$V_{T–}$	Negative Threshold Voltage (Figure 3)		3.0 4.5 5.5	0.9 1.35 1.65			0.90 1.35 1.65		V
V_H	Hysteresis Voltage (Figure 3)		3.0 4.5 5.5	0.30 0.40 0.50		1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF		7.6	11.9	1.0	14.0	ns
			C_L = 50pF		10.1	15.4	1.0	17.5	
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF		4.9	7.7	1.0	9.0	
			C_L = 50pF		6.4	9.7	1.0	11.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	16	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

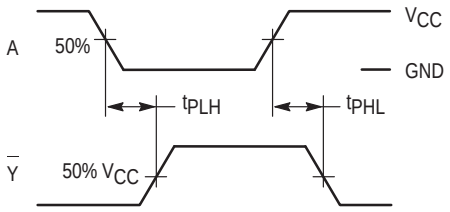
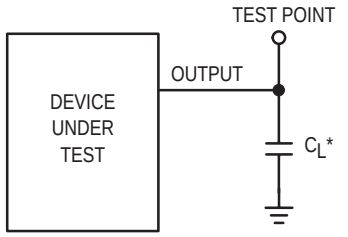


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

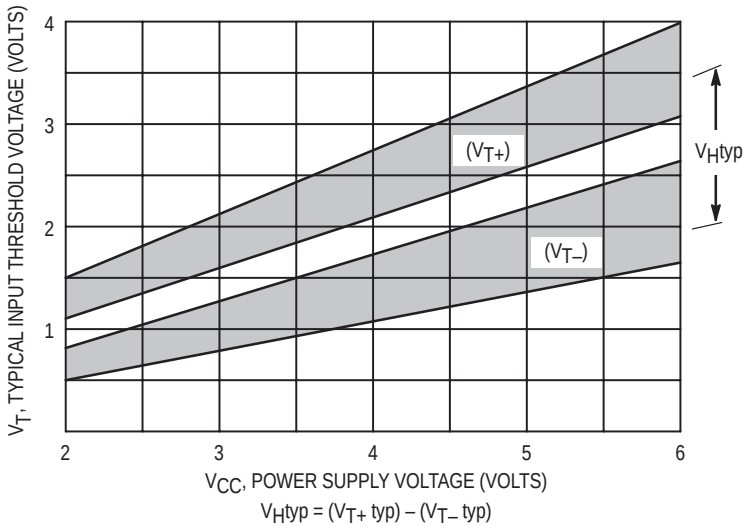


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

(a) A Schmitt–Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt–Trigger Offers Maximum Noise Immunity

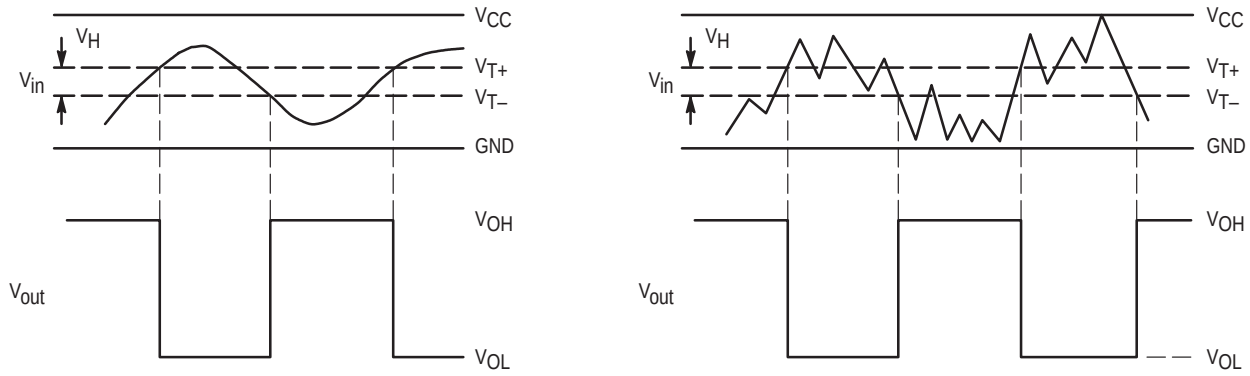


Figure 4. Typical Schmitt–Trigger Applications

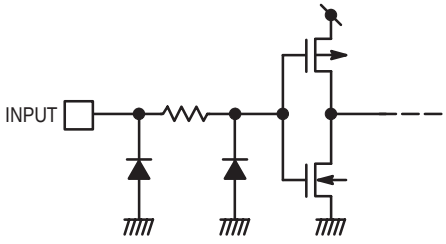


Figure 5. Input Equivalent Circuit

3-to-8 Line Decoder

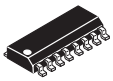
MC74VHC138

The MC74VHC138 is an advanced high speed CMOS 3–to–8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs (Y0 – Y7) will go Low. When enable input E3 is held Low or either E2 or E1 is held High, decoding function is inhibited and all outputs go high. E3, E2, and E1 inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

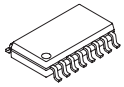
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 5.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

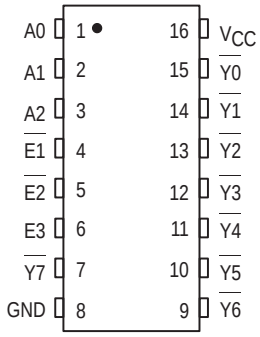


M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

ORDERING INFORMATION

MC74VHCXXXD	SOIC
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

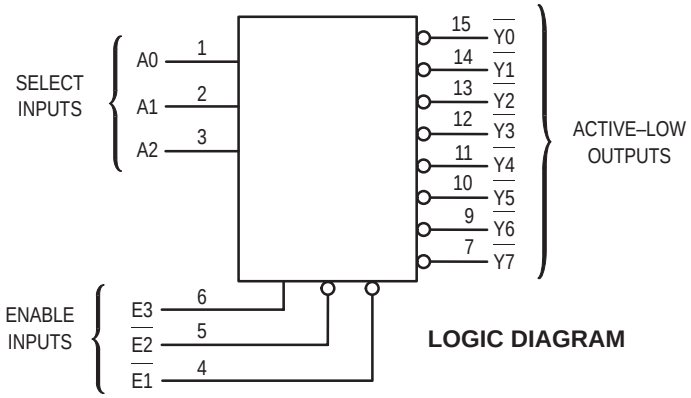
PIN ASSIGNMENT



FUNCTION TABLE

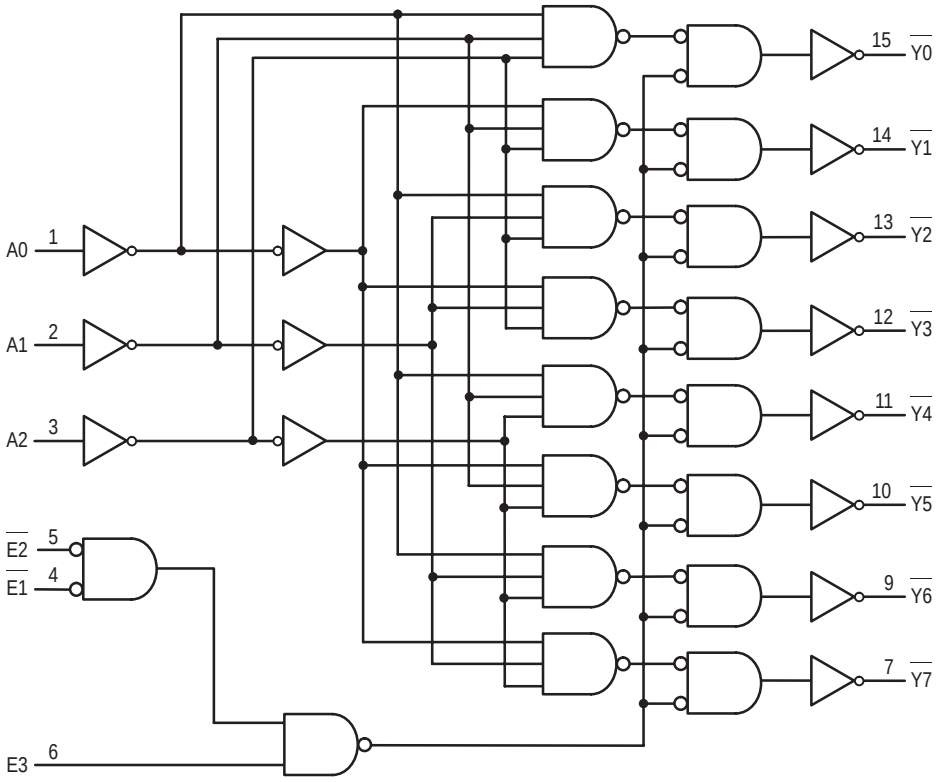
Inputs						Outputs							
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state); L = low level (steady state);
X = don't care



LOGIC DIAGRAM

EXPANDED LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		8.2	11.4	1.0	13.5	ns
			C_L = 50pF		10.0	15.8	1.0	18.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		5.7	8.1	1.0	9.5	
			C_L = 50pF		7.2	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E3 to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		8.1	12.8	1.0	15.0	ns
			C_L = 50pF		10.6	16.3	1.0	18.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		5.6	8.1	1.0	9.5	
			C_L = 50pF		7.1	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E2 or E1 to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		8.2	11.4	1.0	13.5	ns
			C_L = 50pF		10.7	14.9	1.0	17.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		5.8	8.1	1.0	9.5	
			C_L = 50pF		7.3	10.1	1.0	11.5	
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	34	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

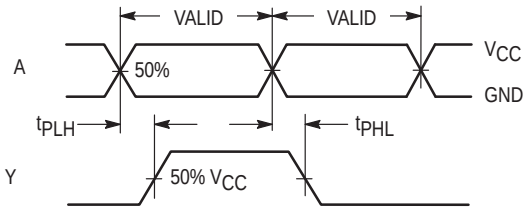


Figure 1.

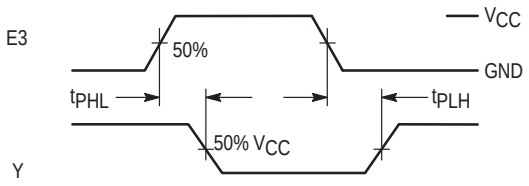


Figure 2.

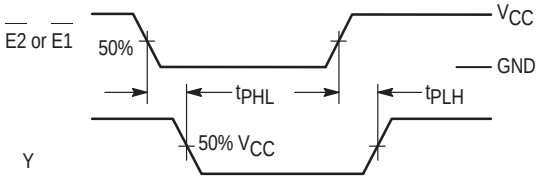
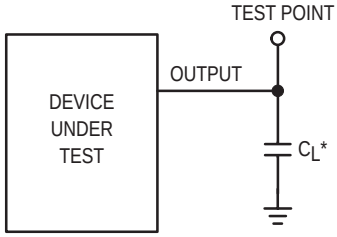


Figure 3.



* Includes all probe and jig capacitance

Figure 4. Test Circuit

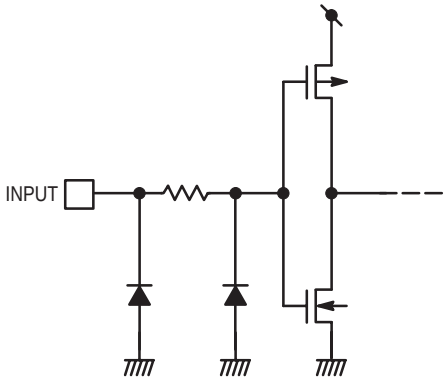


Figure 5. Input Equivalent Circuit

3-to-8 Line Decoder

MC74VHCT138A

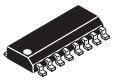
The MC74VHCT138A is an advanced high speed CMOS 3–to–8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs (Y0 – Y7) will go Low. When enable input E3 is held Low or either E2 or E1 is held High, decoding function is inhibited and all outputs go high. E3, E2, and E1 inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because they have full 5V CMOS level output swings.

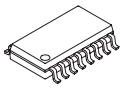
The VHCT138A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: t_{PD} = 7.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

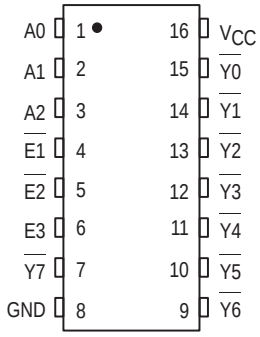


M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

ORDERING INFORMATION

MC74VHCTXXXAD	SOIC
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

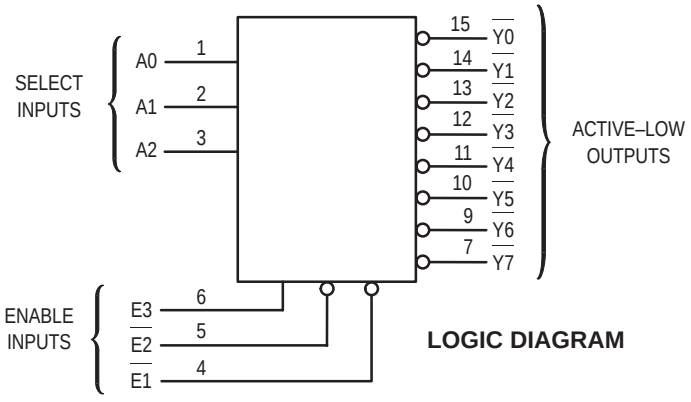
PIN ASSIGNMENT



FUNCTION TABLE

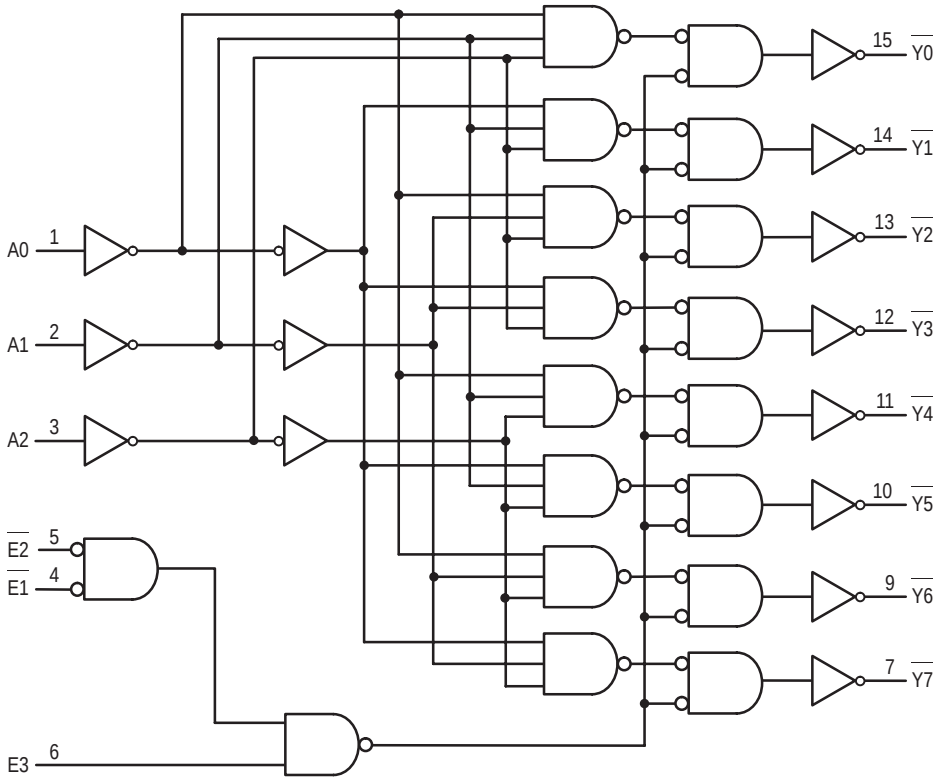
Inputs						Outputs							
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state); L = low level (steady state); X = don't care



LOGIC DIAGRAM

EXPANDED LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage V_{CC} = 0 High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50µA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50µA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		20.0	µA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		7.6	10.4	1.0	12.0	ns
		$C_L = 50pF$		8.1	11.4	1.0	13.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E3 to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		6.6	9.1	1.0	10.5	ns
		$C_L = 50pF$		7.1	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E2 or E1 to Y	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		7.0	9.6	1.0	11.0	ns
		$C_L = 50pF$		7.5	10.6	1.0	12.0	
C_{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 1.)	49	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

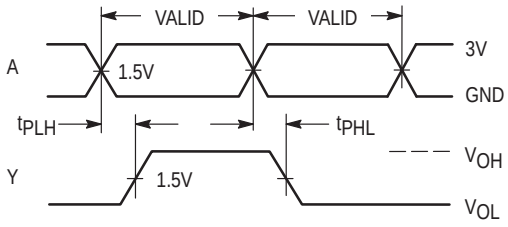


Figure 1.

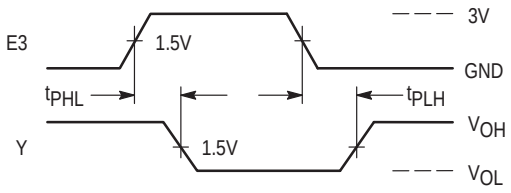


Figure 2.

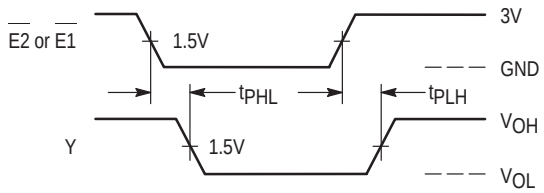
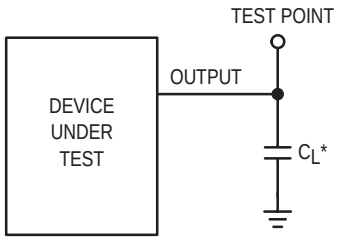


Figure 3.

TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Dual 2-to-4 Decoder/ Demultiplexer

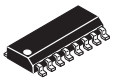
MC74VHC139

The MC74VHC139 is an advanced high speed CMOS 2–to–4 decoder/ demultiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled ($\overline{E}$ = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

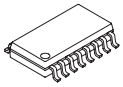
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 5.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 100 FETs or 25 Equivalent Gates



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

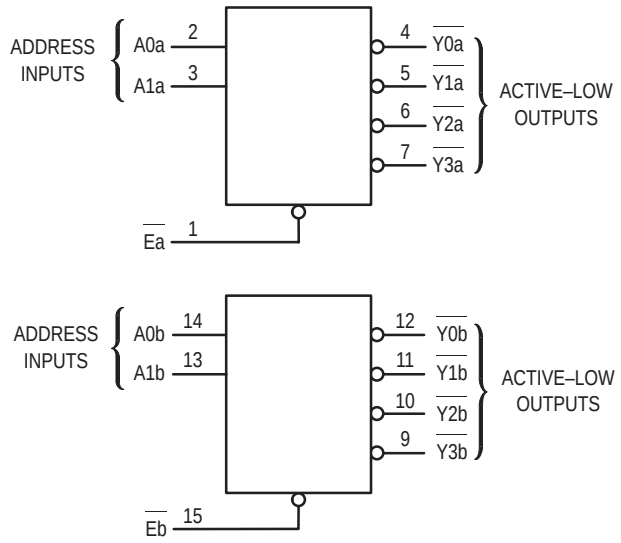


M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

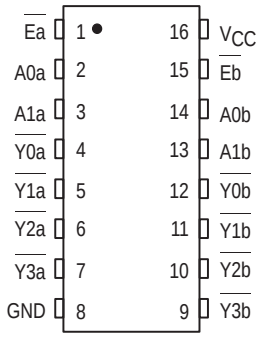
ORDERING INFORMATION

MC74VHCXXXD	SOIC
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



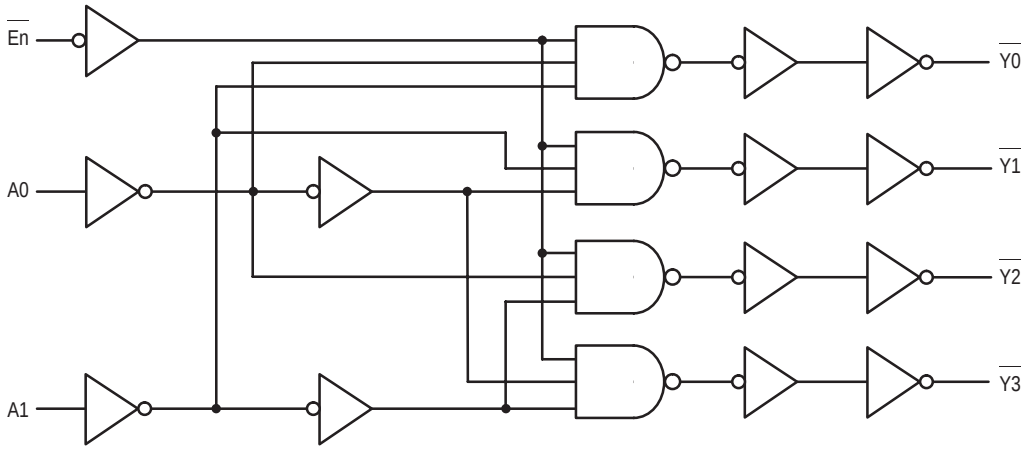
PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs			
E	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

EXPANDED LOGIC DIAGRAM
(1/2 OF DEVICE)



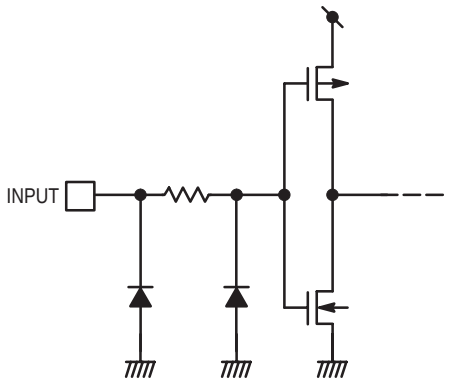


Figure 1. Input Equivalent Circuit

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.2	11.0	1.0	13.0	ns
			C_L = 50pF		9.7	14.5	1.0	16.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		5.0	7.2	1.0	8.5	
			C_L = 50pF		6.5	9.2	1.0	10.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		6.4	9.2	1.0	11.0	ns
			C_L = 50pF		8.9	12.7	1.0	14.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		4.4	6.3	1.0	7.5	
			C_L = 50pF		5.9	8.3	1.0	9.5	
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	26	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per decoder). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

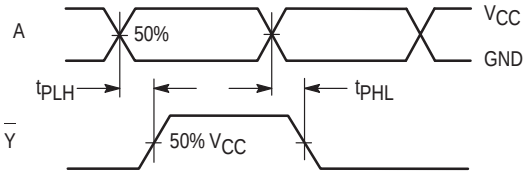


Figure 2.

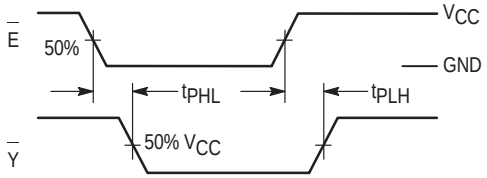
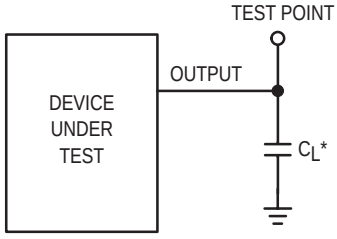


Figure 3.



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Quad 2-Channel Multiplexer

MC74VHC157

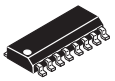
The MC74VHC157 is an advanced high speed CMOS quad 2–channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2–input digital multiplexers with common select (S) and enable (E) inputs. When E is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

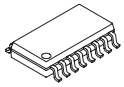
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 4.1ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 82 FETs or 20 Equivalent Gates



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

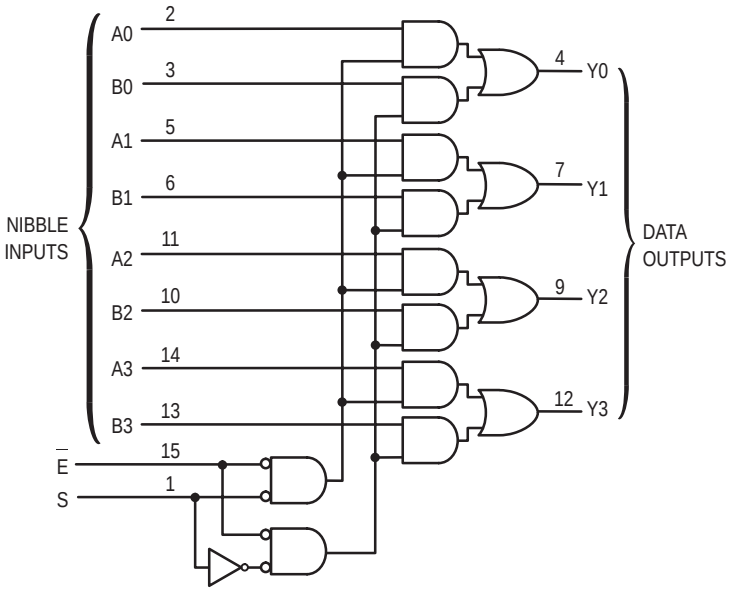


M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

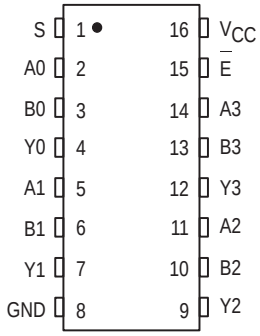
ORDERING INFORMATION

MC74VHCXXXD	SOIC
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

EXPANDED LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
E	**S**	**Y0 – Y3**
H	X	L
L	L	A0 – A3
L	H	B0 – B3

A0 – A3, B0 – B3 = the levels of the respective Data–Word Inputs.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V V_{CC} = 5.0V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		6.2 8.7	9.7 13.2	1.0 1.0	11.5 15.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		4.1 5.6	6.4 8.4	1.0 1.0	7.5 9.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, S to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		8.4 10.9	13.2 16.7	1.0 1.0	15.5 19.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		5.3 6.8	8.1 10.1	1.0 1.0	9.5 11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, E to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		8.7 11.2	13.6 17.1	1.0 1.0	16.0 19.5	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		5.6 7.1	8.6 10.6	1.0 1.0	10.0 12.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	20	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

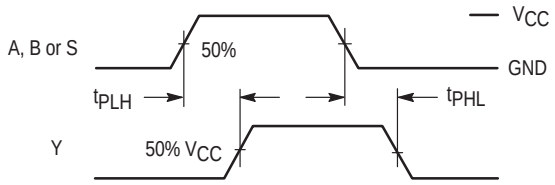


Figure 1. Switching Waveform

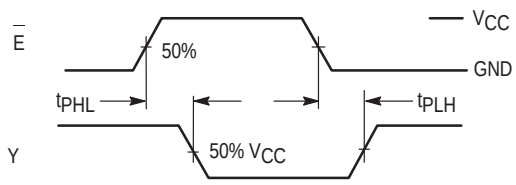
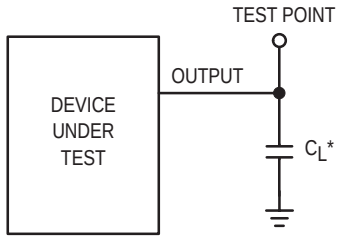


Figure 2. Inverting Switching



* Includes all probe and jig capacitance

Figure 3. Test Circuit

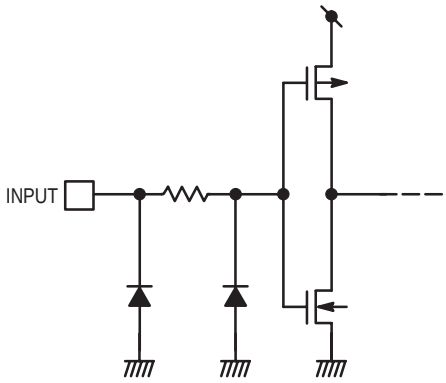


Figure 4. Input Equivalent Circuit

Octal Bus Buffer/Line Driver
Inverting with 3-State Outputs

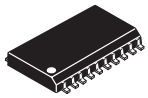
MC74VHC240

The MC74VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

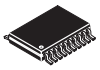
The MC74VHC240 is an inverting 3–state buffer, and has two active–low output enables. This device is designed to drive bus lines or buffer memory address registers.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

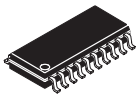
- High Speed: t_{PD} = 3.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.9V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 120 FETs or 30 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

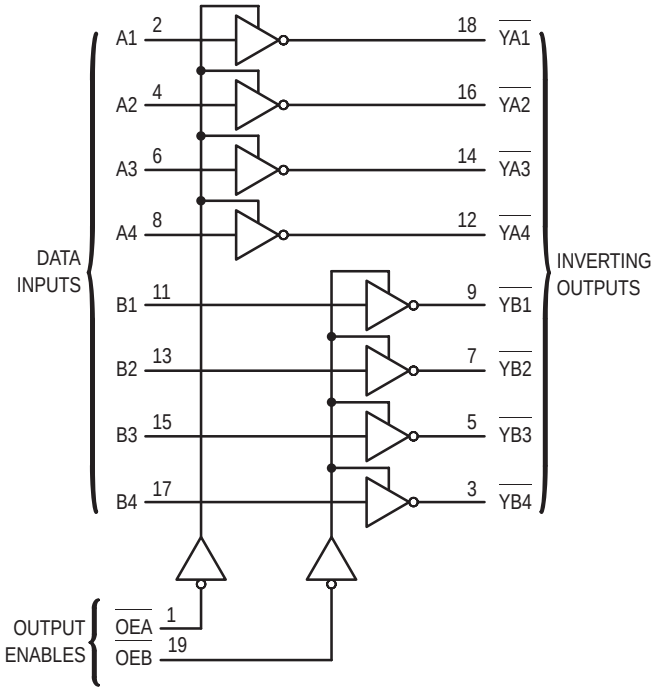


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

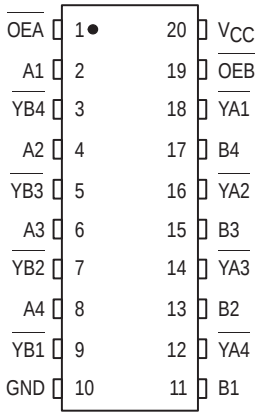
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}$, $\overline{OEB}$	A, B	$\overline{YA}$, $\overline{YB}$
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.3	7.5	1.0	9.0	ns
			C_L = 50pF		7.8	11.0	1.0	12.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		3.6	5.5	1.0	6.5	
			C_L = 50pF		5.1	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	Output Enable Time ___ OEA to YA or OEB to YB	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF		6.6	10.6	1.0	12.5	ns
			C_L = 50pF		9.1	14.1	1.0	16.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF		4.7	7.3	1.0	8.5	
			C_L = 50pF		6.2	9.3	1.0	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time ___ OEA to YA or OEB to YB	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		10.3	14.0	1.0	16.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.7	9.2	1.0	10.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	17	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.6	– 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

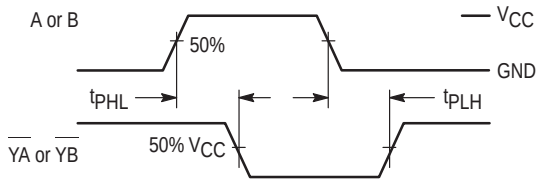


Figure 1.

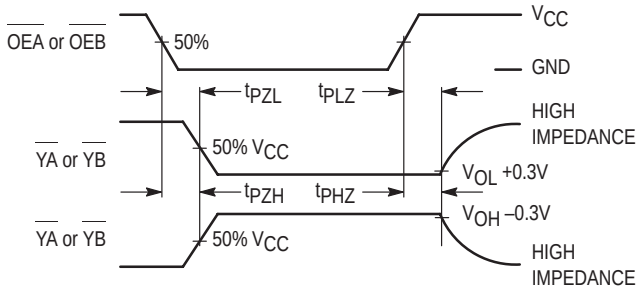
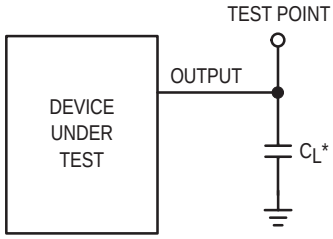


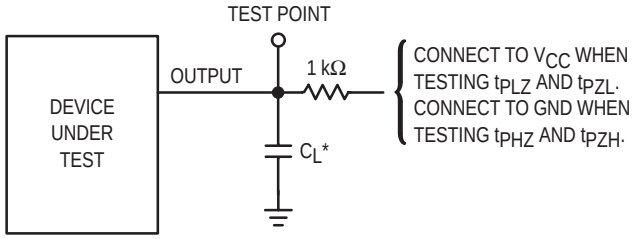
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

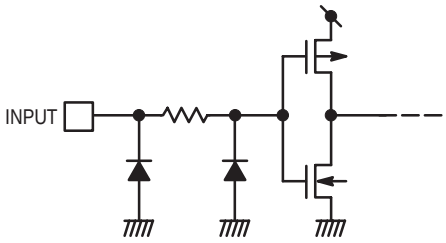


Figure 5. Input Equivalent Circuit

Octal Bus Buffer/Line Driver
Inverting with 3-State Outputs

MC74VHCT240A

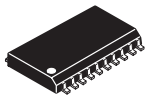
The MC74VHCT240A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT240A is an inverting 3–state buffer, and has two active–low output enables. This device is designed to be used with 3–state memory address drivers, etc.

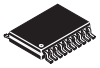
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT240A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

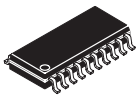
- High Speed: t_{PD} = 5.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.1V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

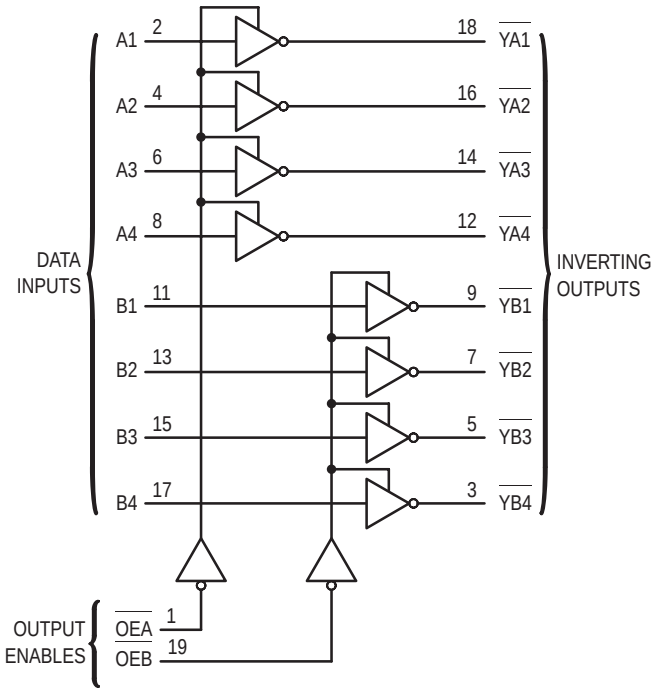


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

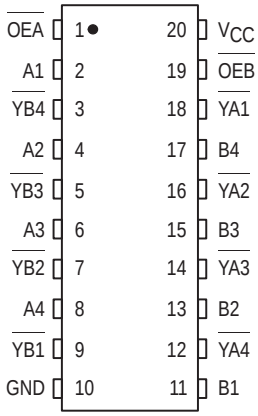
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}$, $\overline{OEB}$	A, B	$\overline{YA}$, $\overline{YB}$
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Output in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Output in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay A to YA or B to YB	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		5.6 6.1	7.8 8.8	1.0 1.0	9.0 10.0	ns
t_{PZL}, t_{PZH}	Output Enable Time OEA to YA or OEB to YB	V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		7.7 8.2	10.4 11.4	1.0 1.0	12.0 13.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time OEA to YA or OEB to YB	V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		8.8	11.4	1.0	13.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			9				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	19	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.1	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.1	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

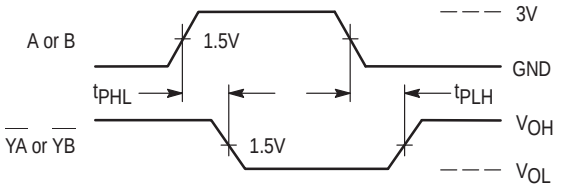


Figure 1.

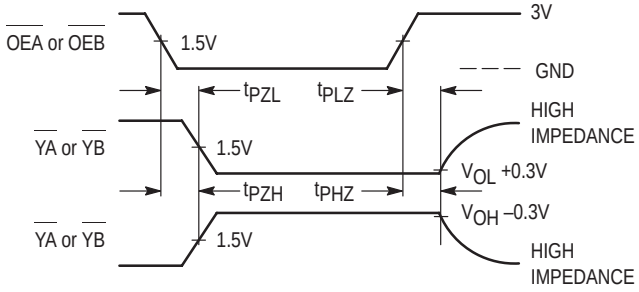
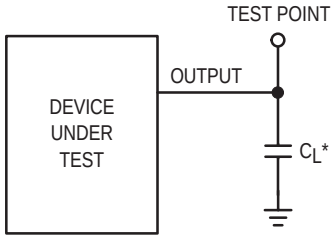


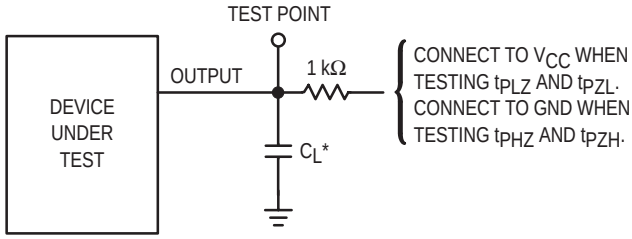
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

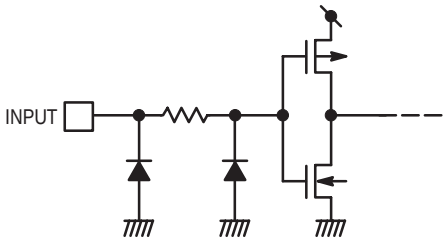


Figure 5. Input Equivalent Circuit

Octal Bus Buffer

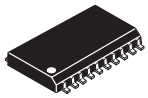
MC74VHC244

The MC74VHC244 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

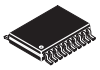
The MC74VHC244 is a noninverting 3–state buffer, and has two active–low output enables. This device is designed to be used with 3–state memory address drivers, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

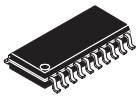
- High Speed: t_{PD} = 3.9ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.9V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 136 FETs or 34 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

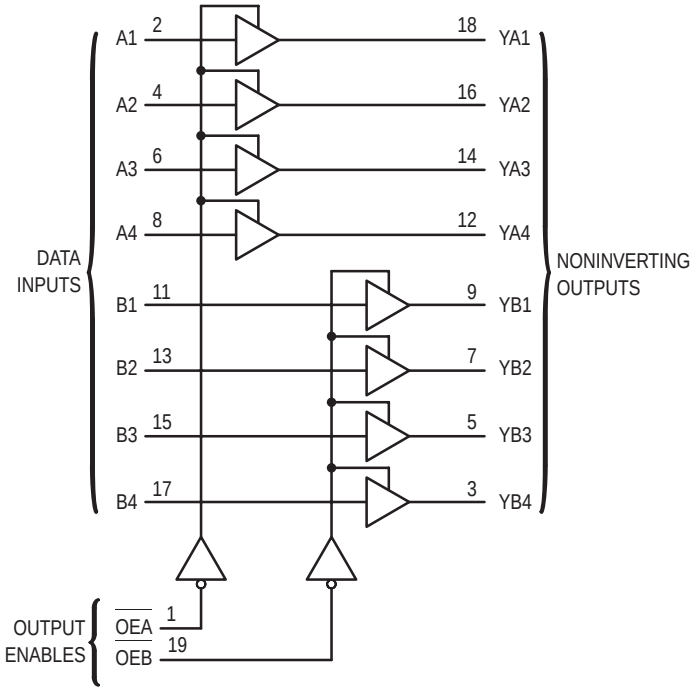


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

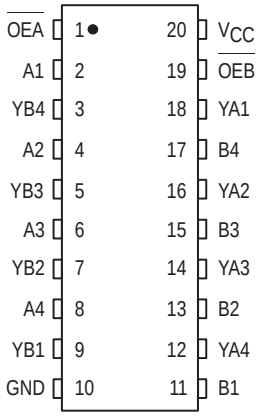
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}$, $\overline{OEB}$	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.8	8.4	1.0	10.0	ns
			C_L = 50pF		8.3	11.9	1.0	13.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		3.9	5.5	1.0	6.5	
			C_L = 50pF		5.4	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	Output Enable Time OEA to YA or OEB to YB	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF		6.6	10.6	1.0	12.5	ns
			C_L = 50pF		9.1	14.1	1.0	16.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF		4.7	7.3	1.0	8.5	
			C_L = 50pF		6.2	9.3	1.0	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time OEA to YA or OEB to YB	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		10.3	14.0	1.0	16.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.7	9.2	1.0	10.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	19	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.6	– 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

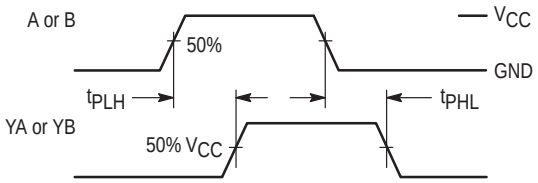


Figure 1.

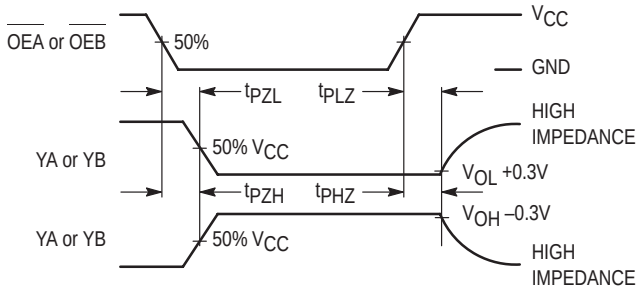
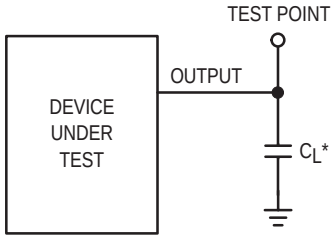


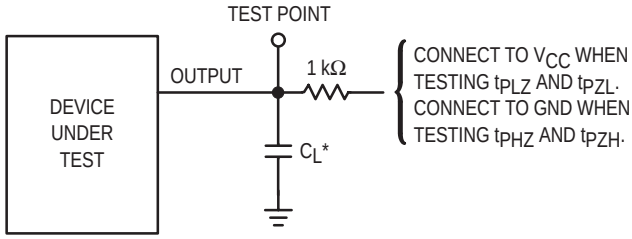
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

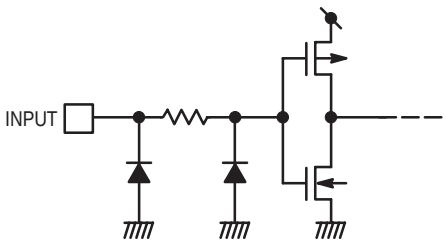


Figure 5. Input Equivalent Circuit

Octal Bus Buffer/Line Driver
with 3-State Outputs

MC74VHCT244A

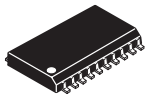
The MC74VHCT244A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT244A is a noninverting 3–state buffer, and has two active–low output enables. This device is designed to be used with 3–state memory address drivers, etc.

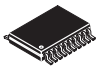
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT244A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

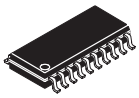
- High Speed: t_{PD} = 5.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.1V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 112 FETs or 28 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

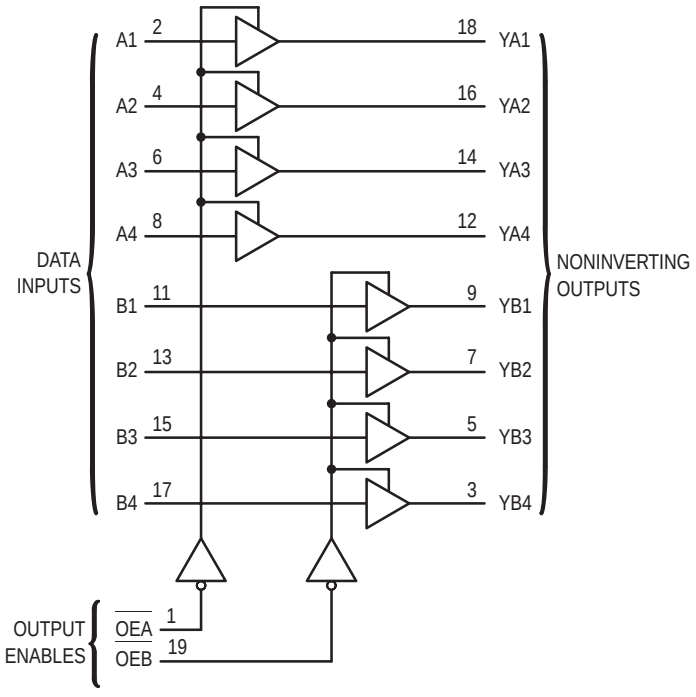


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

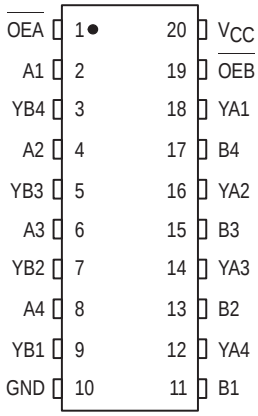
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}$, $\overline{OEB}$	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Output in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Output in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay A to YA or B to YB	V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		5.4 5.9	7.4 8.4	1.0 1.0	8.5 9.5	ns
t_{PZL}, t_{PZH}	Output Enable Time OEA to YA or OEB to YB	V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF		7.7 8.2	10.4 11.4	1.0 1.0	12.0 13.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time OEA to YA or OEB to YB	V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		8.8	11.4	1.0	13.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				9				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	18	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.1	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.1	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

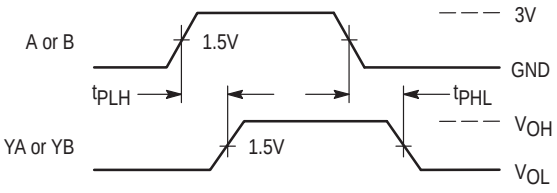


Figure 1.

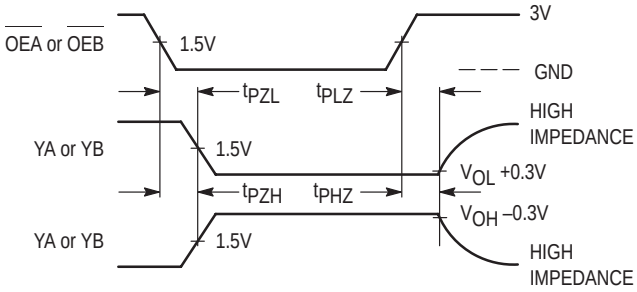
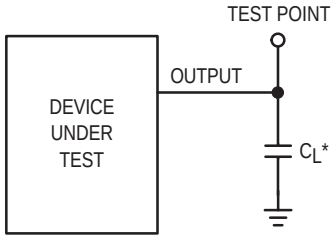


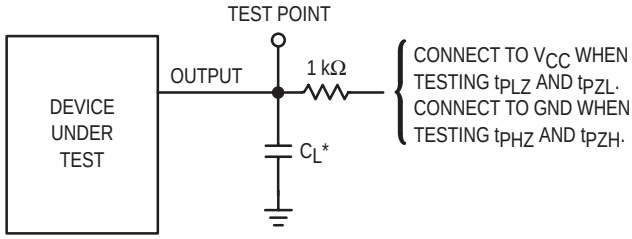
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Octal Bus Transceiver

MC74VHC245

The MC74VHC245 is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

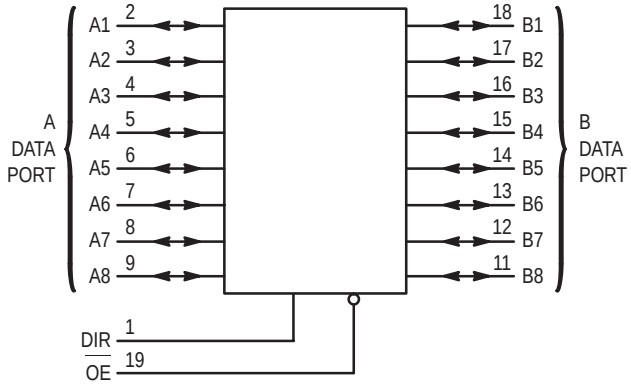
It is intended for two–way asynchronous communication between data buses. The direction of data transmission is determined by the level of the DIR input. The output enable pin (OE) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

- High Speed: t_{PD} = 4.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.2V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 308 FETs or 77 Equivalent Gates

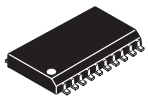
APPLICATION NOTES

1. Do not force a signal on an I/O pin when it is an active output, damage may occur.
2. All floating (high impedence) input or I/O pins must be fixed by means of pull up or pull down resistors or bus terminator ICs.
3. A parasitic diode is formed between the bus and V_{CC} terminals. Therefore, the VHC245 cannot be used to interface 5V to 3V systems directly.

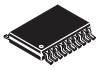


FUNCTION TABLE

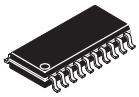
Control Inputs		Operation
OE	DIR	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High–Impedance State)



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

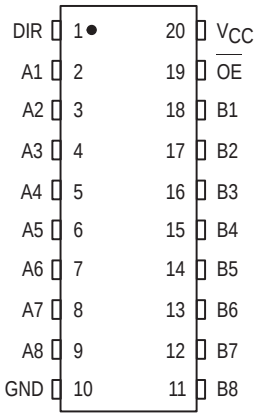


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

PIN ASSIGNMENT



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND (DIR, OE)	0 to 5.5			± 0.1		± 1.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B or B to A	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.8	8.4	1.0	10.0	ns
			C_L = 50pF		8.3	11.9	1.0	13.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		4.0	5.5	1.0	6.5	
			C_L = 50pF		5.5	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	Output Enable Time OE to A or B	V_{CC} = 3.3 ± 0.3V R_L = 1 kΩ	C_L = 15pF		8.5	13.2	1.0	15.5	ns
			C_L = 50pF		11.0	16.7	1.0	19.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1 kΩ	C_L = 15pF		5.8	8.5	1.0	10.0	
			C_L = 50pF		7.3	10.6	1.0	12.0	
t_{PLZ}, t_{PHZ}	Output Disable Time OE to A or B	V_{CC} = 3.3 ± 0.3V R_L = 1 kΩ	C_L = 50pF		11.5	15.8	1.0	18.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1 kΩ	C_L = 50pF		7.0	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance DIR, OE				4	10		10	pF
$C_{I/O}$	Maximum Three–State I/O Capacitance				8				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	21	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.9	–1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

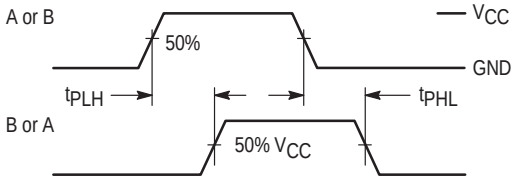


Figure 1.

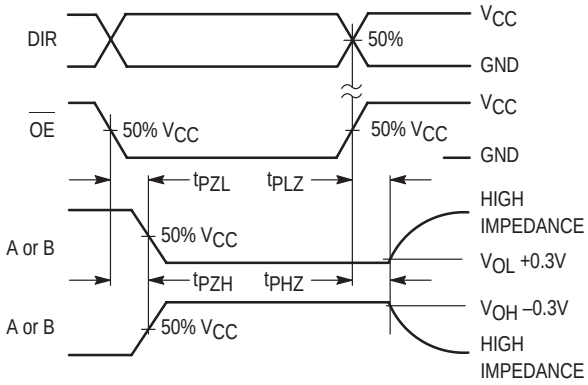
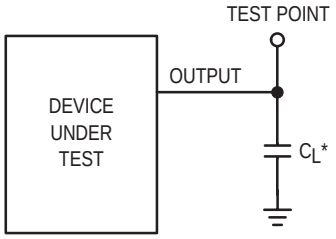


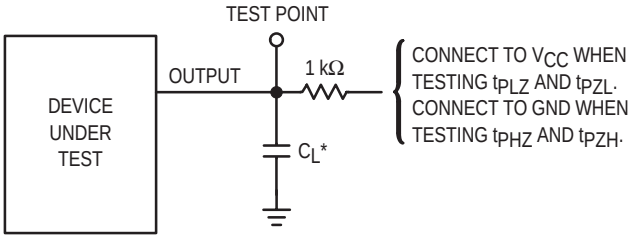
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

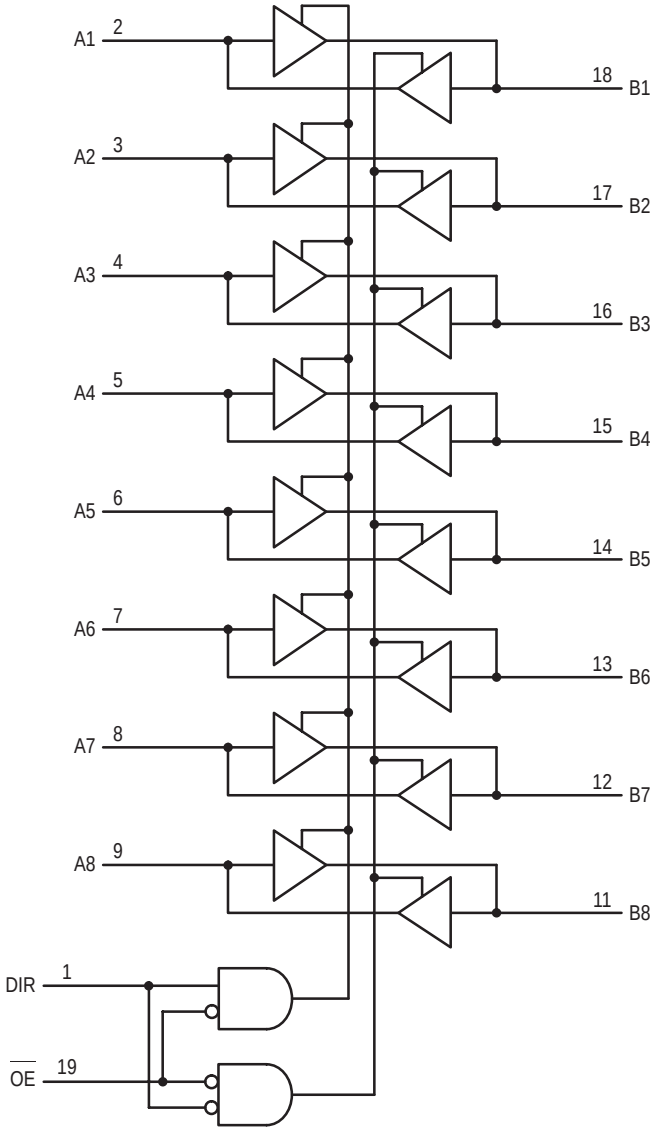
Figure 3.



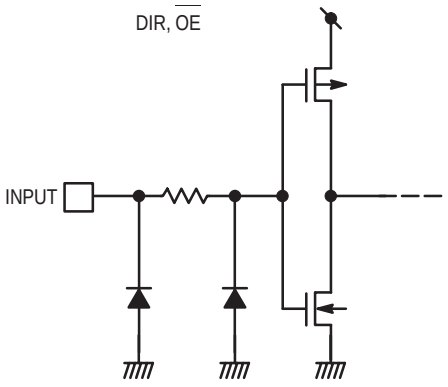
* Includes all probe and jig capacitance

Figure 4.

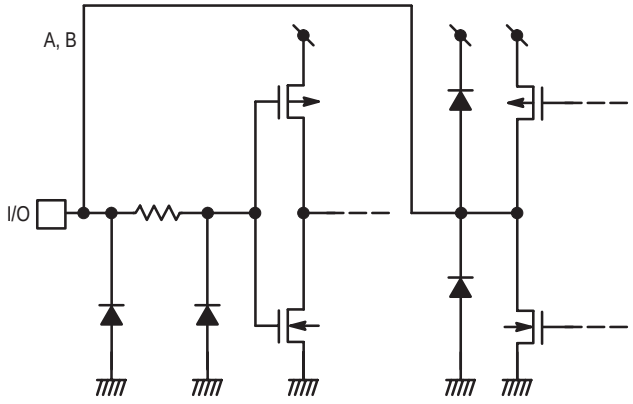
EXPANDED LOGIC DIAGRAM



INPUT EQUIVALENT CIRCUIT



BUS TERMINAL EQUIVALENT CIRCUIT



Octal Bus Transceiver

MC74VHCT245A

The MC74VHCT245A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It is intended for two–way asynchronous communication between data buses. The direction of data transmission is determined by the level of the DIR input. The output enable pin (OE) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

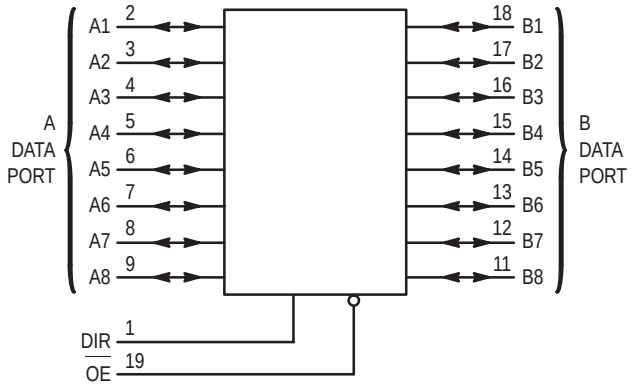
The VHCT245A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

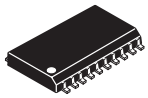
- High Speed: t_{PD} = 4.9ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 304 FETs or 76 Equivalent Gates

APPLICATION NOTES

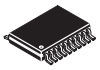
1. Do not force a signal on an I/O pin when it is an active output, damage may occur.
2. All floating (high impedence) input or I/O pins must be fixed by means of pull up or pull down resistors or bus terminator ICs.

LOGIC DIAGRAM

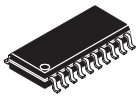




DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

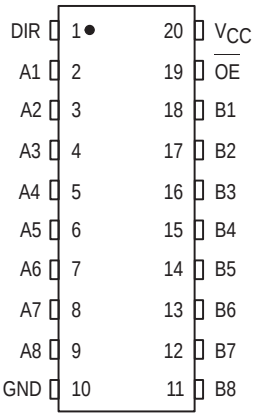


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
$\overline{OE}$	DIR	Operation
L	L	Data Tx from Bus B to Bus A
L	H	Data Tx from Bus A to Bus B
H	X	Buses Isolated (High–Z State)

MAXIMUM RATINGS*

V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
$V_{I/O}$	DC Output Voltage Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
$V_{I/O}$	DC Output Voltage	Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay A to B or B to A	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$ $C_L = 50pF$		4.9 5.4	7.7 8.7	1.0 1.0	8.5 9.5	ns
t_{PZL}, t_{PZH}	Output Enable Time OE to A or B	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$ $R_L = 1k\Omega$ $C_L = 50pF$		9.4 9.9	13.8 14.8	1.0 1.0	15.0 16.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time OE to A or B	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$ $R_L = 1k\Omega$		10.1	15.4	1.0	16.5	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$ (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			13				pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 2.)	16	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50pF$, $V_{CC} = 5.0V$)

Symbol	Parameter	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

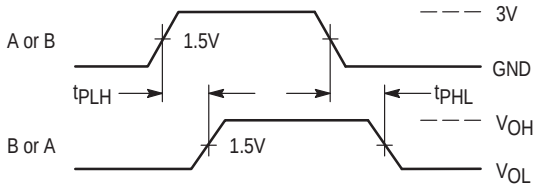


Figure 1.

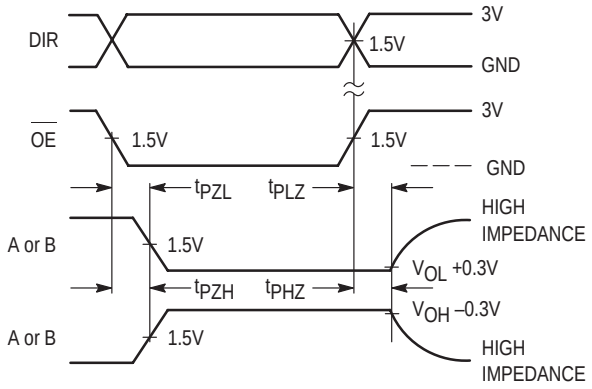
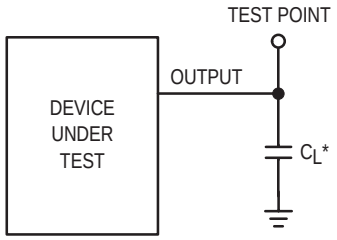


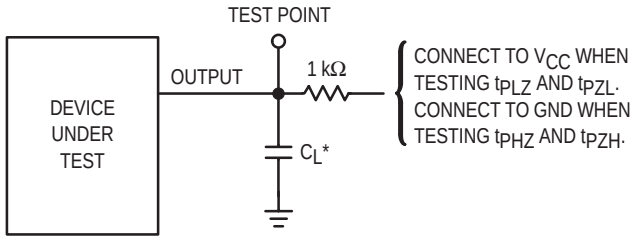
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

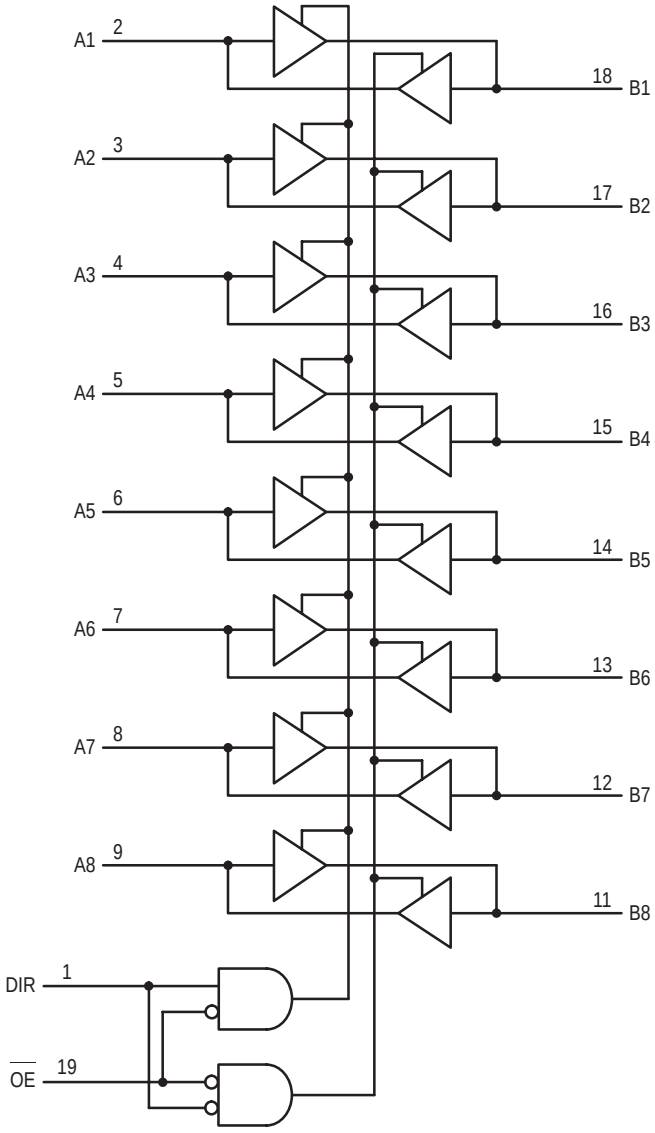
Figure 3.



* Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM



Octal D-Type Latch with 3-State Output

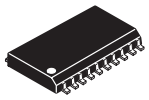
MC74VHC373

The MC74VHC373 is an advanced high speed CMOS octal latch with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

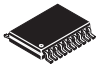
This 8–bit D–type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

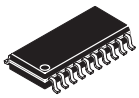
- High Speed: t_{PD} = 5.0ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.9V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

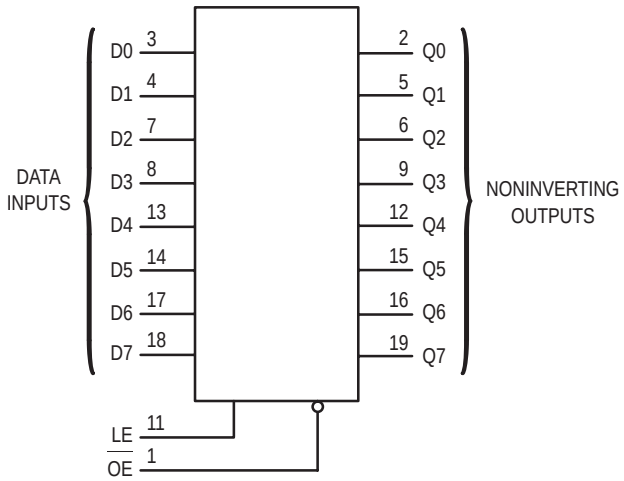


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

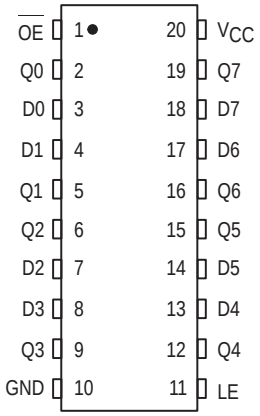
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V V_{CC} = 5.0V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.0	11.0	1.0	13.0	ns
			C_L = 50pF		9.5	14.5	1.0	16.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		4.9	7.2	1.0	8.5	
			C_L = 50pF		6.4	9.2	1.0	10.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.3	11.4	1.0	13.5	ns
			C_L = 50pF		9.8	14.9	1.0	17.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		5.0	7.2	1.0	8.5	
			C_L = 50pF		6.5	9.2	1.0	10.5	
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF		7.3	11.4	1.0	13.5	ns
			C_L = 50pF		9.8	14.9	1.0	17.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF		5.5	8.1	1.0	9.5	
			C_L = 50pF		7.0	10.1	1.0	11.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		9.5	13.2	1.0	15.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.5	9.2	1.0	10.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.5 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	27	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50 pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.6	– 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 3.3 \pm 0.3V$ $V_{CC} = 5.0 \pm 0.5V$		5.0 5.0	5.0 5.0	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 3.3 \pm 0.3V$ $V_{CC} = 5.0 \pm 0.5V$		4.0 4.0	4.0 4.0	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 3.3 \pm 0.3V$ $V_{CC} = 5.0 \pm 0.5V$		1.0 1.0	1.0 1.0	ns

SWITCHING WAVEFORMS

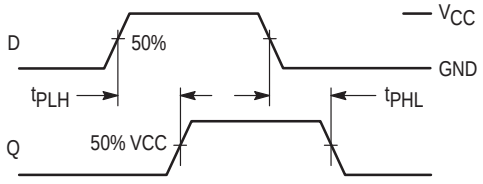


Figure 1.

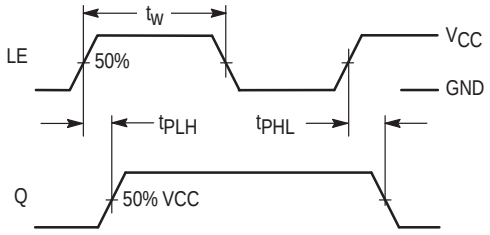


Figure 2.

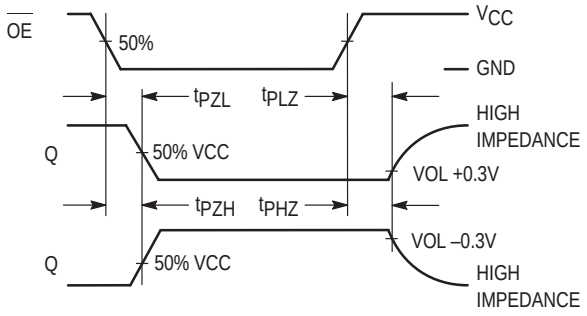


Figure 3.

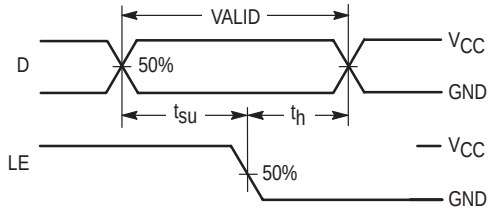
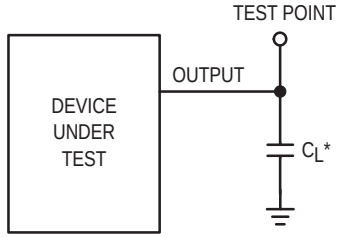


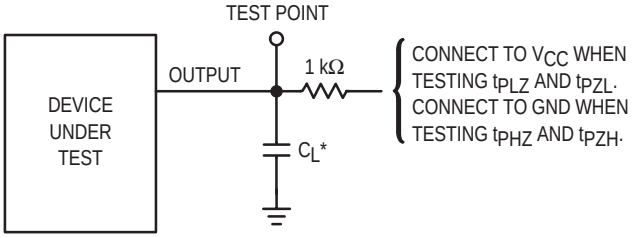
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

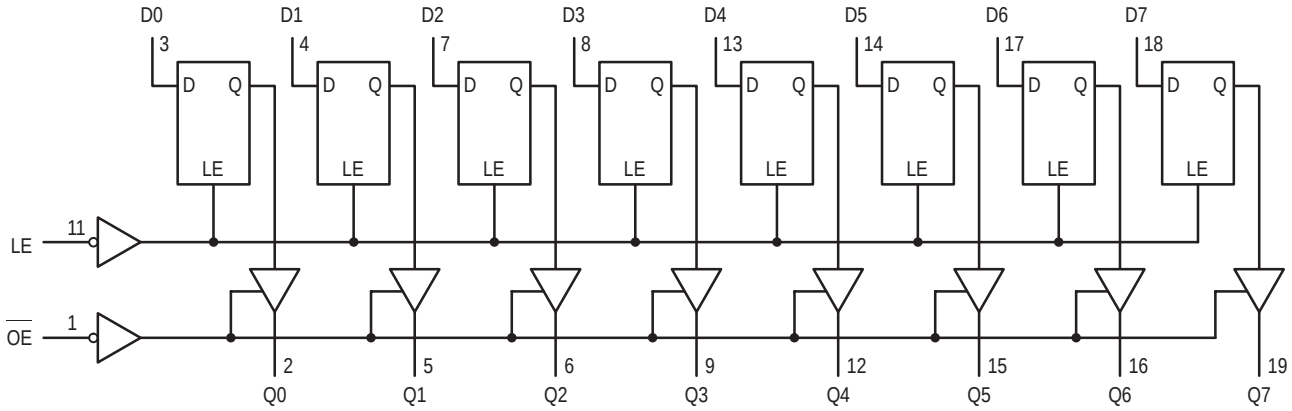
Figure 5.



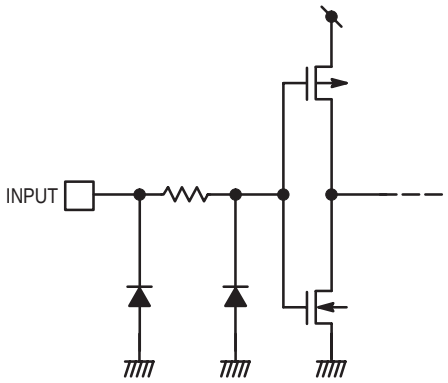
* Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



INPUT EQUIVALENT CIRCUIT



Octal D-Type Latch with 3-State Output

MC74VHCT373A

The MC74VHCT373A is an advanced high speed CMOS octal latch with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

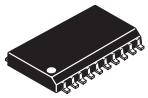
This 8–bit D–type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

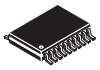
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT373A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

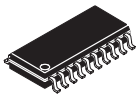
- High Speed: t_{PD} = 7.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 196 FETs or 49 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

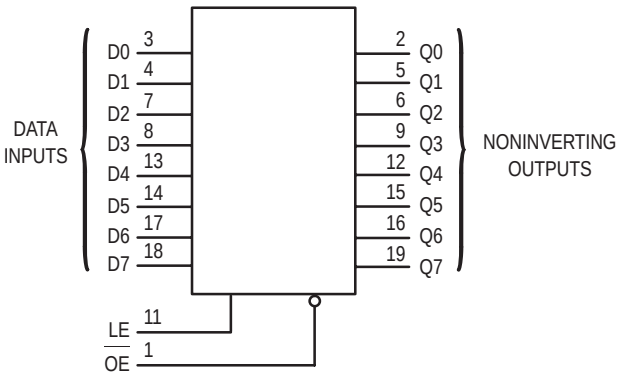


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

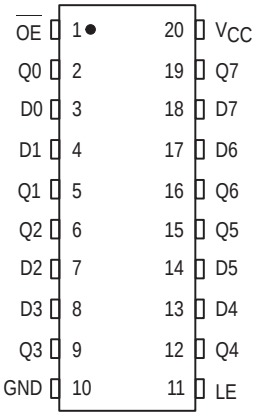
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{in}	DC Input Voltage		– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature		– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage	Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50µA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50µA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	µA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	µA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	µA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		7.7 8.5	12.3 13.3	1.0 1.0	13.5 14.5	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		5.1 5.9	8.5 9.5	1.0 1.0	9.5 10.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		6.3 7.1	10.9 11.9	1.0 1.0	12.5 13.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		8.8	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.5 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	25	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50 pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = – 40 to 85°C	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	V_{CC} = 5.0 ±0.5V		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to LE	V_{CC} = 5.0 ± 0.5V		1.5	1.5	ns
t_h	Minimum Hold Time, D to LE	V_{CC} = 5.0 ± 0.5V		3.5	3.5	ns

SWITCHING WAVEFORMS

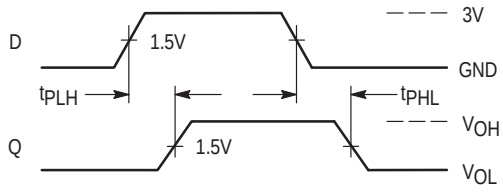


Figure 1.

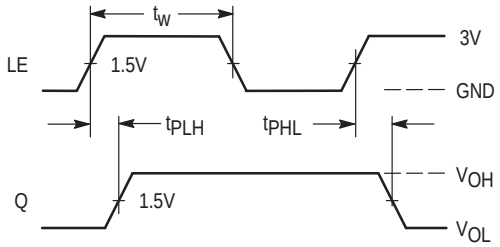


Figure 2.

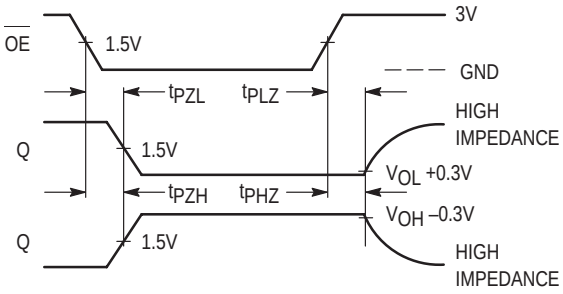


Figure 3.

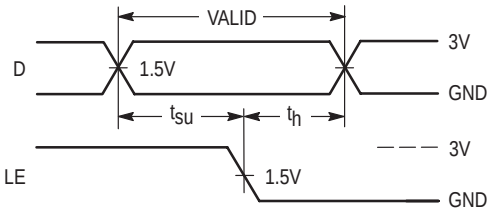
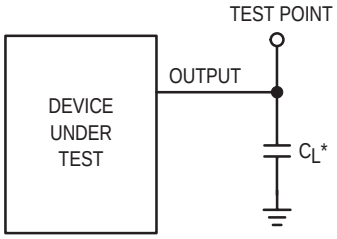


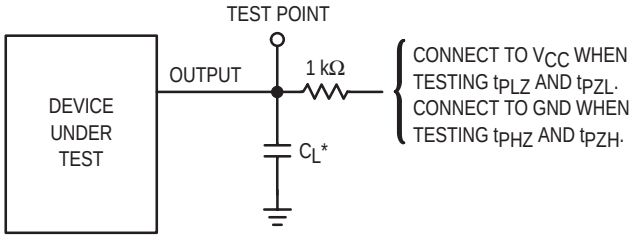
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

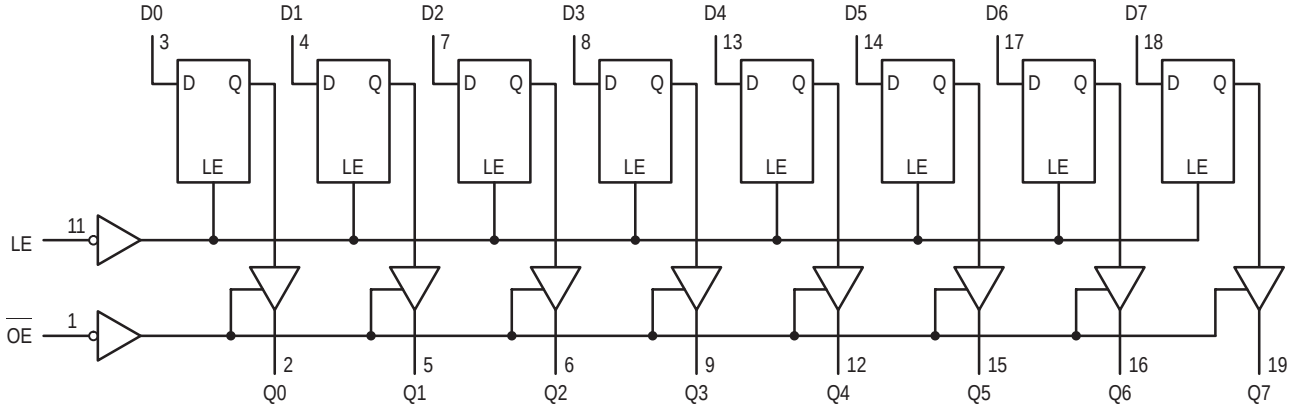
Figure 5.



* Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



Octal D-Type Flip-Flop with 3-State Output

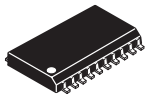
MC74VHC374

The MC74VHC374 is an advanced high speed CMOS octal flip–flip with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

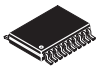
This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

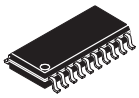
- High Speed: f_{max} = 185MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.9V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

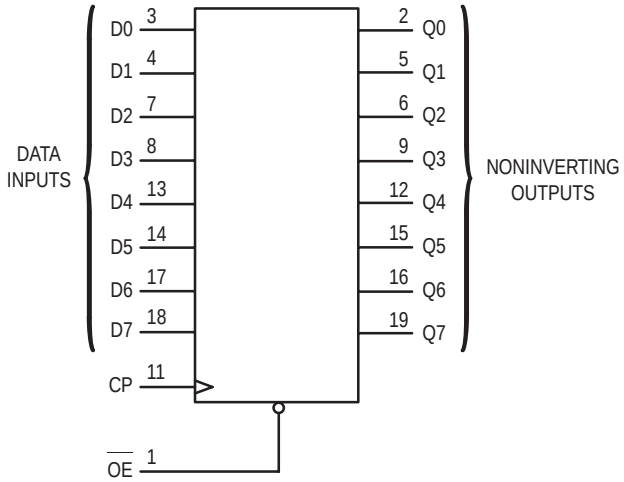


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

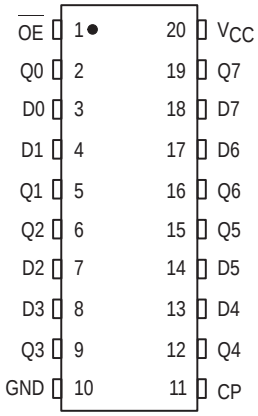
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V	0	100	ns/V
		V_{CC} = 5.0V	0	20	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0	1.50			1.50		V
			3.0 to 5.5	V_{CC} x 0.7			V_{CC} x 0.7		
V_{IL}	Maximum Low–Level Input Voltage		2.0			0.50		0.50	V
			3.0 to 5.5			V_{CC} x 0.3		V_{CC} x 0.3	
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			4.5	4.4	4.5		4.4		
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA	3.0	2.58			2.48		
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			4.5		0.0	0.1		0.1	
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA	3.0			0.36		0.44	
		I_{OL} = 8mA	4.5			0.36		0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3V C_L = 15pF C_L = 50pF	80 55	130 85		70 50		ns
		V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF	130 85	185 120		110 75		
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	V_{CC} = 3.3 ± 0.3V C_L = 15pF C_L = 50pF		8.1 10.6	12.7 16.2	1.0 1.0	15.0 18.5	ns
		V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		5.4 6.9	8.1 10.1	1.0 1.0	9.5 11.5	
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 3.3 ± 0.3V C_L = 15pF R_L = 1kΩ C_L = 50pF		7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5	ns
		V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		5.1 6.6	7.6 9.6	1.0 1.0	9.0 11.0	
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 3.3 ± 0.3V C_L = 50pF R_L = 1kΩ		10.2	14.0	1.0	16.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		6.1	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V C_L = 50pF (Note 1.)			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	32	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.6	– 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.5 5.0	ns
t_{su}	Minimum Setup Time, D to CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		4.5 3.0	4.5 3.0	ns
t_h	Minimum Hold Time, D to CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		2.0 2.0	2.0 2.0	ns
t_r, t_f	Maximum Input Rise and Fall Times	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V				ns

SWITCHING WAVEFORMS

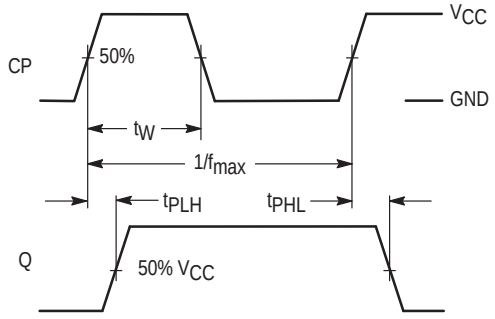


Figure 1.

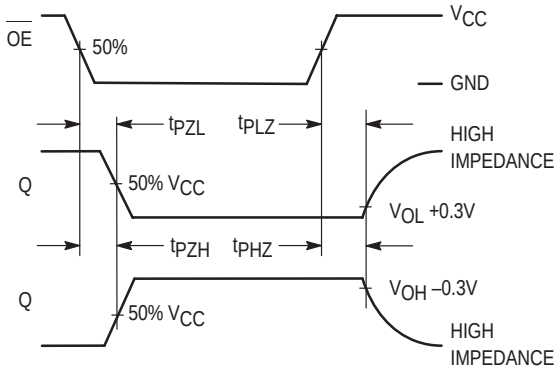


Figure 2.

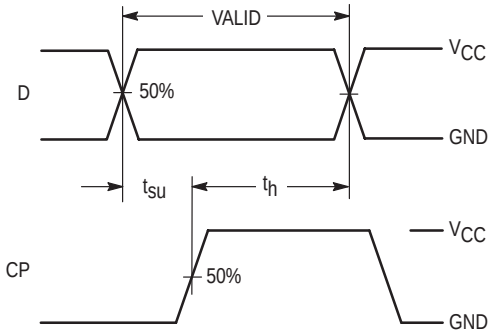
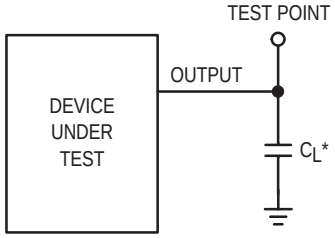


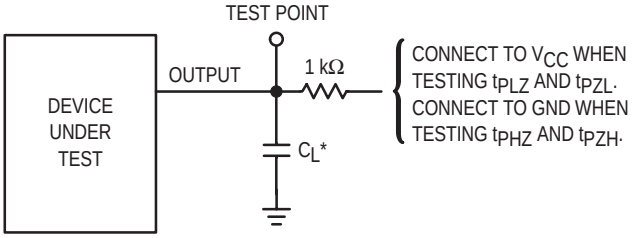
Figure 3.

TEST CIRCUITS



* Includes all probe and jig capacitance

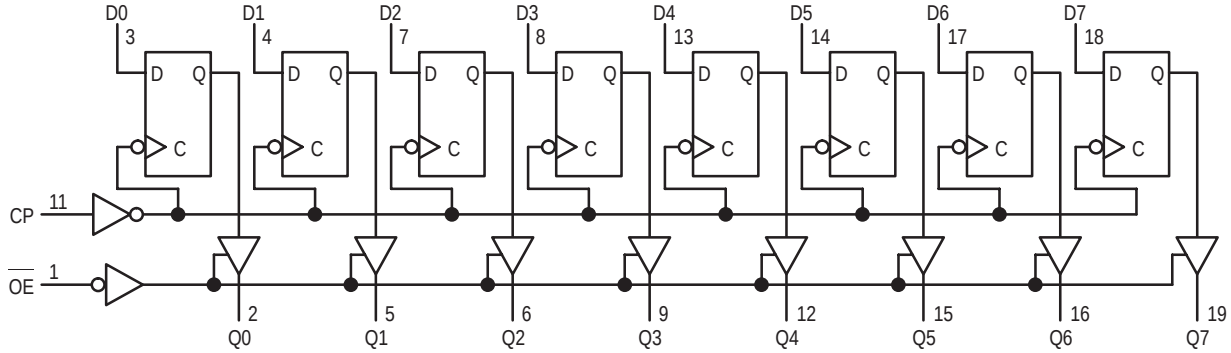
Figure 4.



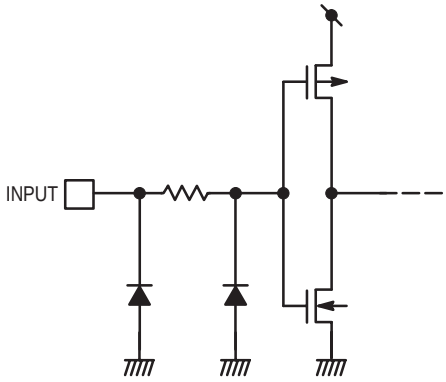
* Includes all probe and jig capacitance

Figure 5.

EXPANDED LOGIC DIAGRAM



INPUT EQUIVALENT CIRCUIT



Octal D-Type Flip-Flop with 3-State Output

MC74VHCT374A

The MC74VHCT374A is an advanced high speed CMOS octal flip–flop with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

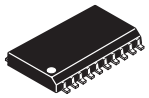
This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

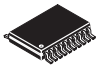
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT374A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

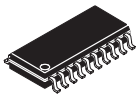
- High Speed: f_{max} = 140MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 276 FETs or 69 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

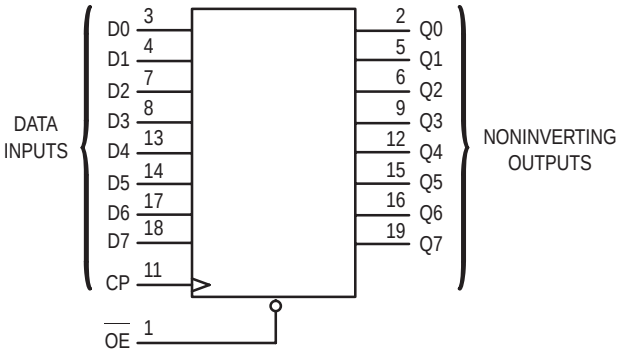


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

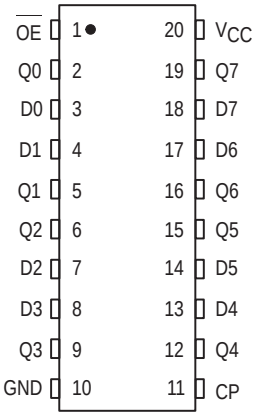
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF	90 85	140 130		80 95		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time OE to Q	V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		7.0	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				9				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	25	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = – 40 to 85°C	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	V_{CC} = 5.0 ± 0.5 V		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns
t_h	Minimum Hold Time, D to CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns

SWITCHING WAVEFORMS

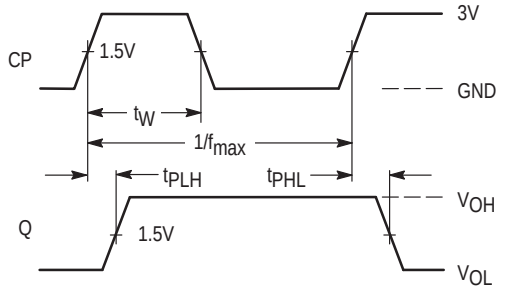


Figure 1.

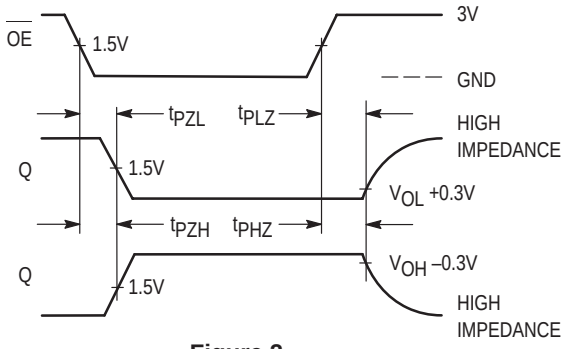


Figure 2.

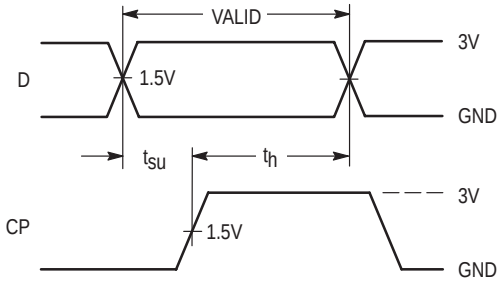
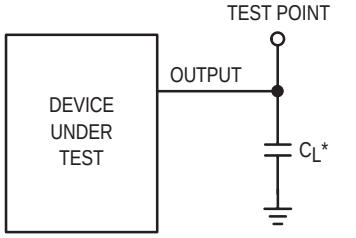


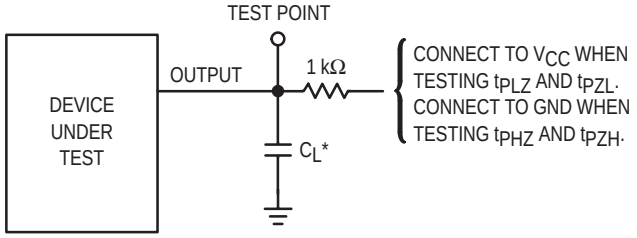
Figure 3.

TEST CIRCUITS



* Includes all probe and jig capacitance

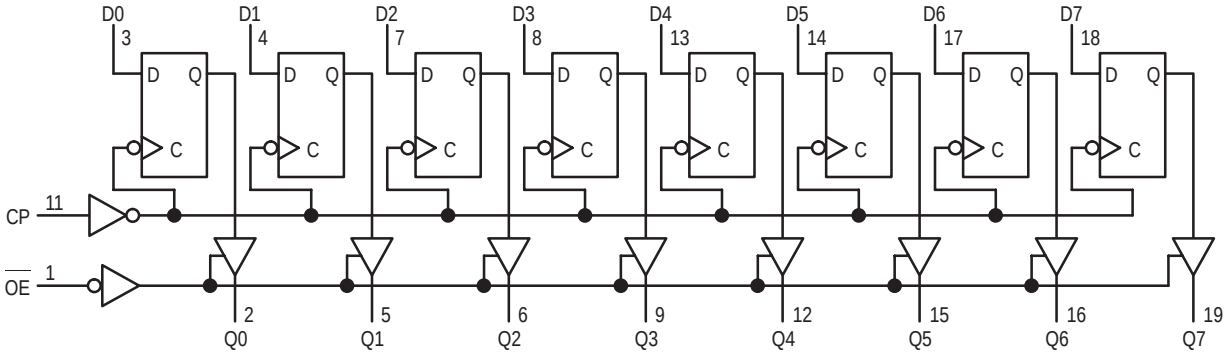
Figure 4.



* Includes all probe and jig capacitance

Figure 5.

EXPANDED LOGIC DIAGRAM



Dual 4-Bit Binary Ripple Counter

MC74VHC393

The MC74VHC393 is an advanced high speed CMOS dual 4–bit binary ripple counter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This device consists of two independent 4–bit binary ripple counters with parallel outputs from each counter stage. A ÷256 counter can be obtained by cascading the two binary counters.

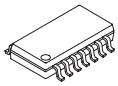
Internal flip–flops are triggered by high–to–low transitions of the clock input. Reset for the counters is asynchronous and active–high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the VHC393.

The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: f_{max} = 170MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 236 FETs or 59 Equivalent Gates

D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

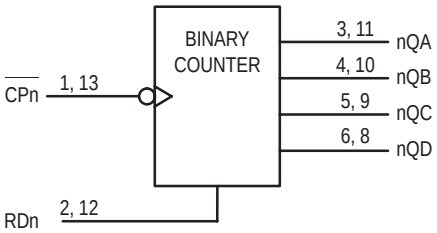


M SUFFIX
14–LEAD SOIC EIAJ PACKAGE
CASE 965–01

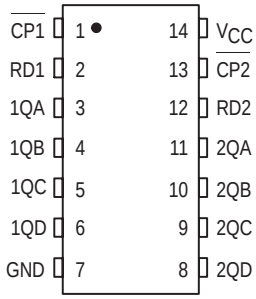
ORDERING INFORMATION

MC74VHCXXXD	SOIC
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		
Clock	**Reset**	**Outputs**
X	H	L
H	L	No Change
L	L	No Change
↑	L	No Change
↓	L	Next State

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V V_{CC} = 5.0V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF	75 45	120 65		65 35		ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF	125 85	170 115		105 75		
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to QA	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		8.6 11.1	13.2 16.7	1.0 1.0	15.5 19.0	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		5.8 7.3	8.5 10.5	1.0 1.0	10.0 12.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to QB	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		10.2 12.7	15.8 19.3	1.0 1.0	18.5 22.0	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		6.8 8.3	9.8 11.8	1.0 1.0	11.5 13.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to QC	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		11.7 14.2	18.0 21.5	1.0 1.0	21.0 24.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		7.7 9.2	11.2 13.2	1.0 1.0	13.0 15.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to QD	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		13.0 15.5	19.7 23.2	1.0 1.0	23.0 26.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		8.5 10.0	12.5 14.5	1.0 1.0	14.5 16.5	
t_{PHL}	Maximum Propagation Delay, RD to Qn	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		7.9 10.4	12.3 15.8	1.0 1.0	14.5 18.0	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		5.4 6.9	8.1 10.1	1.0 1.0	9.5 11.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	23	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per 4–bit counter). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0ns$, $C_L = 50pF$, $V_{CC} = 5.0V$)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.5	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0ns$)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	ns
t_w	Minimum Pulse Width, RD	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	ns
t_{rec}	Minimum Recovery Time, RD to CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 4.0	5.0 4.0	ns
t_r, t_f	Minimum Input Rise and Fall Times	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		330 100	330 100	ns

SWITCHING WAVEFORMS

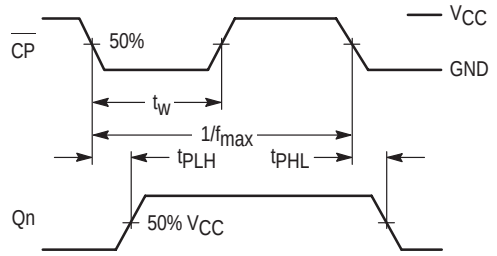


Figure 1.

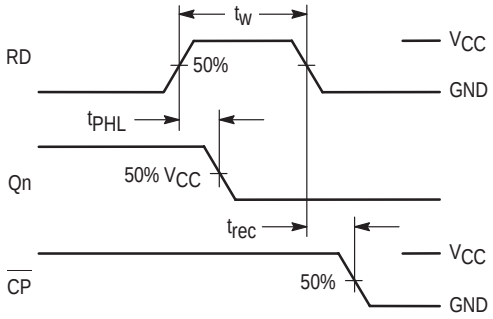
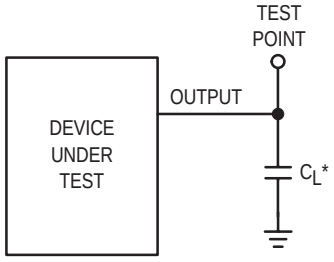


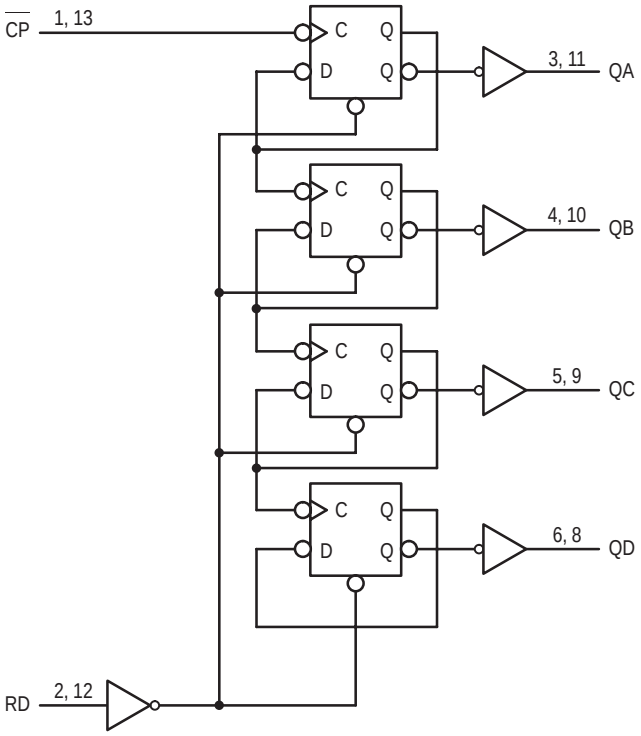
Figure 2.



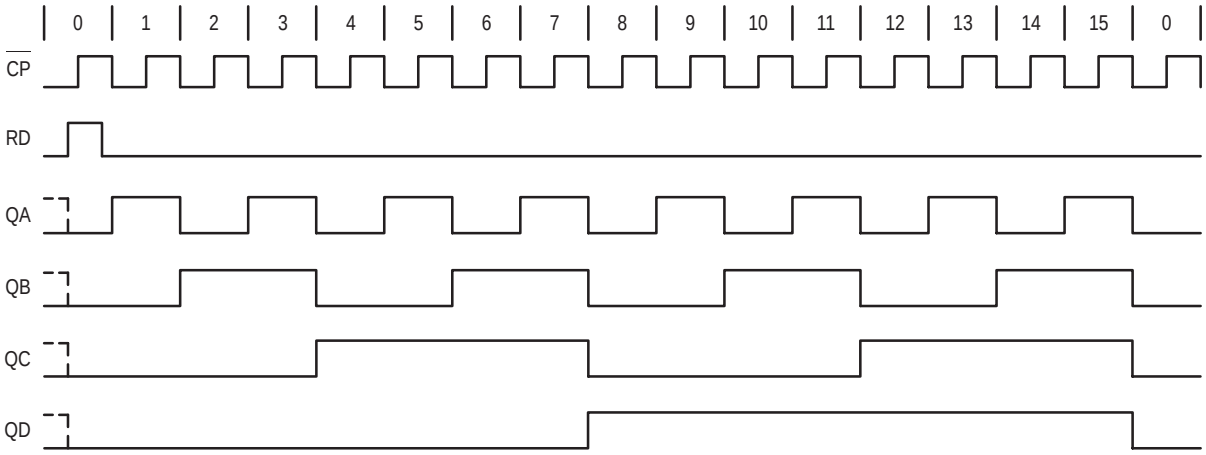
* Includes all probe and jig capacitance

Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



COUNT SEQUENCE

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Octal Bus Buffer
Inverting

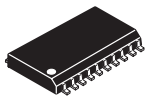
MC74VHC540

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

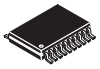
The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND–ed active–low output enables. When either OE1 or OE2 are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

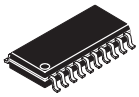
- High Speed: t_{PD} = 3.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.2V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 124 FETs or 31 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

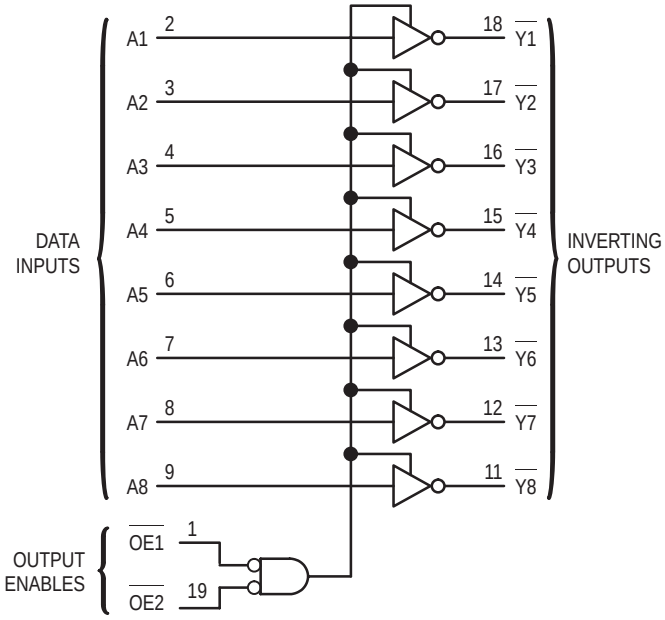


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

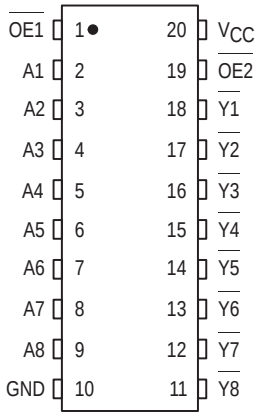
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output $\overline{Y}$
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y (Figures 1 and 3)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		4.8	7.0	1.0	8.5	ns
			C_L = 50pF		7.3	10.5	1.0	12.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		3.7	5.0	1.0	6.0	
			C_L = 50pF		5.2	7.0	1.0	8.0	
t_{PZL}, t_{PZH}	Output Enable TIme, OEn to Y (Figures 2 and 4)	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF		6.8	10.5	1.0	12.5	ns
			C_L = 50pF		9.3	14.0	1.0	16.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF		4.7	7.2	1.0	8.5	
			C_L = 50pF		6.2	9.2	1.0	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, OEn to Y (Figures 2 and 4)	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		11.2	15.4	1.0	17.5	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.0	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5			ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0			ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	17	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

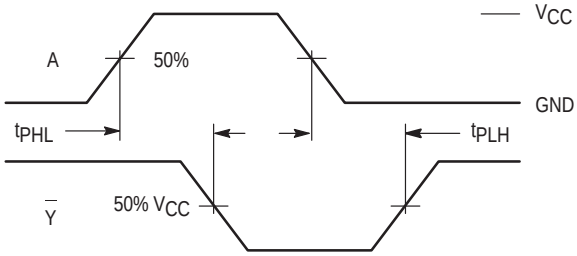


Figure 1.

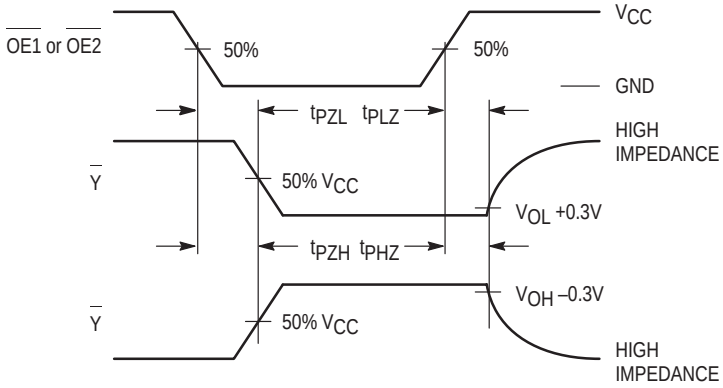
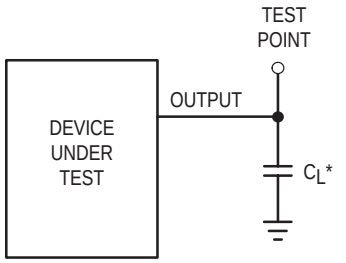


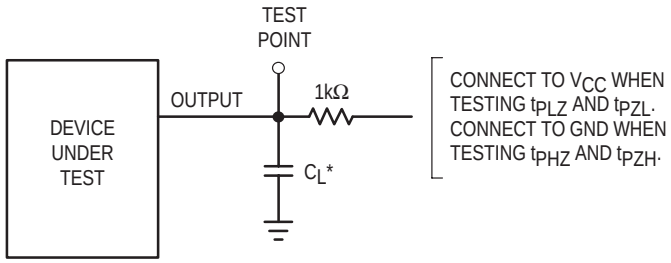
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

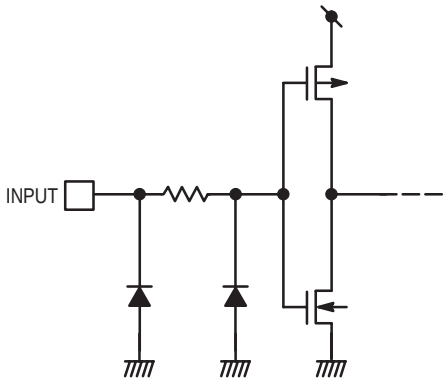
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

INPUT EQUIVALENT CIRCUIT



Octal Bus Buffer

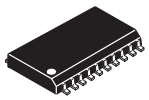
MC74VHC541

The MC74VHC541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

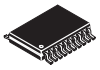
The MC74VHC541 is a noninverting type. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

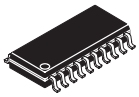
- High Speed: t_{PD} = 3.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.2V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

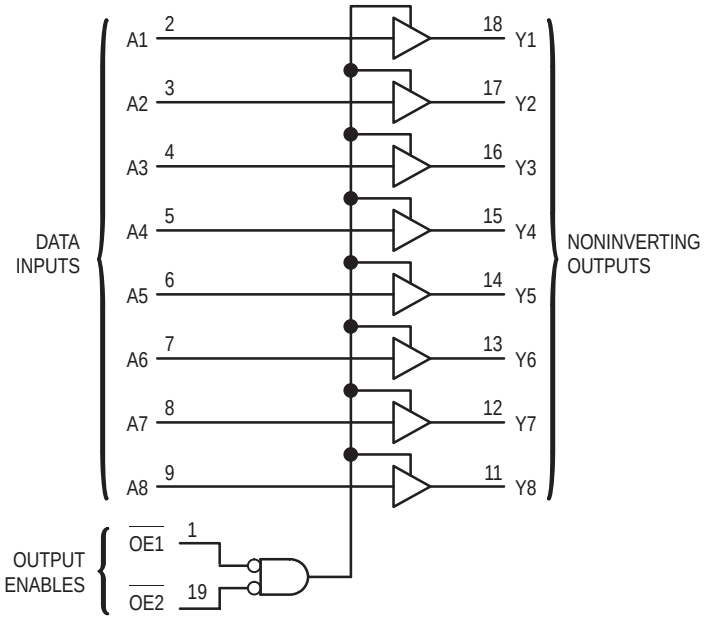


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

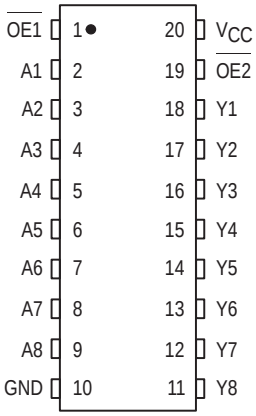
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		5.0	7.0	1.0	8.5	ns
			C_L = 50pF		7.5	10.5	1.0	12.0	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		3.5	5.0	1.0	6.0	
			C_L = 50pF		5.0	7.0	1.0	8.0	
t_{PZL}, t_{PZH}	Output Enable TIme, OE to Y	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF		6.8	10.5	1.0	12.5	ns
			C_L = 50pF		9.3	14.0	1.0	16.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF		4.7	7.2	1.0	8.5	
			C_L = 50pF		6.2	9.2	1.0	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Y	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		11.2	15.4	1.0	17.5	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.0	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	18	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

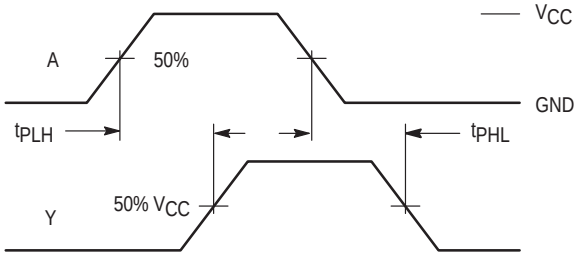


Figure 1.

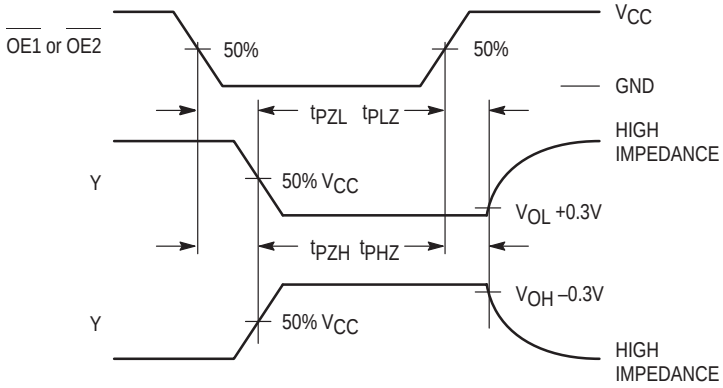
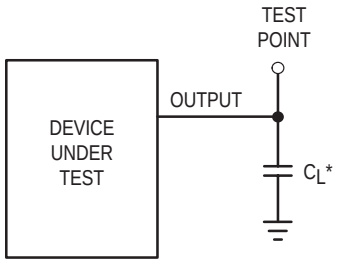


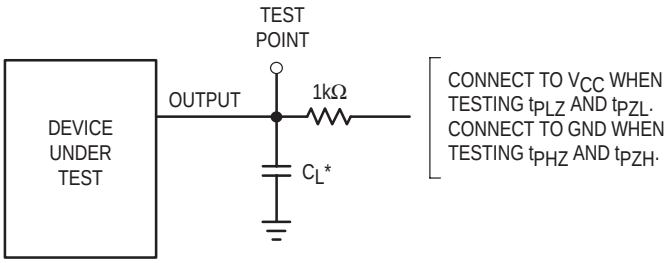
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

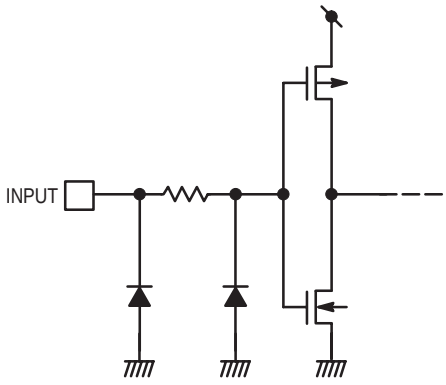
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

INPUT EQUIVALENT CIRCUIT



Octal Bus Buffer

MC74VHCT541A

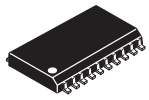
The MC74VHCT541A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT541A is a noninverting, 3–state, buffer/line driver/line receiver. When either OE1 or OE2 is high, the terminal outputs are in the high impedance state.

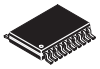
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT541A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

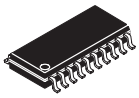
- High Speed: t_{PD} = 5.4ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4µA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

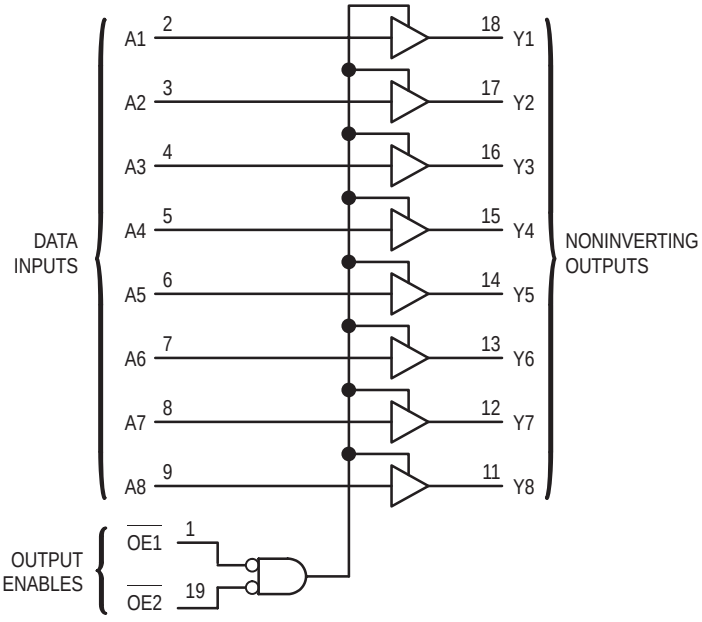


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

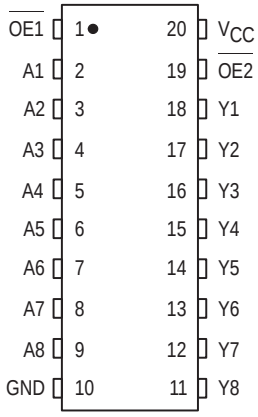
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		5.0 5.5	6.9 7.9	1.0 1.0	8.0 9.0	ns
t_{PZL}, t_{PZH}	Output Enable TIme, OE to Y	V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		8.3 8.8	11.3 12.3	1.0 1.0	13.0 14.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Y	V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		9.4	11.9	1.0	13.5	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)			9				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	19	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

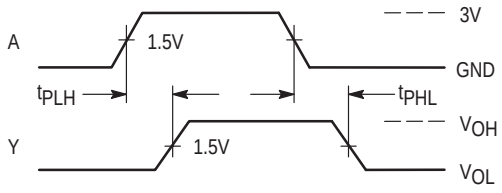


Figure 1.

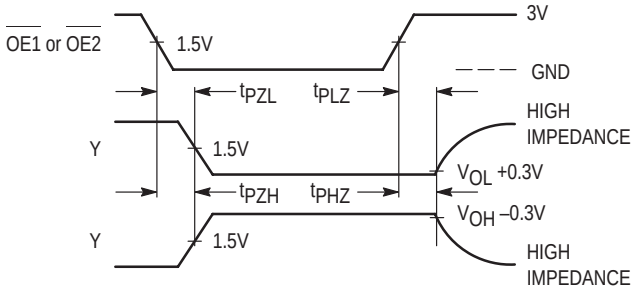
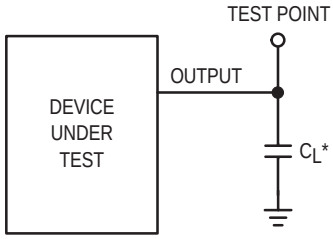


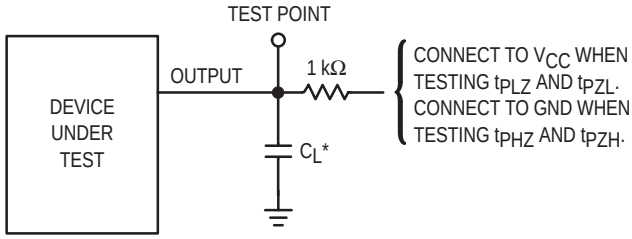
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

Octal D-Type Latch with 3-State Output

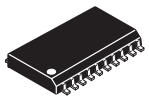
MC74VHC573

The MC74VHC573 is an advanced high speed CMOS octal latch with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

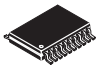
This 8–bit D–type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

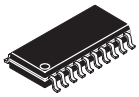
- High Speed: t_{PD} = 4.5ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.2V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

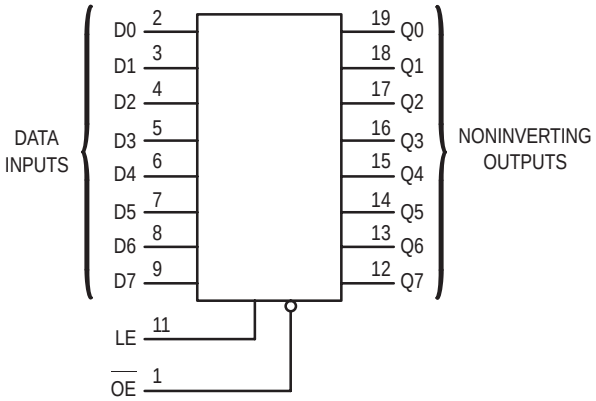


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

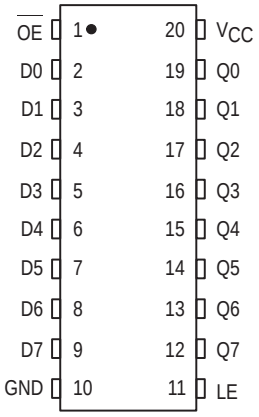
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V V_{CC} = 5.0V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		7.6 10.1	11.9 15.4	1.0 1.0	14.0 17.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		5.0 6.5	7.7 9.7	1.0 1.0	9.0 11.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.5 6.0	6.8 8.0	1.0 1.0	8.0 10.0	
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF C_L = 50pF		7.3 9.8	11.5 15.0	1.0 1.0	13.5 17.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF		5.2 6.7	7.7 9.7	1.0 1.0	9.0 11.0	
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		10.7	14.5	1.0	16.5	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.7	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.5 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	29	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50 pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 3.3 \pm 0.3V$ $V_{CC} = 5.0 \pm 0.5V$		5.0 5.0	5.0 5.0	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 3.3 \pm 0.3V$ $V_{CC} = 5.0 \pm 0.5V$		3.5 3.5	3.5 3.5	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 3.3 \pm 0.3V$ $V_{CC} = 5.0 \pm 0.5V$		1.5 1.5	1.5 1.5	ns

SWITCHING WAVEFORMS

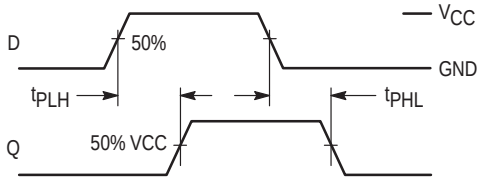


Figure 1.

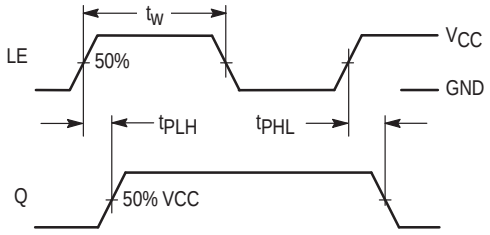


Figure 2.

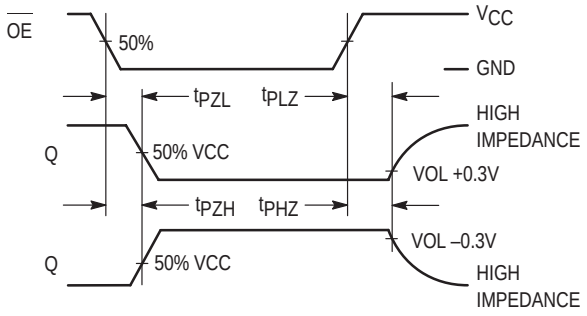


Figure 3.

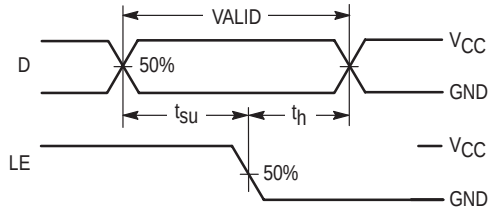
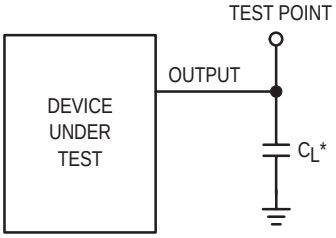


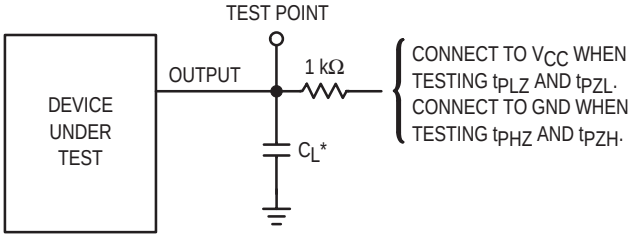
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

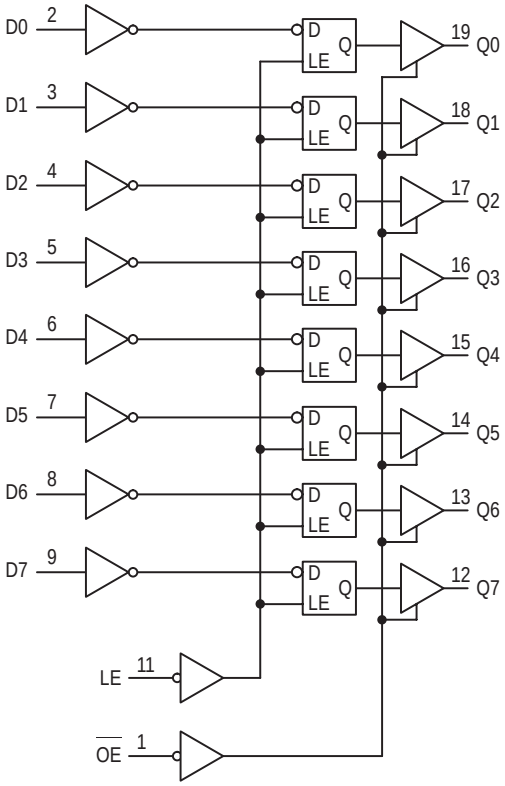
Figure 5.



* Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



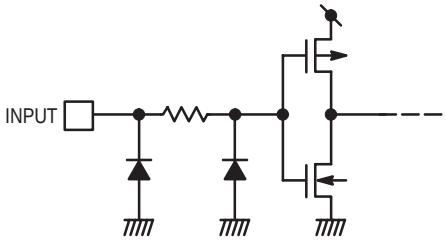


Figure 7. Input Equivalent Circuit

Octal D-Type Latch with 3-State Output

MC74VHCT573A

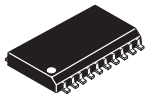
The MC74VHCT573A is an advanced high speed CMOS octal latch with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8–bit D–type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

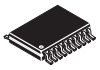
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT573A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

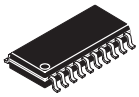
- High Speed: t_{PD} = 7.7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

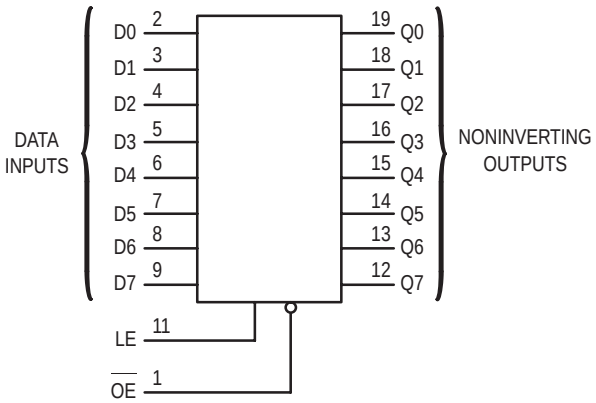


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

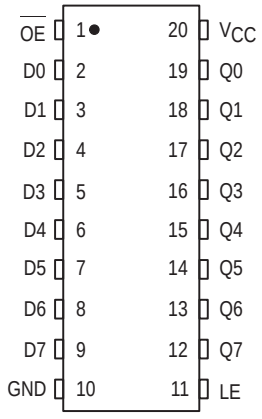
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		7.7 8.5	12.3 13.3	1.0 1.0	13.5 14.5	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF C_L = 50pF		5.1 5.9	8.5 9.5	1.0 1.0	9.5 10.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ C_L = 50pF		6.3 7.1	10.9 11.9	1.0 1.0	12.5 13.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		8.8	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.5 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	25	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50 pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = – 40 to 85°C	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	V_{CC} = 5.0 ±0.5V		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to LE	V_{CC} = 5.0 ± 0.5V		1.5	1.5	ns
t_h	Minimum Hold Time, D to LE	V_{CC} = 5.0 ± 0.5V		3.5	3.5	ns

SWITCHING WAVEFORMS

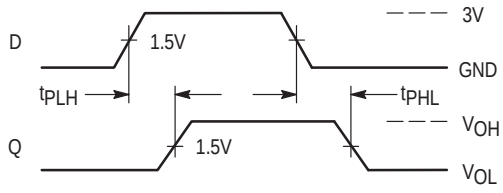


Figure 1.

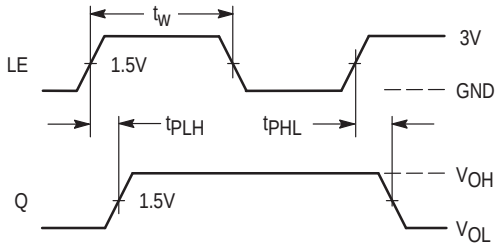


Figure 2.

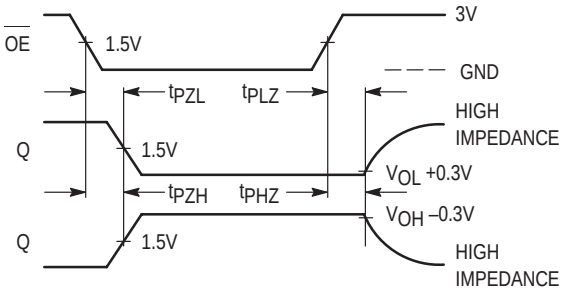


Figure 3.

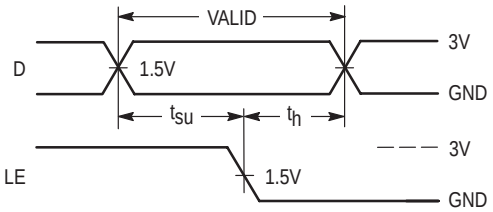
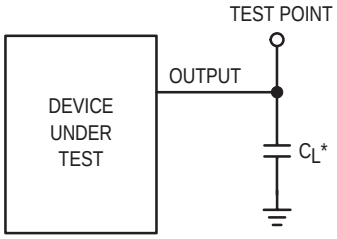


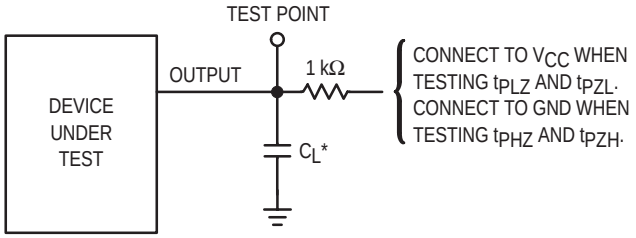
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance

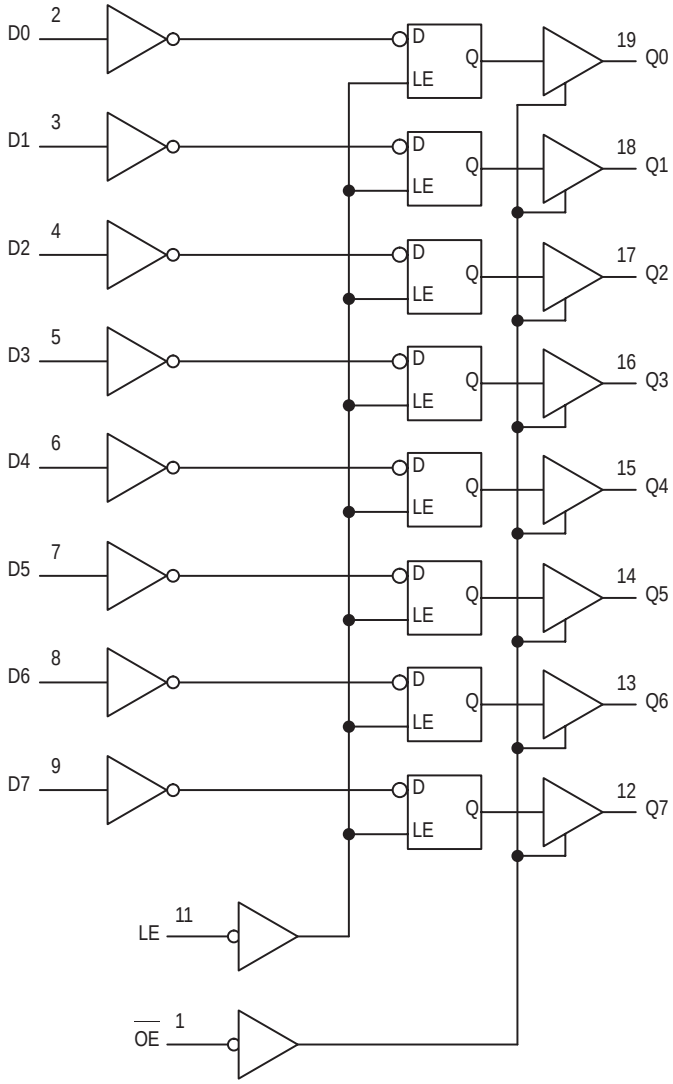
Figure 5.



* Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



Octal D-Type Flip-Flop with 3-State Output

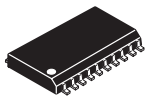
MC74VHC574

The MC74VHC574 is an advanced high speed CMOS octal flip–flip with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

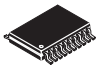
This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

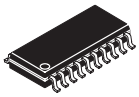
- High Speed: f_{max} = 180MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.2V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

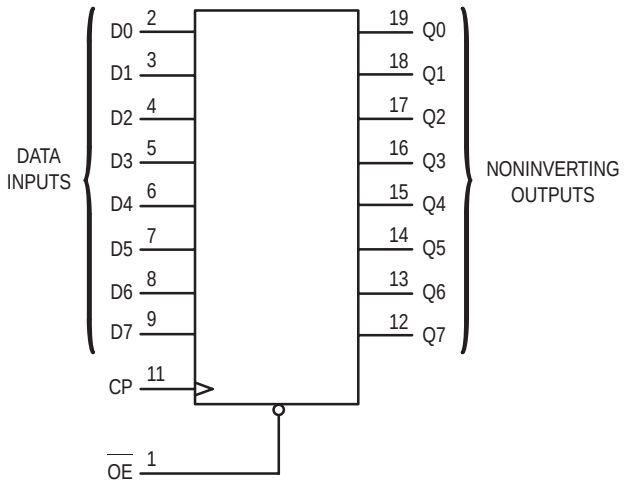


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

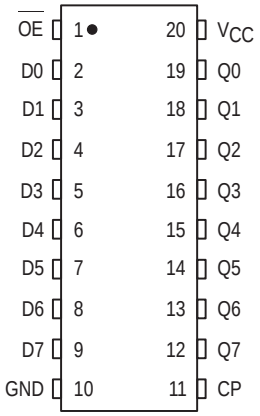
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V V_{CC} = 5.0V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF	80 50	125 75	— —	65 45	— —	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF	130 85	180 115	— —	110 75	— —	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	V_{CC} = 3.3 ± 0.3	C_L = 15pF C_L = 50pF	— —	8.5 11.0	13.2 16.7	1.0 1.0	15.5 19.0	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF	— —	5.6 7.1	8.6 10.6	1.0 1.0	10.0 12.0	
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF C_L = 50pF	— —	8.2 10.7	12.8 16.3	1.0 1.0	15.0 18.5	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF	— —	5.9 7.4	9.0 11.0	1.0 1.0	10.5 12.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF	—	11.0	15.0	1.0	17.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF	—	7.1	10.1	1.0	11.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1.)	C_L = 50pF	—	—	1.5	—	1.5	ns
		V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF	—	—	1.0	—	1.0	ns
C_{in}	Maximum Input Capacitance			—	4	10	—	10	pF
C_{out}	Maximum Three–State Output Capacitance, Output in High–Impedance State			—	6	—	—	—	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	28	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage	—	3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage	—	1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
t_{su}	Minimum Setup Time, D to CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V	— —	3.5 3.5	3.5 3.5	ns
t_h	Minimum Hold Time, CP to D	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V	— —	1.5 1.5	1.5 1.5	ns
t_w	Minimum Pulse Width, CP	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V	— —	5.0 5.0	5.5 5.0	ns

SWITCHING WAVEFORMS

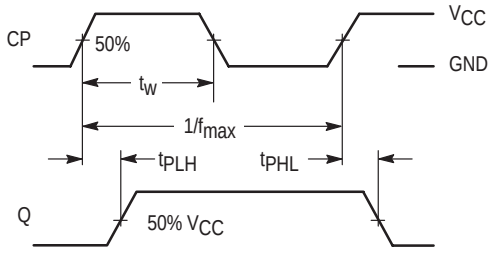


Figure 1.

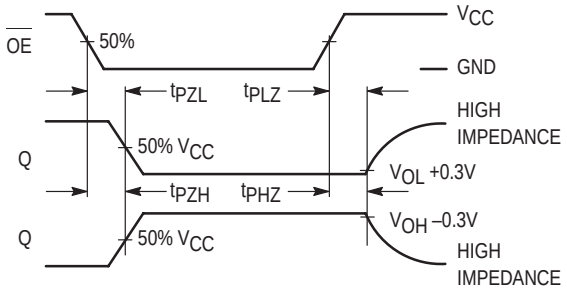


Figure 2.

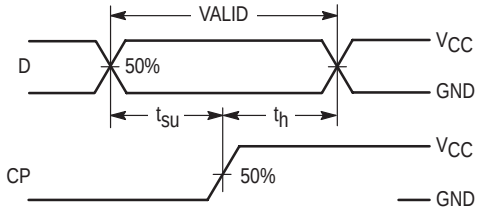
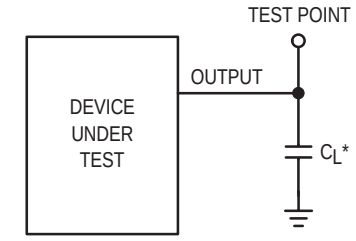
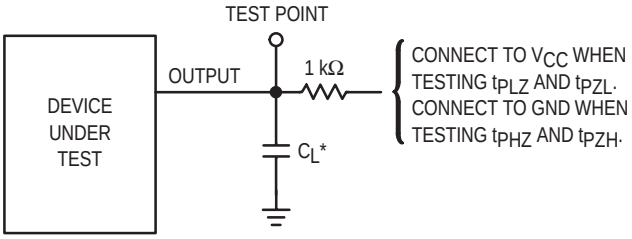


Figure 3.



* Includes all probe and jig capacitance

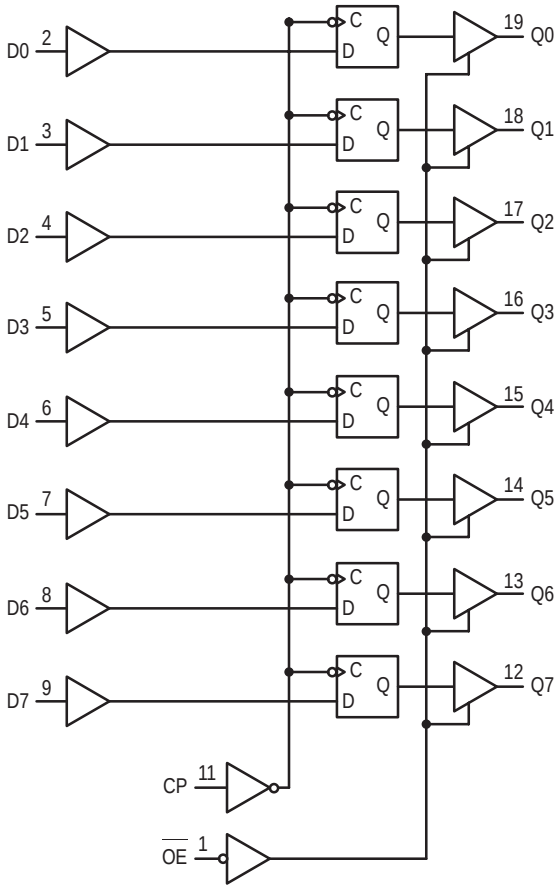
Figure 4.



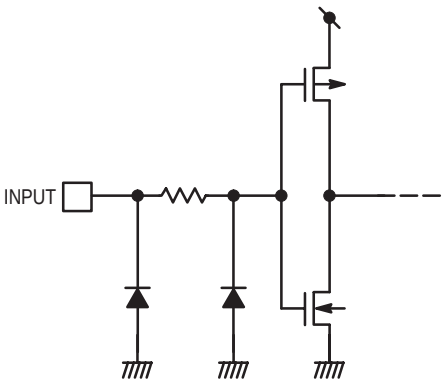
* Includes all probe and jig capacitance

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



INPUT EQUIVALENT CIRCUIT



Octal D-Type Flip-Flop with 3-State Output

MC74VHCT574A

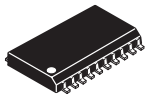
The MC74VHCT574A is an advanced high speed CMOS octal flip–flop with 3–state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8–bit D–type flip–flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

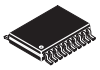
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT574A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

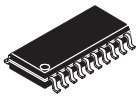
- High Speed: f_{max} = 140MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.6V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04



DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

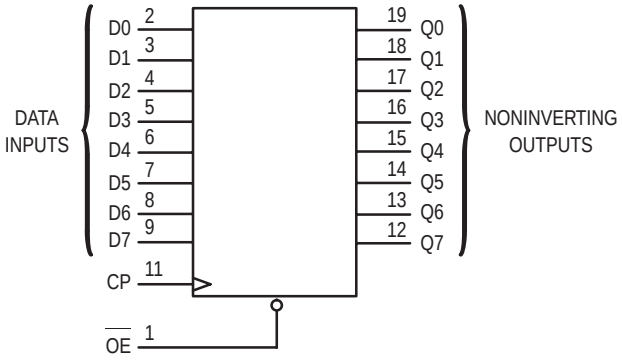


M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

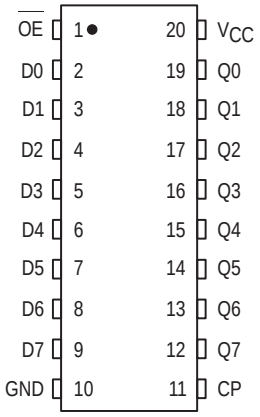
ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	– 0.5 to + 7.0 – 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Outputs in 3–State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = – 50μA	4.5	4.4	4.5		4.4		V
		I_{OH} = – 8mA	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF	90 85	140 130		80 95		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, OE to Q	V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to Q	V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		7.0	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5V (Note 1.)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance, Output in High–Impedance State				9				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	25	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = – 40 to 85°C	Unit
			Typ	Limit	Limit	
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 5.0 ± 0.5 V		6.5	8.5	ns
t_h	Minimum Hold Time, CP to D	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns
t_w	Minimum Pulse Width, CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns

SWITCHING WAVEFORMS

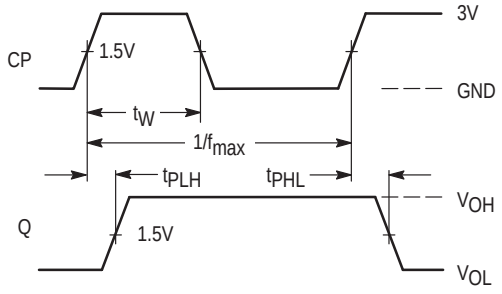


Figure 1.

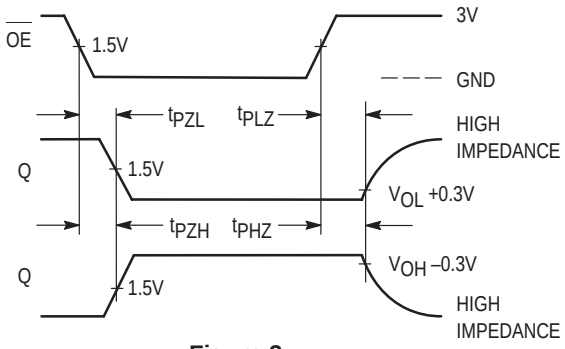


Figure 2.

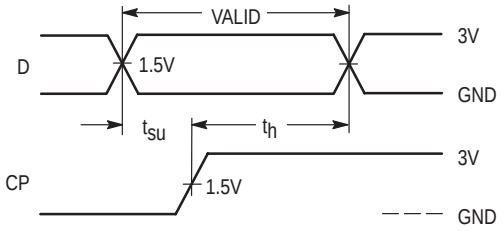
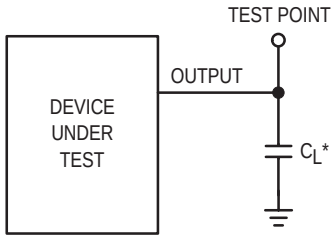
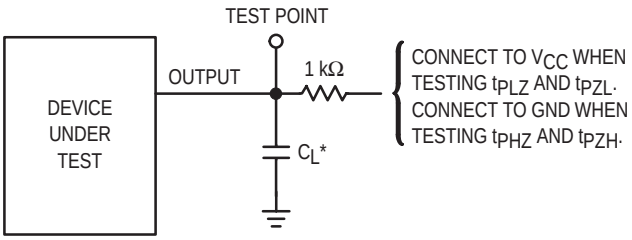


Figure 3.



* Includes all probe and jig capacitance

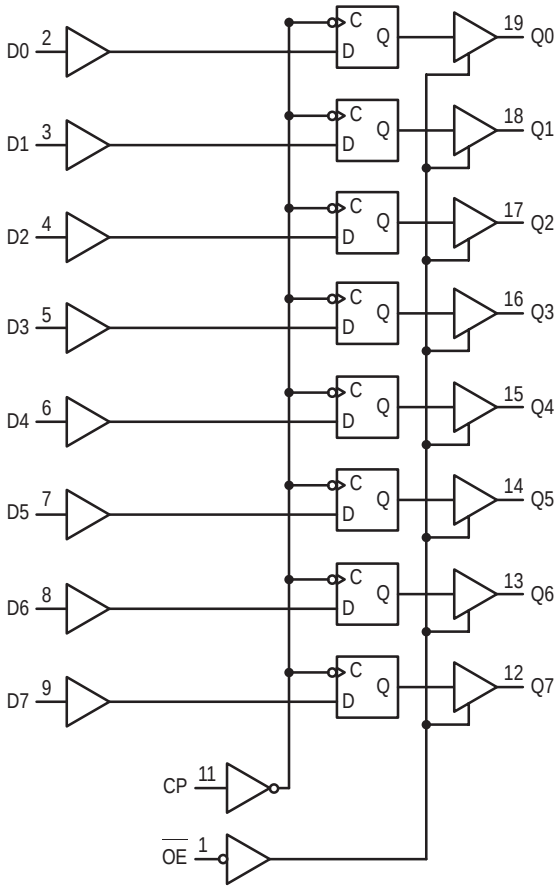
Figure 4.



* Includes all probe and jig capacitance

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



8-Bit Shift Register with Output Storage Register (3-State)

MC74VHC595

The MC74VHC595 is an advanced high speed 8–bit shift register with an output storage register fabricated with silicon gate CMOS technology.

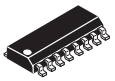
It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC595 contains an 8–bit static shift register which feeds an 8–bit storage register.

Shift operation is accomplished on the positive going transition of the Shift Clock input (SCK). The output register is loaded with the contents of the shift register on the positive going transition of the Register Clock input (RCK). Since the RCK and SCK signals are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3–state, the VHC595 can be directly connected to an 8–bit bus. This register can be used in serial–to–parallel conversion, data receivers, etc.

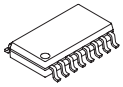
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: f_{max} = 185MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 1.0V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 328 FETs or 82 Equivalent Gates



D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

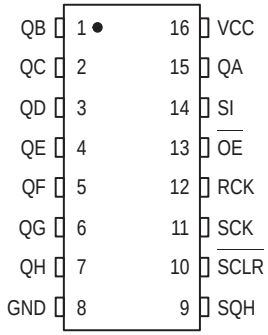


M SUFFIX
16–LEAD SOIC EIAJ PACKAGE
CASE 966–01

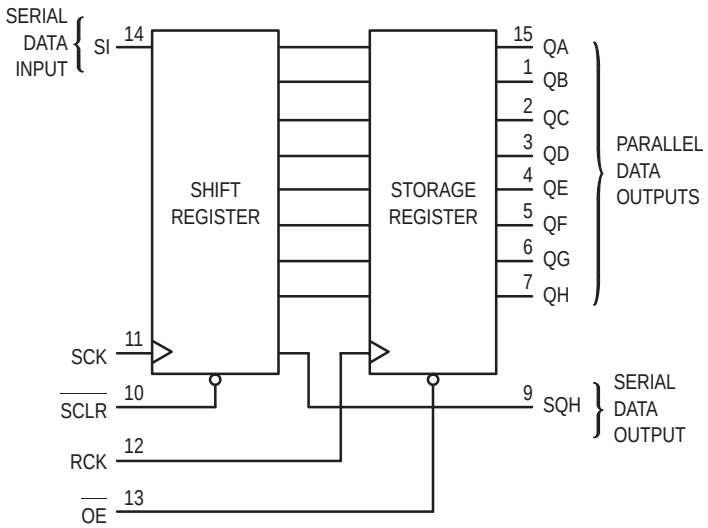
ORDERING INFORMATION

MC74VHCXXXD	SOIC
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset (SCLR)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable (OE)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA – QH)
Clear shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	$D \rightarrow SR_A$; $SR_N \rightarrow SR_{N+1}$	U	$SR_G \rightarrow SR_H$	U
Registers remains unchanged	H	X	L, H, ↓	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H, ↓	↑	L	U	$SR_N \rightarrow STR_N$	*	SR_N
Storage register remains unachanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents D = data (L, H) logic level ↓ = High–to–Low * = depends on Reset and Shift Clock inputs
STR = storage register contents U = remains unchanged ↑ = Low–to–High ** = depends on Register Clock input

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V	0	100	ns/V
		V_{CC} =5.0V ±0.5V	0	20	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	
I_{OZ}	Three–State Output Off–State Current	V_{in} = V_{IH} or V_{IL} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.50	μA
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF C_L = 50pF	80 55	150 130		70 50		MHz
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF	135 95	185 155		115 85		
t_{PLH}, t_{PHL}	Propagation Delay, SCK to SQH	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		8.8 11.3	13.0 16.5	1.0 1.0	15.0 18.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		6.2 7.7	8.2 10.2	1.0 1.0	9.4 11.4	
t_{PHL}	Propagation Delay, SCLR to SQH	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		8.4 10.9	12.8 16.3	1.0 1.0	13.7 17.2	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		5.9 7.4	8.0 10.0	1.0 1.0	9.1 11.1	
t_{PLH}, t_{PHL}	Propagation Delay, RCK to QA – QH	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		7.7 10.2	11.9 15.4	1.0 1.0	13.5 17.0	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		5.4 6.9	7.4 9.4	1.0 1.0	8.5 10.5	
t_{PZL}, t_{PZH}	Output Enable Time, OE to QA – QH	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF C_L = 50pF		7.5 9.0	11.5 15.0	1.0 1.0	13.5 17.0	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF C_L = 50pF		4.8 8.3	8.6 10.6	1.0 1.0	10.0 12.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = -40$ to $85°C$		Unit
			Min	Typ	Max	Min	Max	
t_{PLZ}, t_{PHZ}	Output Disable Time, OE to QA – QH	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 50pF$ $R_L = 1k\Omega$		12.1	15.7	1.0	16.2	ns
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$ $R_L = 1k\Omega$		7.6	10.3	1.0	11.0	
C_{in}	Input Capacitance			4	10		10	pF
C_{out}	Three–State Output Capacitance (Output in High–Impedance State), QA – QH			6			10	

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 1.)	87	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0V$)

Symbol	Characteristic	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.8	– 1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	V_{CC} V	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
t_{su}	Setup Time, SI to SCK	3.3 5.0		3.5 3.0	3.5 3.0	ns
$t_{su(H)}$	Setup Time, SCK to RCK	3.3 5.0		8.0 5.0	8.5 5.0	ns
$t_{su(L)}$	Setup Time, SCLR to RCK	3.3 5.0		8.0 5.0	9.0 5.0	ns
t_h	Hold Time, SI to SCK	3.3 5.0		1.5 2.0	1.5 2.0	ns
$t_{h(L)}$	Hold Time, SCLR to RCK	3.3 5.0		0 0	0 0	ns
t_{rec}	Recovery Time, $\overline{SCLR}$ to SCK	3.3 5.0		3.0 2.5	3.0 2.5	ns
t_w	Pulse Width, SCK or RCK	3.3 5.0		5.0 5.0	5.0 5.0	ns
$t_{w(L)}$	Pulse Width, $\overline{SCLR}$	3.3 5.0		5.0 5.0	5.0 5.0	ns

SWITCHING WAVEFORMS

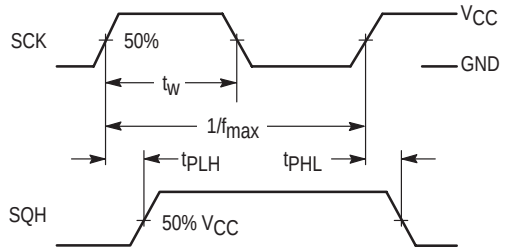


Figure 1.

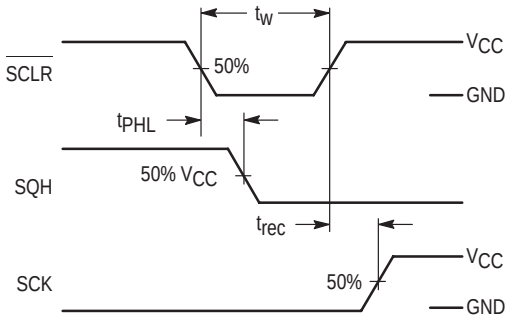


Figure 2.

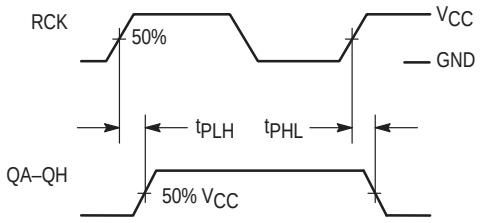
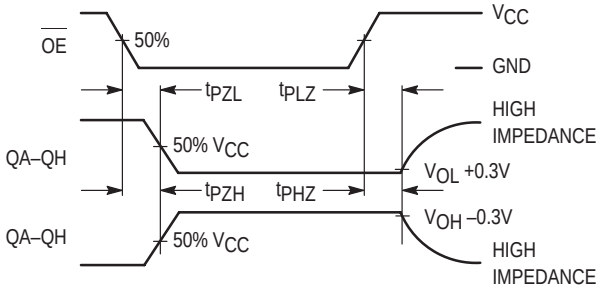


Figure 3.



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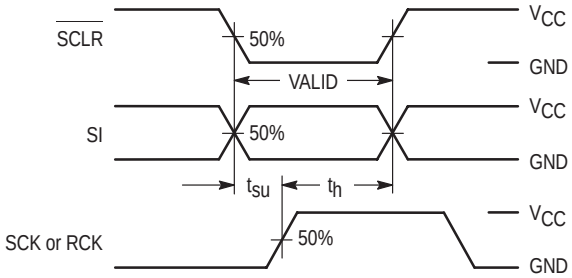

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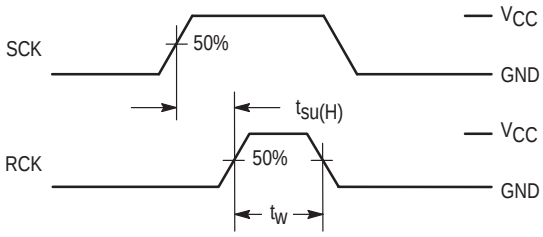
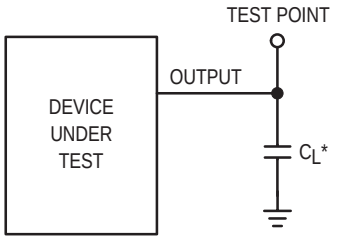


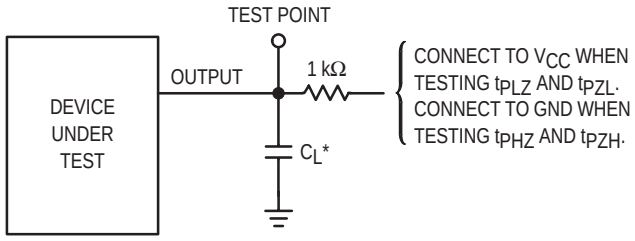
Figure 6.

TEST CIRCUITS



* Includes all probe and jig capacitance

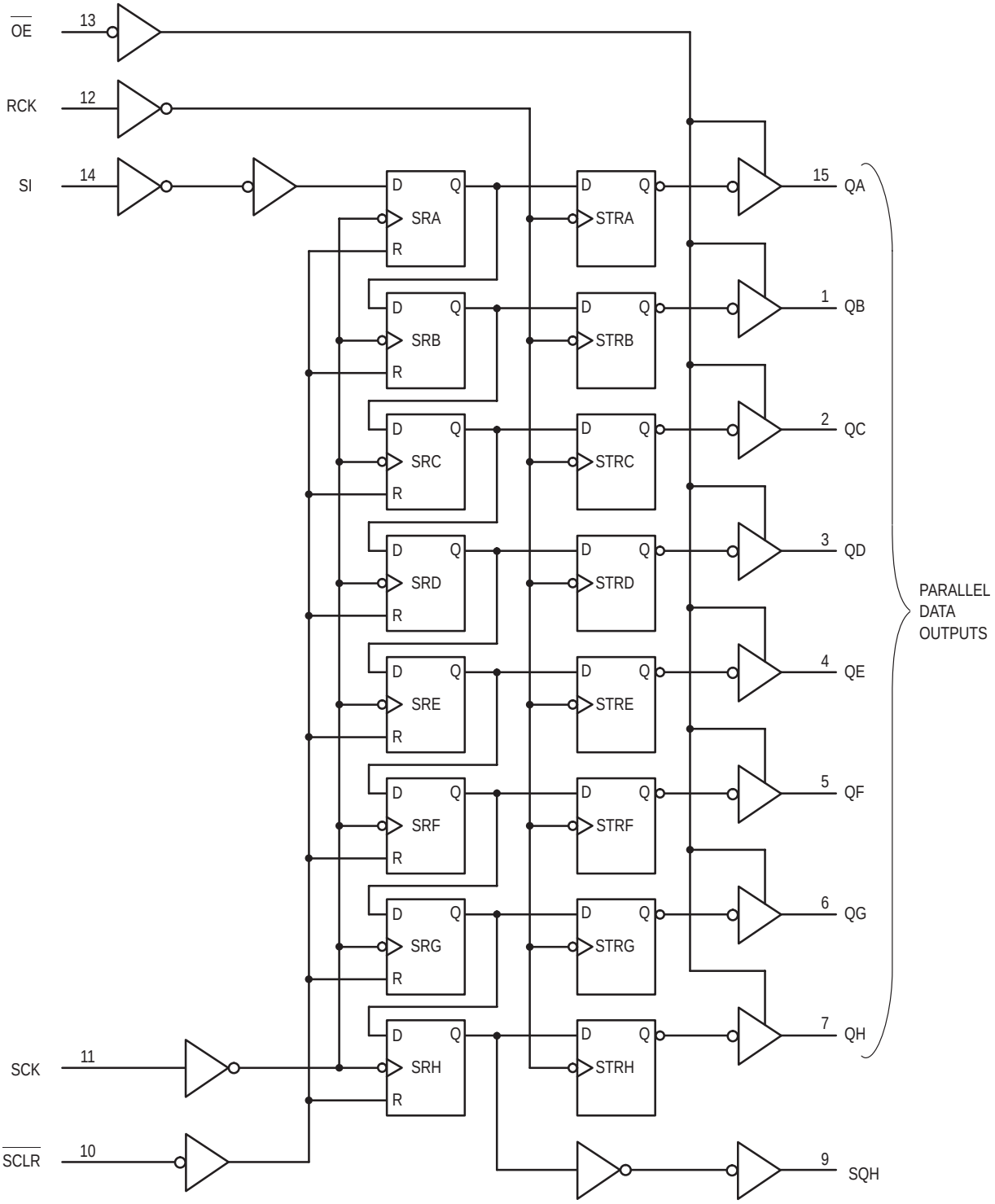
Figure 7.



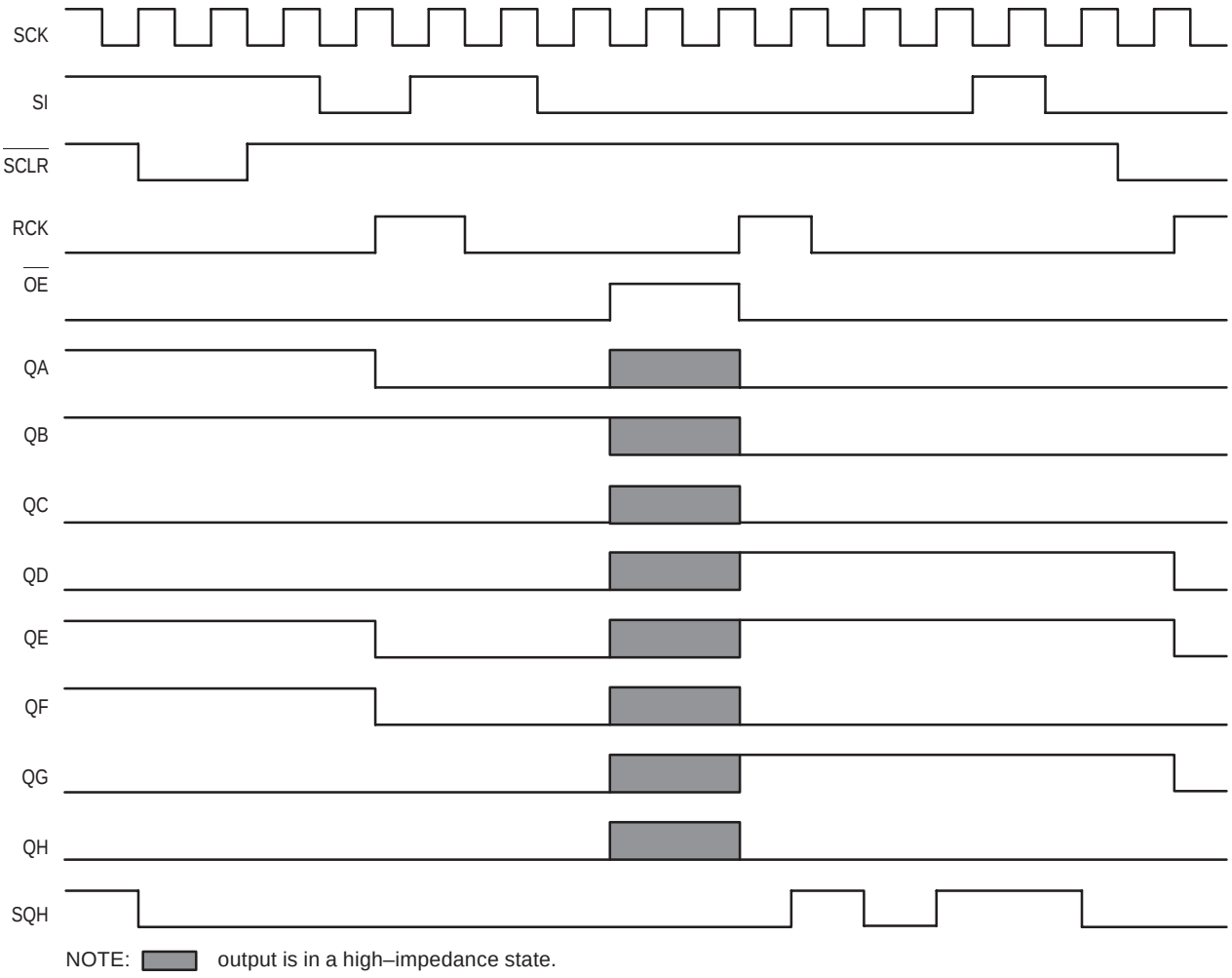
* Includes all probe and jig capacitance

Figure 8.

EXPANDED LOGIC DIAGRAM

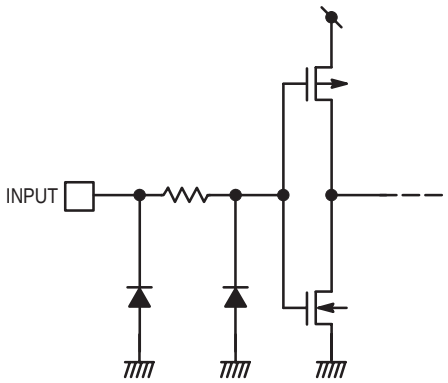


TIMING DIAGRAM



NOTE: output is in a high–impedance state.

INPUT EQUIVALENT CIRCUIT



Advance Information

Analog Multiplexers/ Demultiplexers

High–Performance Silicon–Gate CMOS

MC74VHC4051
MC74VHC4052
MC74VHC4053

The MC74VHC4051, MC74VHC4052 and MC74VHC4053 utilize silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/ demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The VHC4051, VHC4052 and VHC4053 are identical in pinout to the high–speed HC4051A, HC4052A and HC4053A, and the metal–gate MC14051B, MC14052B and MC14053B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

For a multiplexer/demultiplexer with channel–select latches, see VHC4351.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: VHC4051 — 184 FETs or 46 Equivalent Gates
  VHC4052 — 168 FETs or 42 Equivalent Gates
  VHC4053 — 156 FETs or 39 Equivalent Gates

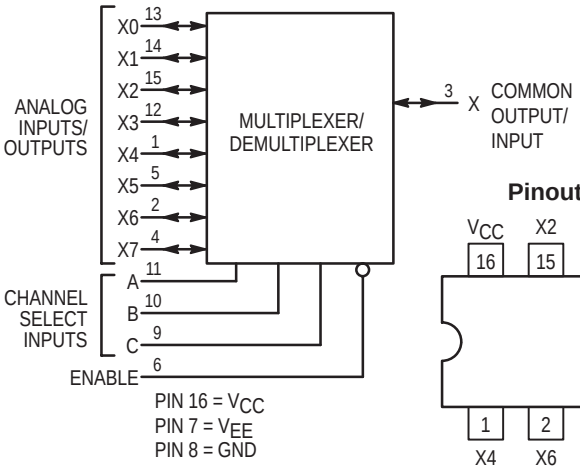
D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

ORDERING INFORMATION

MC74VHCXXXXD	SOIC
MC74VHCXXXXDT	TSSOP

LOGIC DIAGRAM
MC74VHC4051
Single–Pole, 8–Position Plus Common Off

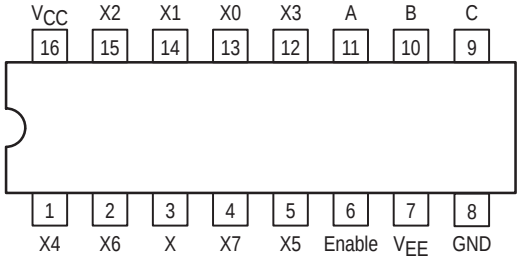


FUNCTION TABLE – MC74VHC4051

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

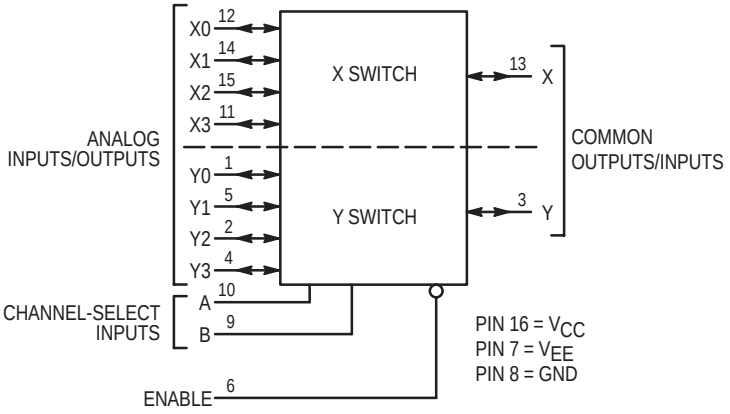
X = Don't Care

Pinout: MC74VHC4051 (Top View)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM
MC74VHC4052
Double–Pole, 4–Position Plus Common Off

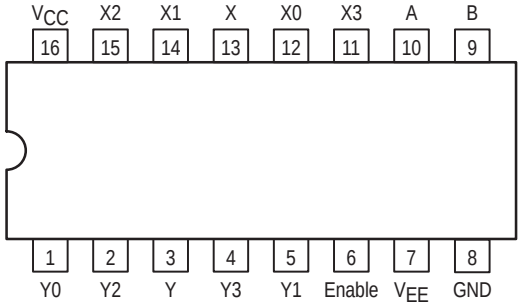


FUNCTION TABLE – MC74VHC4052

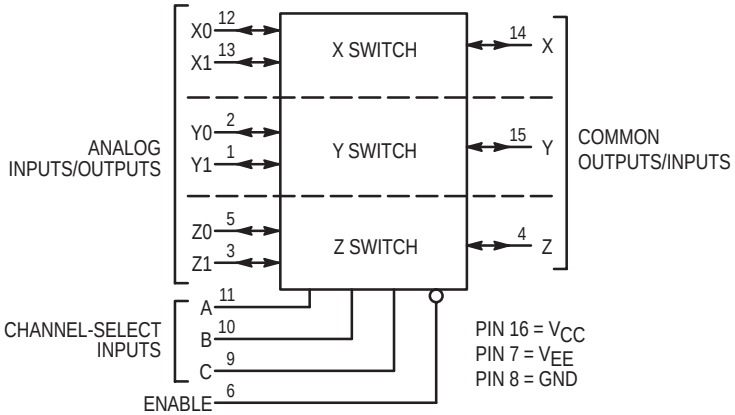
Control Inputs			
Enable	Select B	Select A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

Pinout: MC74VHC4052 (Top View)



LOGIC DIAGRAM
MC74VHC4053
Triple Single–Pole, Double–Position Plus Common Off



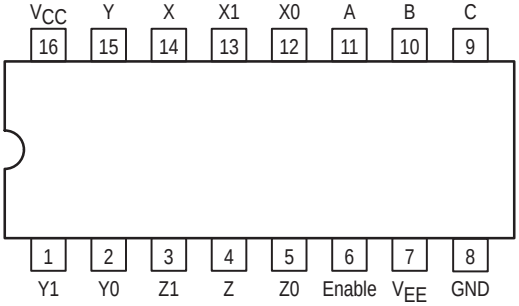
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

FUNCTION TABLE – MC74VHC4053

Control Inputs				
Enable	Select C	Select B	Select A	ON Channels
L	L	L	L	Z0 Y0 X0
L	L	L	H	Z0 Y0 X1
L	L	H	L	Z0 Y1 X0
L	L	H	H	Z0 Y1 X1
L	H	L	L	Z1 Y0 X0
L	H	L	H	Z1 Y0 X1
L	H	H	L	Z1 Y1 X0
L	H	H	H	Z1 Y1 X1
H	X	X	X	NONE

X = Don't Care

Pinout: MC74VHC4053 (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})		2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch			1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 800 500 400	ns

* For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{EE} = GND V_{IO} = 0 V V_{EE} = – 6.0	 6.0 6.0	 1 4	 10 40	 40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to V_{EE} I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	TBD 190 120 100	TBD 240 150 125	TBD 280 170 140	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	TBD 150 100 80	TBD 190 125 100	TBD 230 140 115	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) I_S ≤ 2.0 mA	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	TBD 30 12 10	TBD 35 15 12	TBD 40 18 14	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} – V_{EE}; Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel VHC4051 VHC4052 VHC4053	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} – V_{EE}; Switch Off (Figure 4)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel VHC4051 VHC4052 VHC4053	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} – V_{EE}; (Figure 5)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	370 TBD 74 63	465 TBD 93 79	550 TBD 110 94	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	60 TBD 12 10	75 TBD 15 13	90 TBD 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	290 TBD 58 49	364 TBD 73 62	430 TBD 86 73	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	345 TBD 69 59	435 TBD 87 74	515 TBD 103 87	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O		35	35	35	pF
	(All Switches Off) — Common O/I: VHC4051 VHC4052 VHC4053		130 80 50	130 80 50	130 80 50	
	Feedthrough		1.0	1.0	1.0	

			Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Figure 13)*	VHC4051 VHC4052 VHC4053	45 80 45	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C '51	Limit* 25°C '52	Limit* 25°C '53	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	2.25	–2.25	80	95	120	MHz
			4.50	–4.50	80	95	120	
			6.00	–6.00	80	95	120	
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25	–2.25	–50			dB
			4.50	–4.50	–50			
			6.00	–6.00	–50			
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25	–2.25	–40			
			4.50	–4.50	–40			
			6.00	–6.00	–40			
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V_{in} ≤ 1MHz Square Wave (t_r = t_f = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	2.25	–2.25	25			mV_{PP}
			4.50	–4.50	105			
			6.00	–6.00	135			
		R_L = 10kΩ, C_L = 10pF	2.25	–2.25	35			
			4.50	–4.50	145			
			6.00	–6.00	190			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to VHC4051)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25	–2.25	–50			dB
			4.50	–4.50	–50			
			6.00	–6.00	–50			
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25	–2.25	–60			
			4.50	–4.50	–60			
			6.00	–6.00	–60			
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF THD = $THD_{measured}$ – THD_{source} V_{IS} = 4.0V_{PP} sine wave	2.25	–2.25	0.10			%
		V_{IS} = 8.0V_{PP} sine wave	4.50	–4.50	0.08			
		V_{IS} = 11.0V_{PP} sine wave	6.00	–6.00	0.05			

* Limits not tested. Determined by design and verified by qualification.

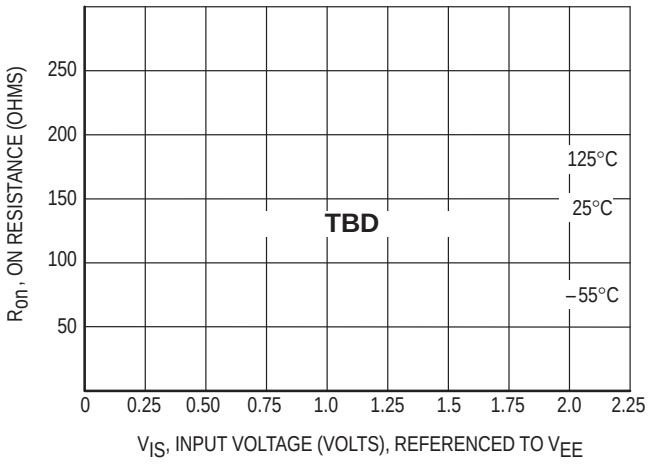


Figure 1a. Typical On Resistance, V_{CC} – V_{EE} = 2.0 V

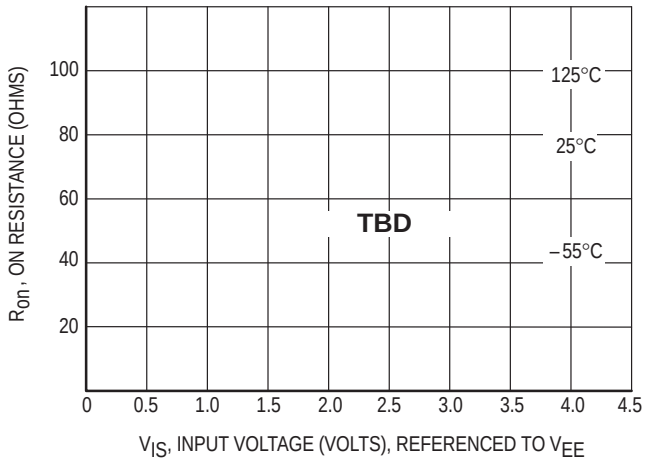


Figure 1b. Typical On Resistance, V_{CC} – V_{EE} = 3.0 V

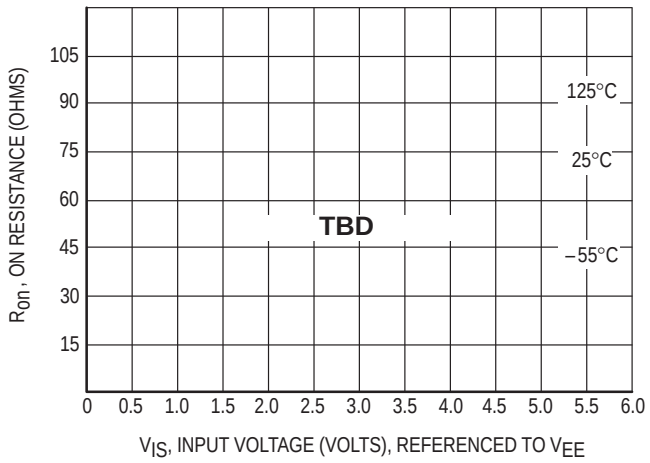


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

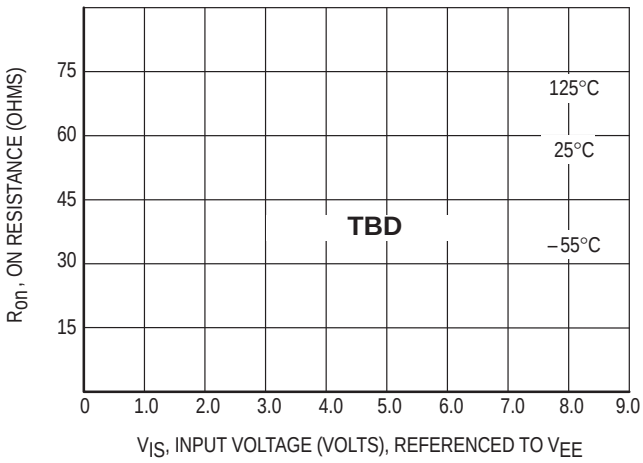


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

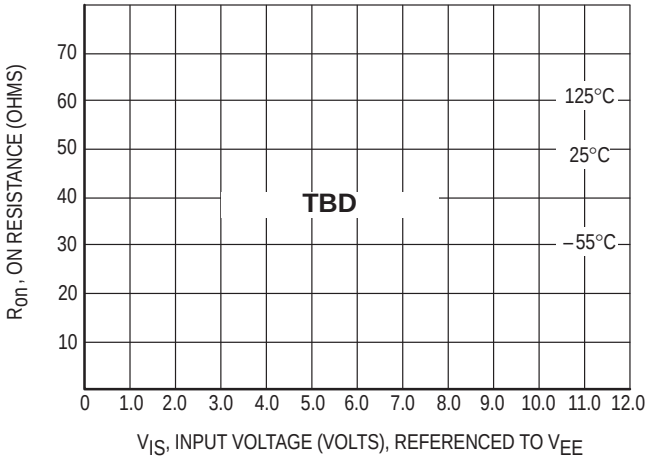


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

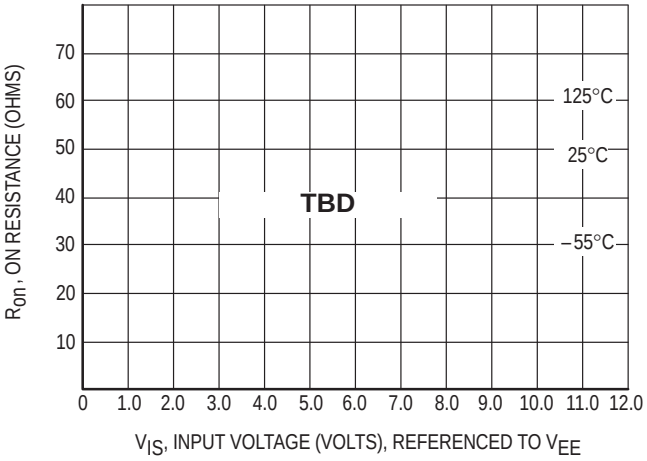


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

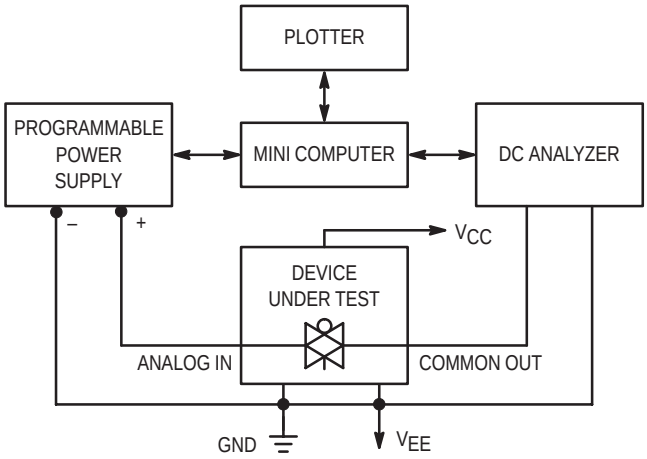


Figure 2. On Resistance Test Set–Up

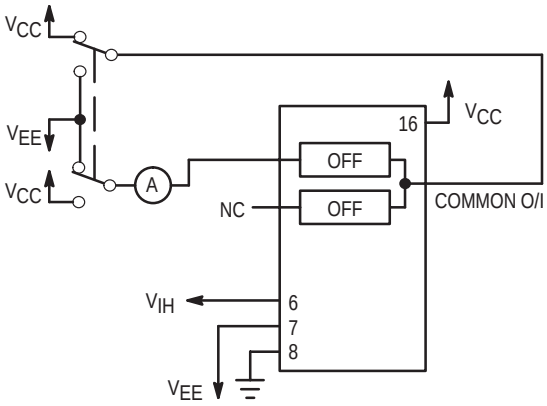


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

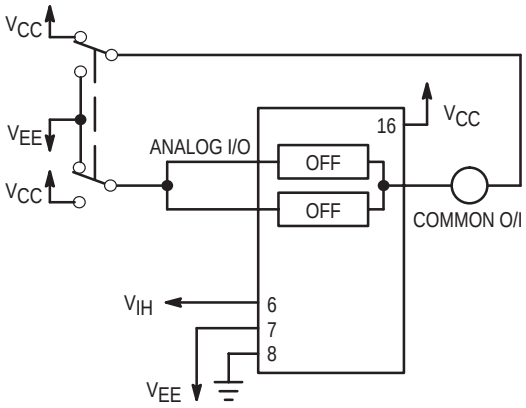


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

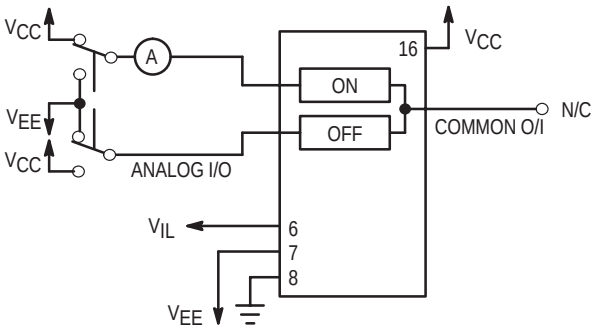


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

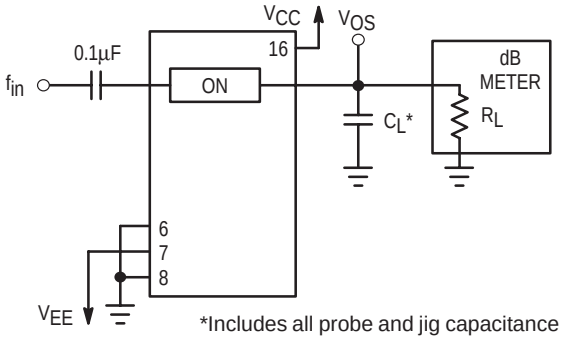


Figure 6. Maximum On Channel Bandwidth, Test Set–Up

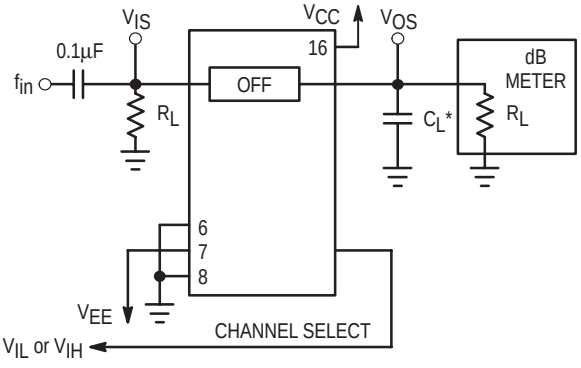


Figure 7. Off Channel Feedthrough Isolation, Test Set–Up

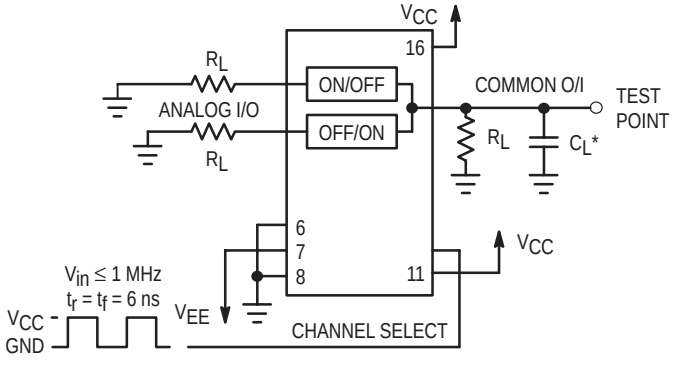


Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

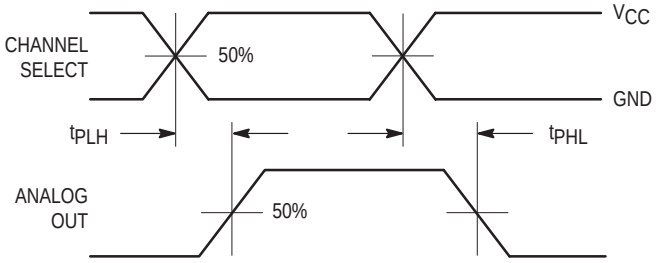
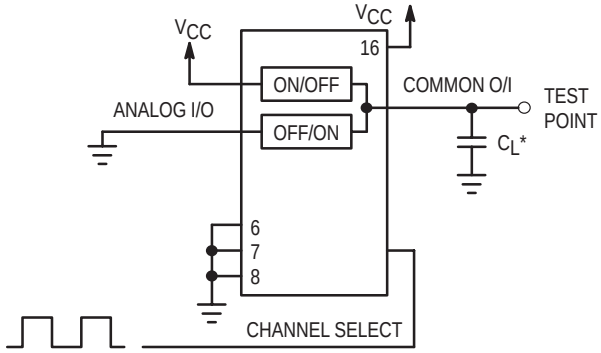


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

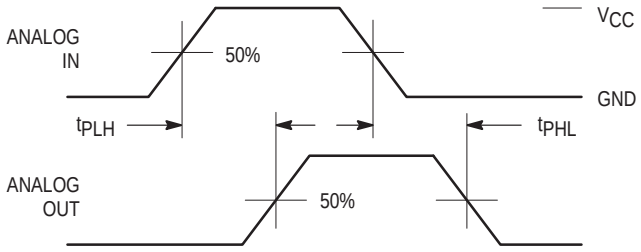
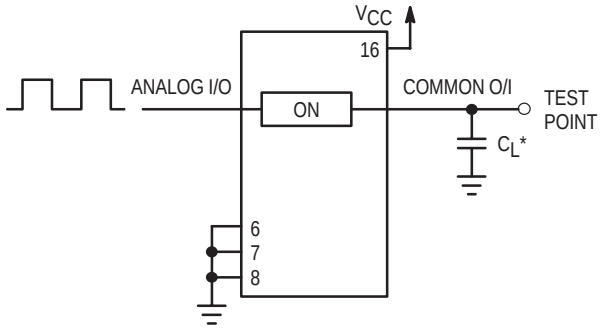


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

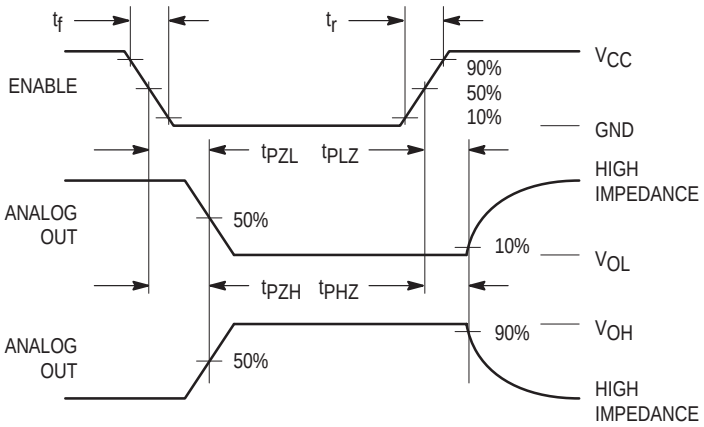


Figure 11a. Propagation Delays, Enable to Analog Out

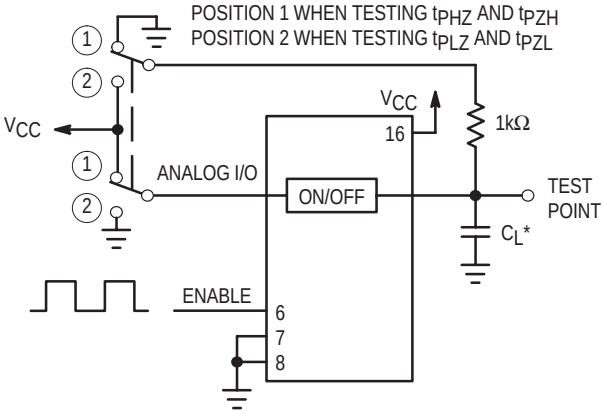
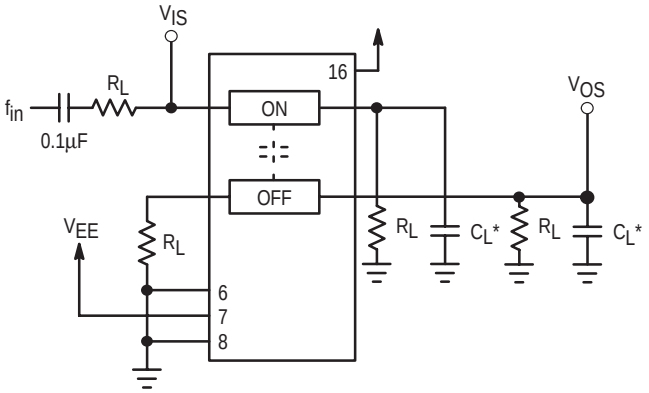


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

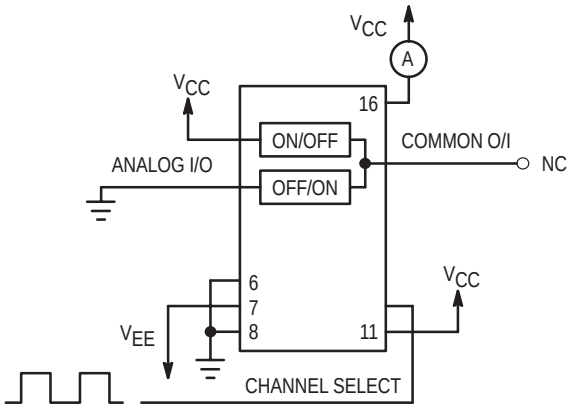
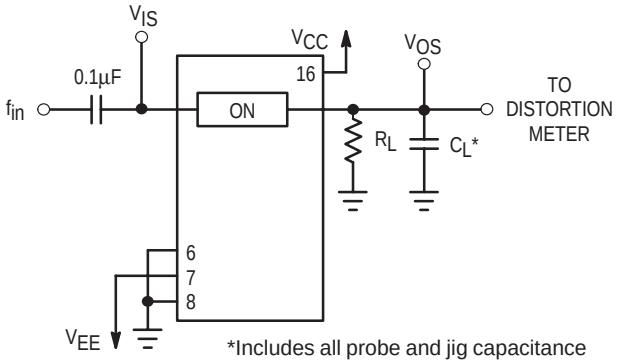


Figure 13. Power Dissipation Capacitance, Test Set–Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set–Up

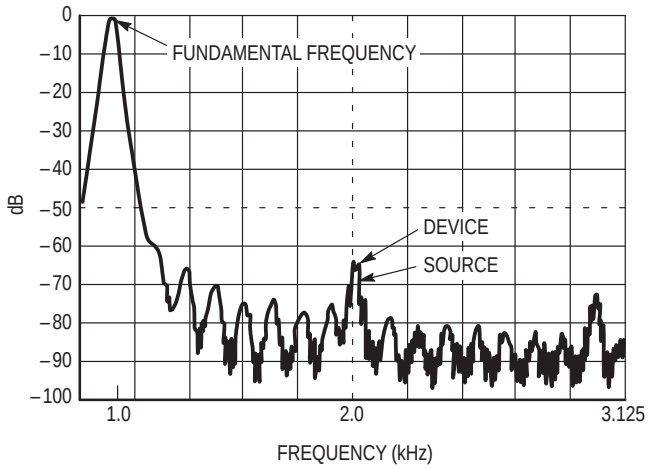


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts
V_{EE} – GND = 0 to –6 volts
V_{CC} – V_{EE} = 2 to 12 volts
and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

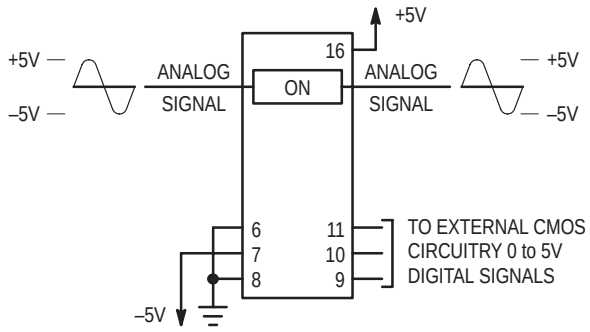


Figure 15. Application Example

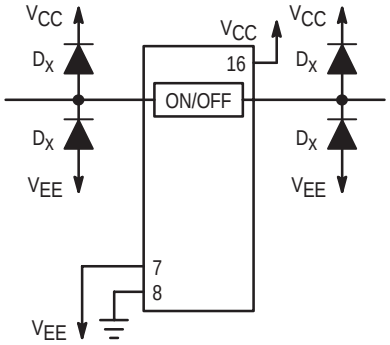
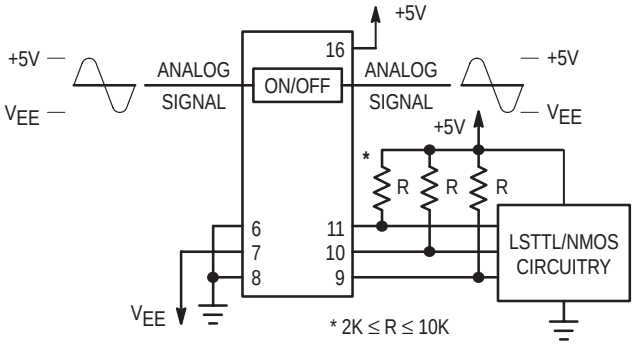
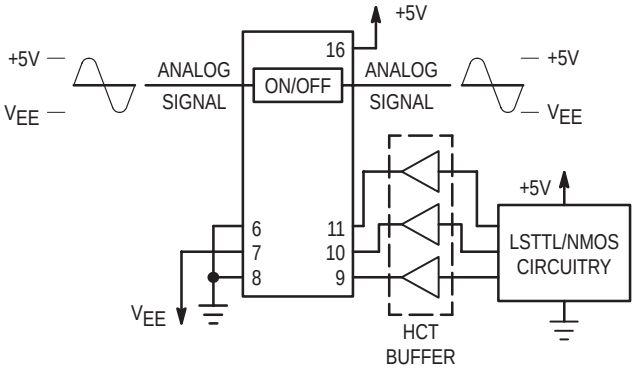


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

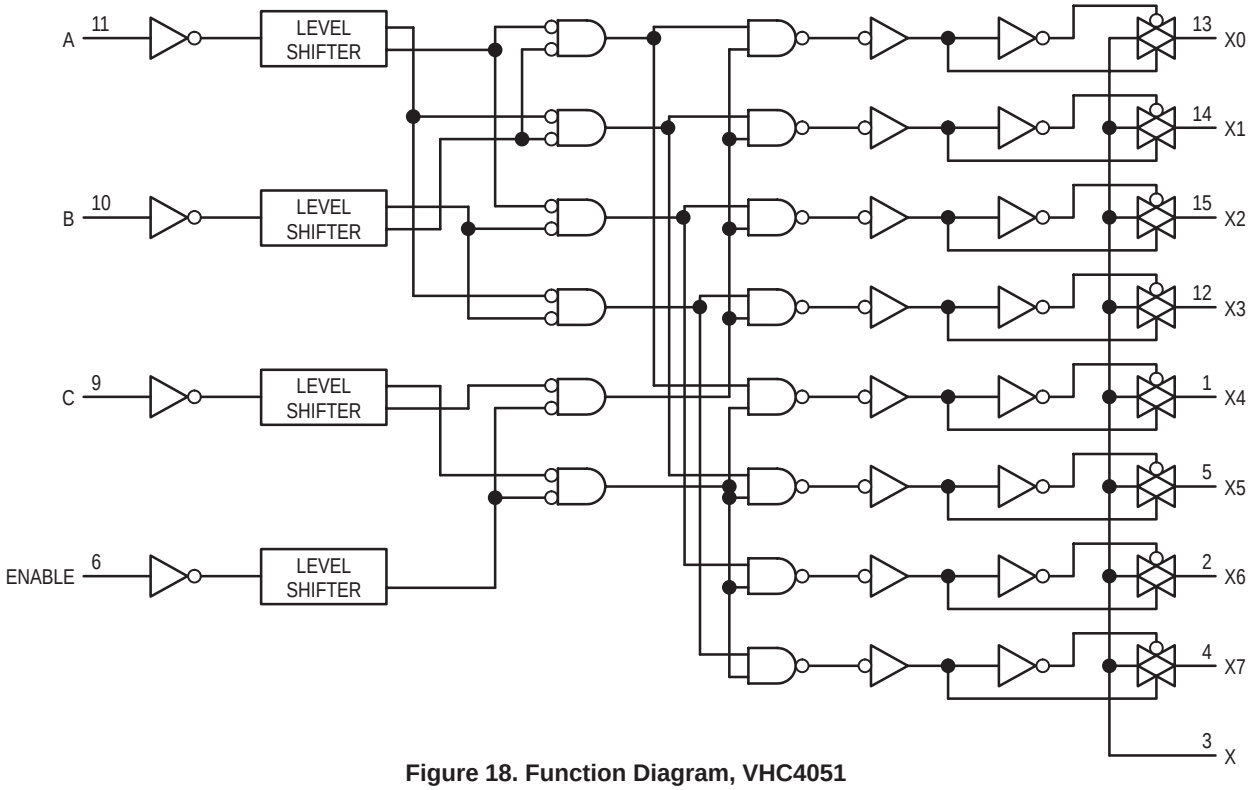


Figure 18. Function Diagram, VHC4051

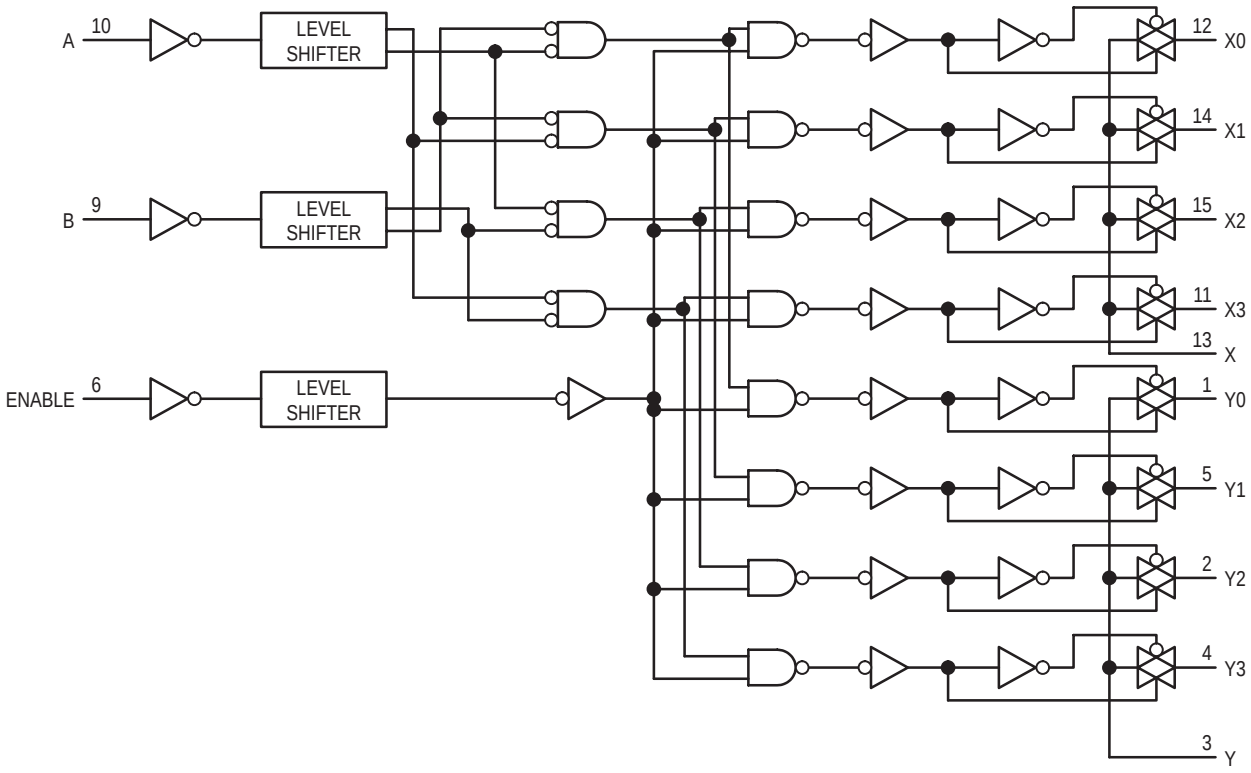


Figure 19. Function Diagram, VHC4052

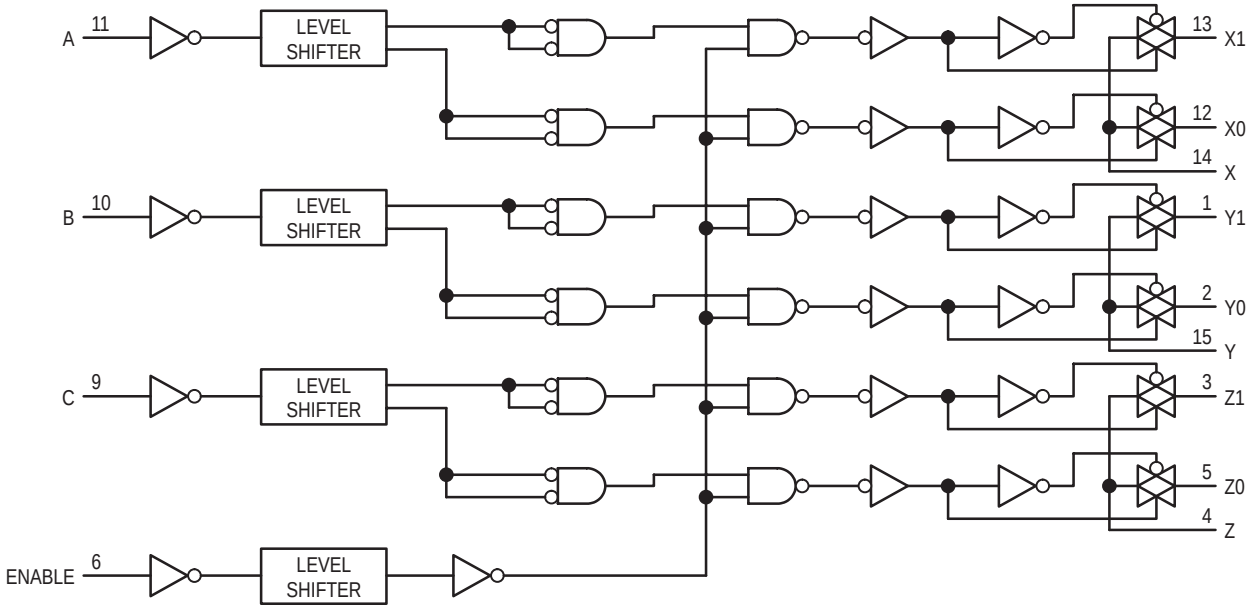


Figure 20. Function Diagram, VHC4053

Advance Information

Quad Analog Switch/ Multiplexer/Demultiplexer

High–Performance Silicon–Gate CMOS

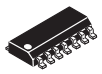
MC74VHC4066

The MC74VHC4066 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The VHC4066 is identical in pinout to the metal–gate CMOS MC14066 and the high–speed CMOS HC4066A. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage–level translators, see the VHC4316.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Analog Input Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates



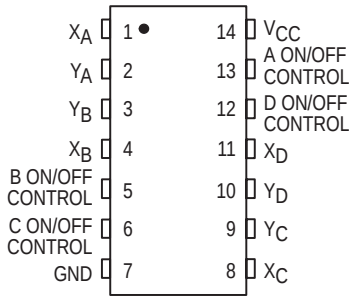
D SUFFIX
14–LEAD SOIC PACKAGE
CASE 751A–03

DT SUFFIX
14–LEAD TSSOP PACKAGE
CASE 948G–01

ORDERING INFORMATION

MC74VHCXXXXD	SOIC
MC74VHCXXXXDT	TSSOP

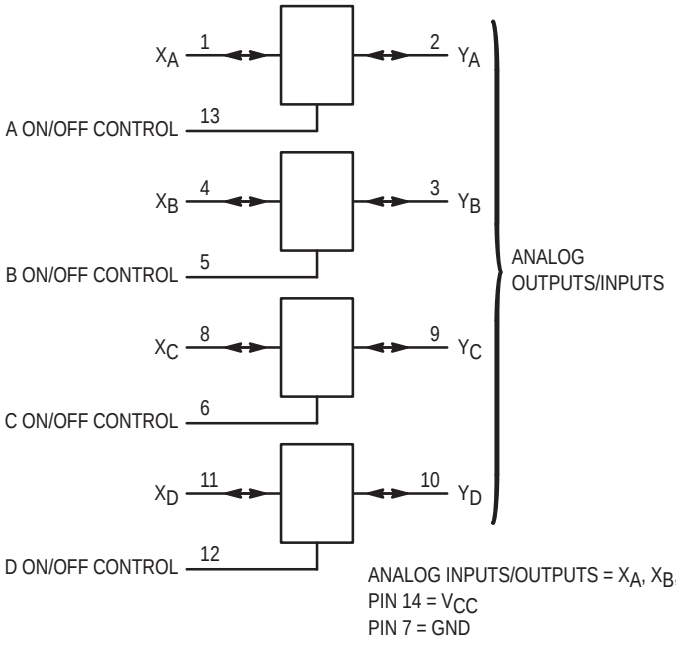
PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 14.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	V_{CC} = 2.0 V	0	1000	
	V_{CC} = 3.0 V	0	600	
	V_{CC} = 4.5 V	0	500	
	V_{CC} = 9.0 V	0	400	
	V_{CC} = 12.0 V	0	250	

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage ON/OFF Control Inputs	R_{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	V
V_{IL}	Maximum Low–Level Voltage ON/OFF Control Inputs	R_{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	V
I_{in}	Maximum Input Leakage Current ON/OFF Control Inputs	V_{in} = V_{CC} or GND	12.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V	6.0 12.0	2 4	20 40	40 160	µA

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_S \leq$ 2.0 mA (Figures 1, 2)	2.0† 3.0† 4.5 9.0 12.0	— — 120 70 70	— — 160 85 85	— — 200 100 100	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Endpoints) $I_S \leq$ 2.0 mA (Figures 1, 2)	2.0 3.0 4.5 9.0 12.0	— — 70 50 30	— — 85 60 60	— — 100 80 80	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ V_{IS} = 1/2 (V_{CC} – GND) $I_S \leq$ 2.0 mA	2.0 4.5 9.0 12.0	— 20 15 15	— 25 20 20	— 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC}) approaching 3 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 3.0 4.5 9.0 12.0	40 30 5 5 5	50 40 7 7 7	60 50 8 8 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 9.0 12.0	80 60 20 20 20	90 70 25 25 25	110 80 35 35 35	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 1 1)	2.0 3.0 4.5 9.0 12.0	80 45 20 20 20	90 50 25 25 25	100 60 30 30 30	ns
C	Maximum Capacitance — ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 — —	 35 1.0	 35 1.0	 35 1.0	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC} V	Limit* 25°C 74HC	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	4.5 9.0 12.0	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 4.5 9.0 12.0	 0.10 0.06 0.04	%

* Guaranteed limits not tested. Determined by design and verified by qualification.

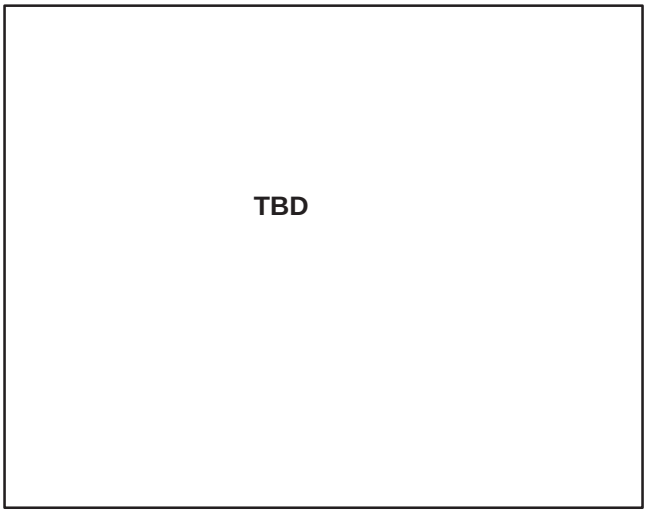


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V

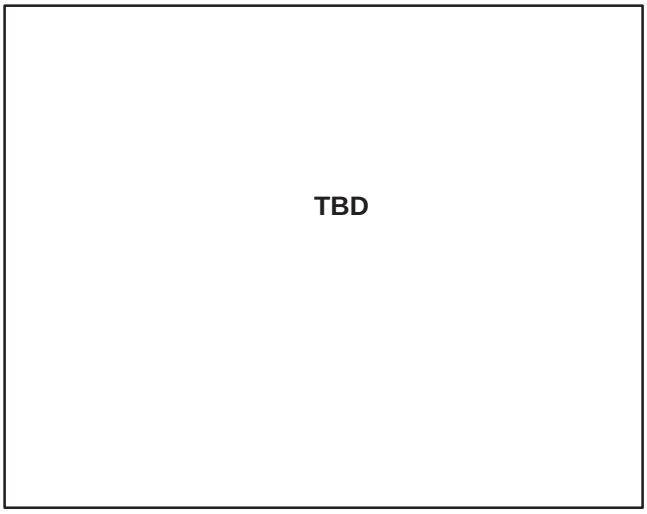


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

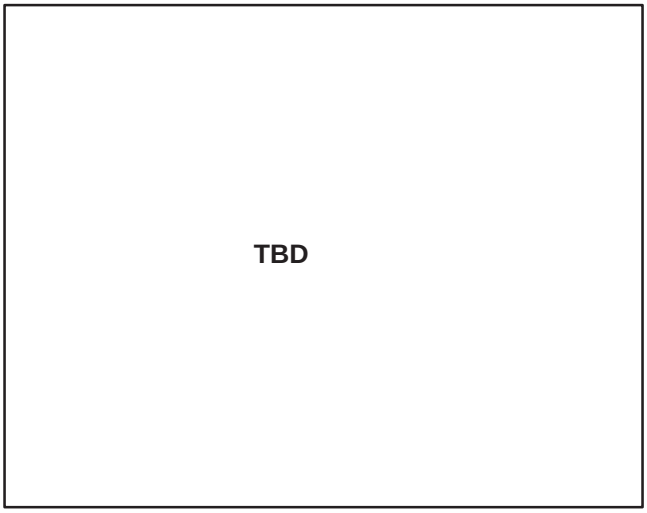


Figure 1c. Typical On Resistance, V_{CC} = 6.0 V

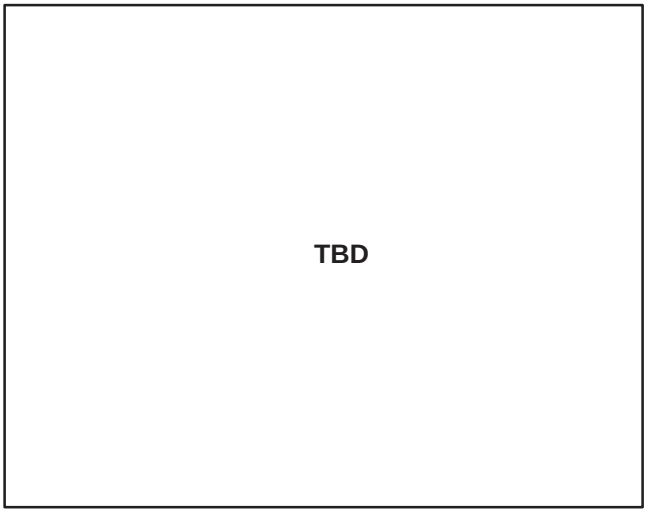


Figure 1d. Typical On Resistance, V_{CC} = 9.0 V

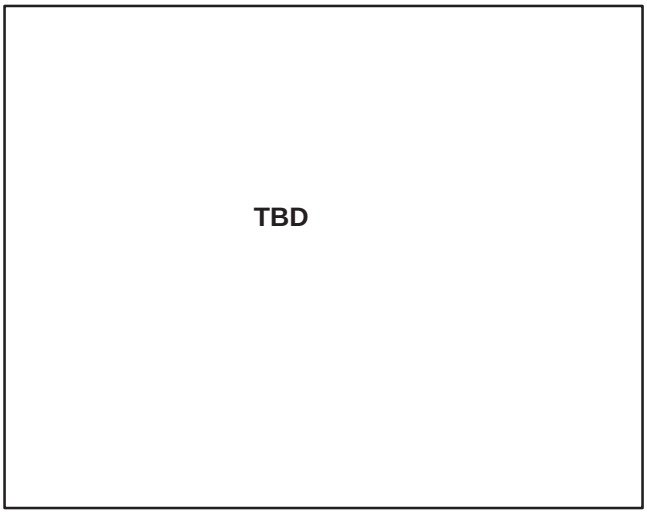


Figure 1e. Typical On Resistance, V_{CC} = 12 V

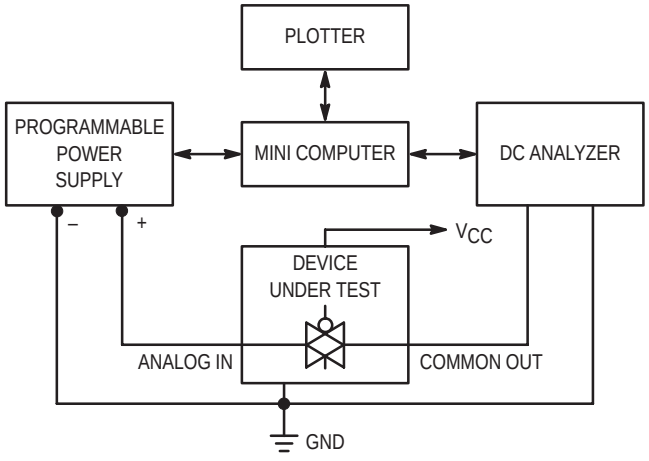


Figure 2. On Resistance Test Set–Up

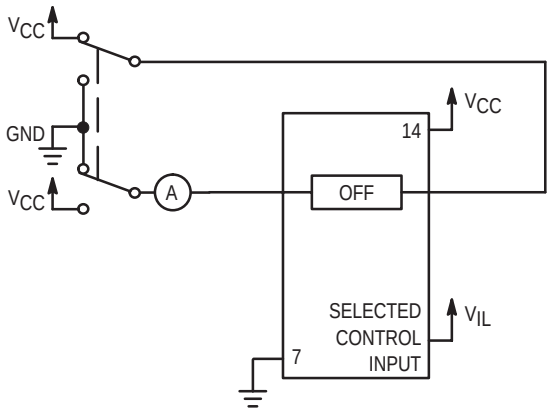


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

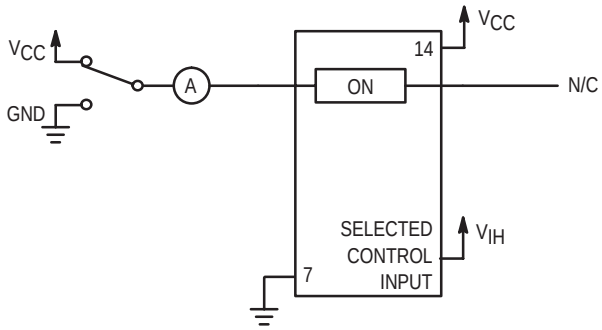
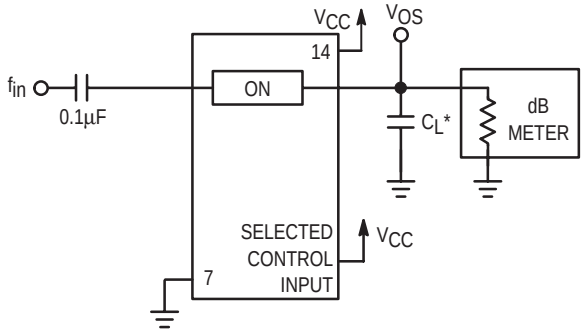
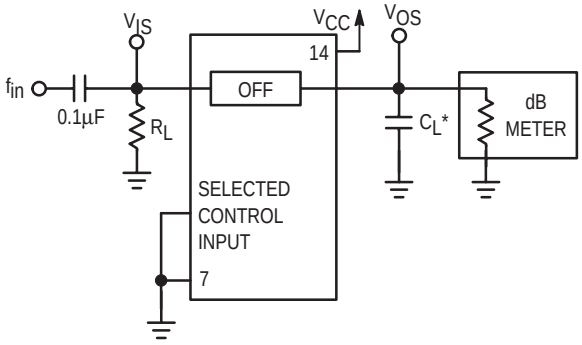


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



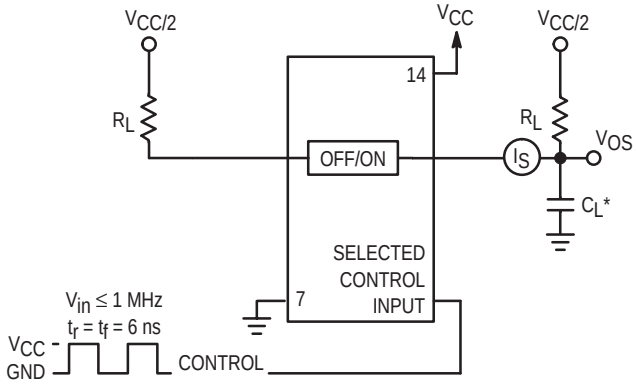
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

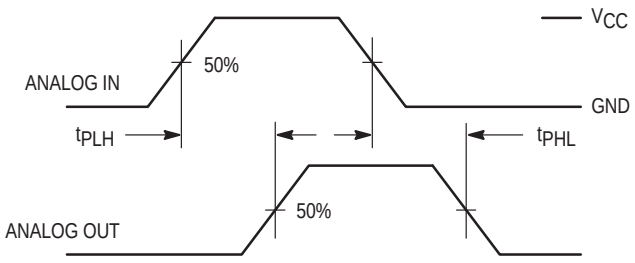
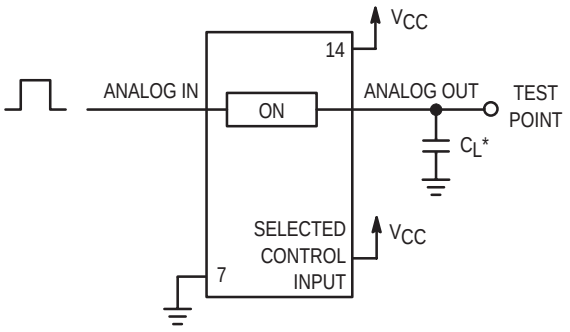


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

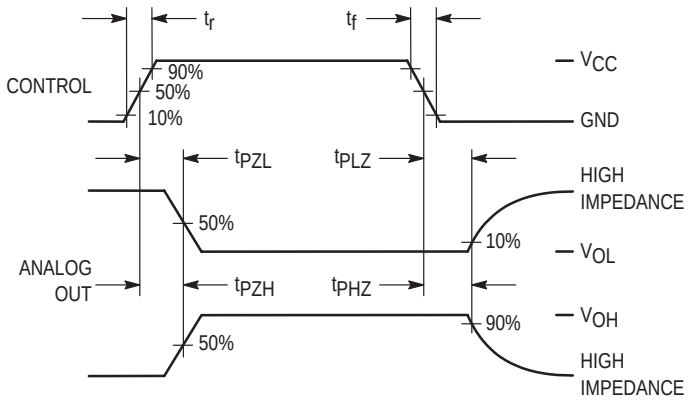
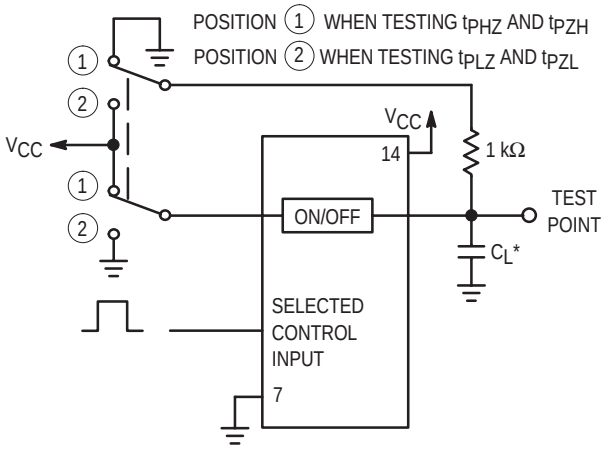
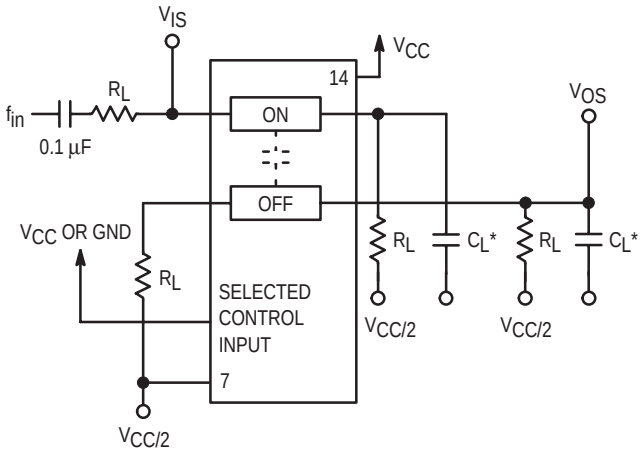


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

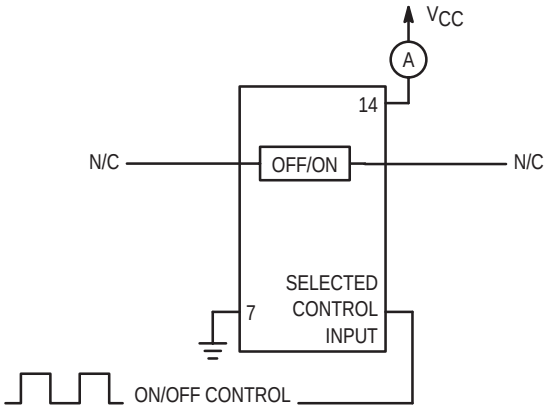
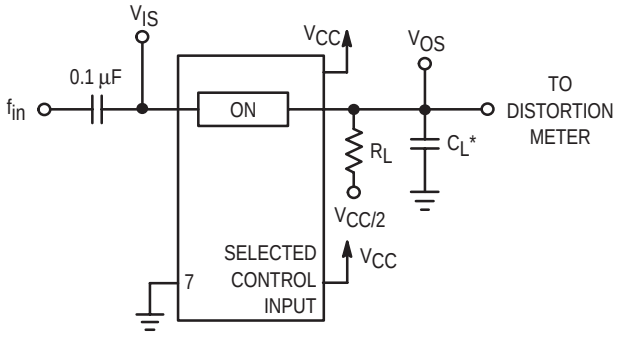


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

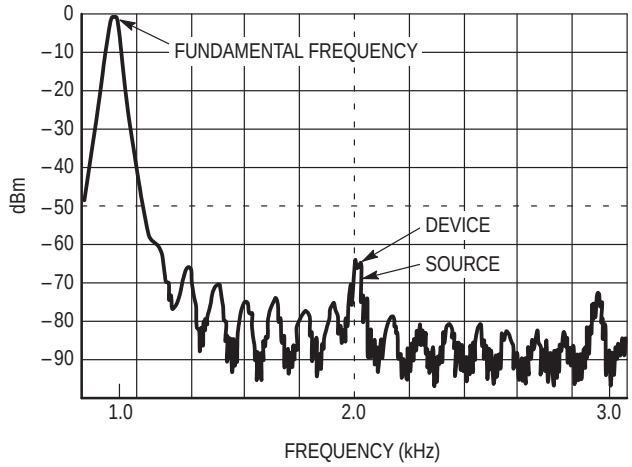


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked–up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn–on devices ideally suited for precise DC protection with no inherent wear out mechanism.

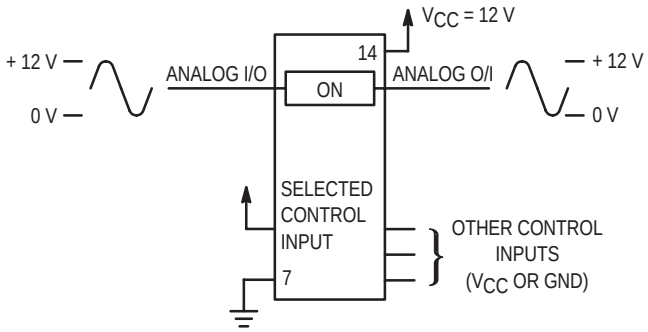


Figure 16. 12 V Application

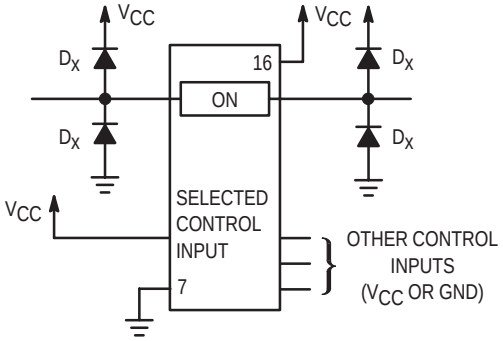
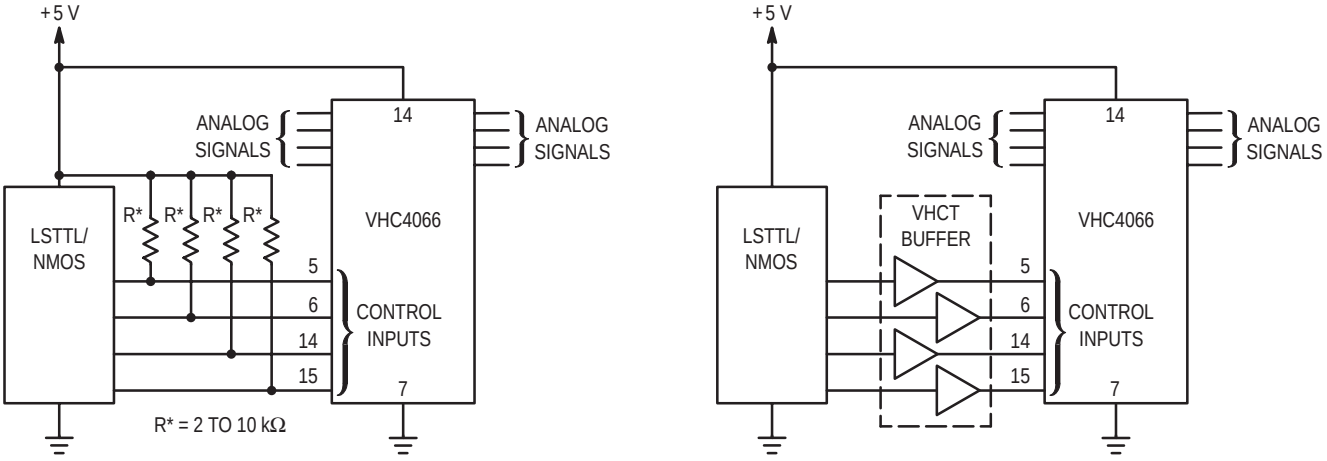


Figure 17. Transient Suppressor Application



a. Using Pull-Up Resistors **b. Using HCT Buffer**

Figure 18. LSTTL/NMOS to HCMOS Interface

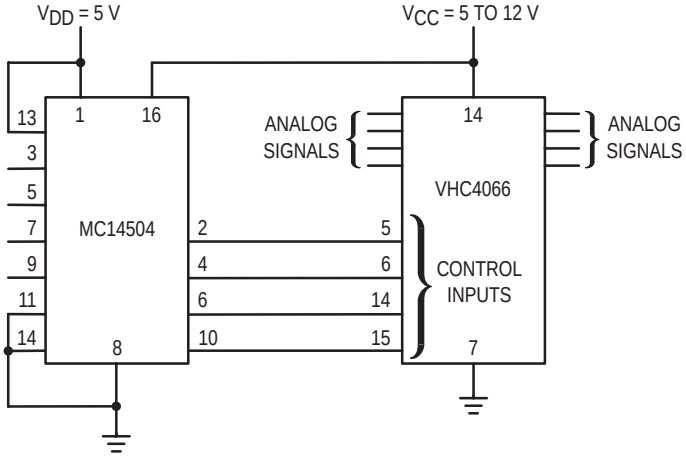


Figure 19. TTL/NMOS–to–CMOS Level Converter Analog Signal Peak–to–Peak Greater than 5 V (Also see VHC4316)

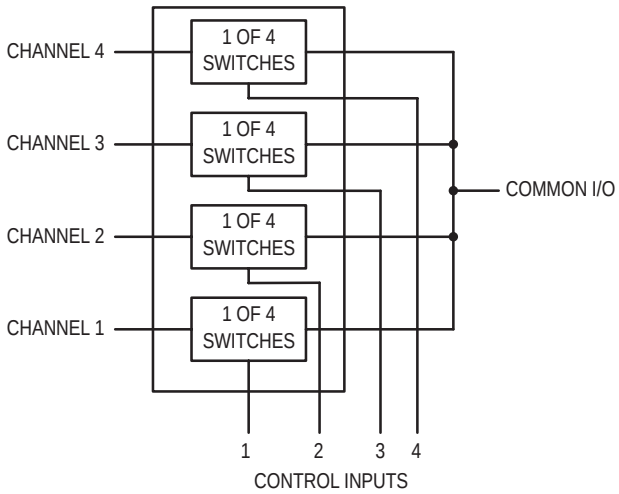


Figure 20. 4–Input Multiplexer

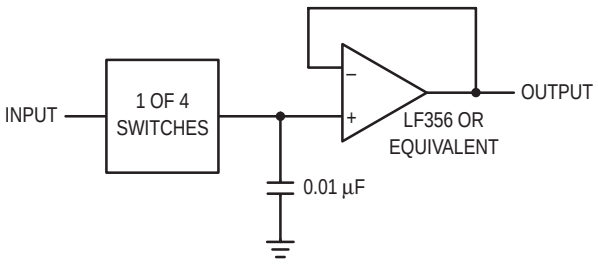


Figure 21. Sample/Hold Amplifier

Advance Information

MC74VHC4316

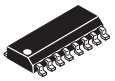
Quad Analog Switch/Multiplexer/ Demultiplexer with Separate Analog and Digital Power Supplies

High–Performance Silicon–Gate CMOS

The MC74VHC4316 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power–supply range (from V_{CC} to V_{EE}).

The VHC4316 is similar in function to the VHC4066, the metal–gate CMOS MC14016 and MC14066, and to the High–Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches. Logic–level translators are provided so that the On/Off Control and Enable logic–level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active–low) is high, all four analog switches are turned off.

- Logic–Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power–Supply Voltage Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 Volts
- Digital (Control) Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates



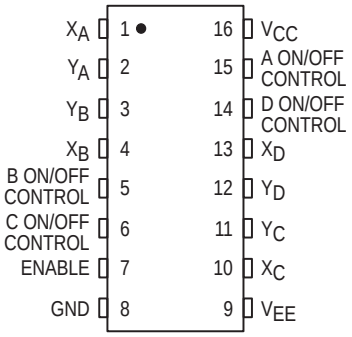
D SUFFIX
16–LEAD SOIC PACKAGE
CASE 751B–05

DT SUFFIX
16–LEAD TSSOP PACKAGE
CASE 948F–01

ORDERING INFORMATION

MC74VHCXXXXD	SOIC
MC74VHCXXXXDT	TSSOP

PIN ASSIGNMENT

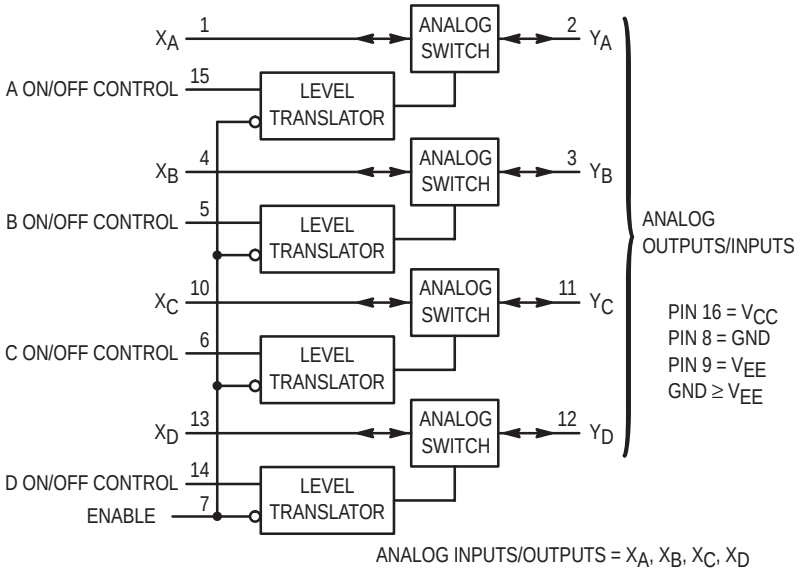


FUNCTION TABLE

Inputs		State of Analog Switch
Enable	On/Off Control	
L	H	On
L	L	Off
H	X	Off

X = don't care

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage		V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)		– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin		± 25	mA
P_D	Power Dissipation in Still Air	SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature		– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND)		2.0	6.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		—	1.2	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Control or Enable Inputs	V_{in} = V_{CC} or GND V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = – 6.0	 6.0 6.0	 2 4	 20 40	 40 160	µA

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to V_{EE} $I_S \leq$ 2.0 mA (Figures 1, 2)	2.0* 3.0 4 5 4.5 6.0	0.0 0.0 0.0 – 4.5 – 6.0	— TBD 160 90 90	— TBD 200 110 110	— TBD 240 130 130	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq$ 2.0 mA (Figures 1, 2)	2.0 3.0 4.5 4.5 6.0	0.0 0.0 0.0 – 4.5 – 6.0	— TBD 90 70 70	— TBD 115 90 90	— TBD 140 105 105	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ $V_{IS} = 1/2 (V_{CC} - V_{EE})$ $I_S \leq$ 2.0 mA	2.0 3.0 4.5 4.5 6.0	0.0 0.0 0.0 – 4.5 – 6.0	— TBD 20 15 15	— TBD 25 20 20	— TBD 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or V_{EE} Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	µA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Figure 4)	6.0	– 6.0	0.1	0.5	1.0	µA

* At supply voltage ($V_{CC} - V_{EE}$) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, V_{EE} = GND)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 3.0 4.5 6.0	40 TBD 6 5	50 TBD 8 7	60 TBD 9 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 6.0	130 TBD 40 30	160 TBD 50 40	200 TBD 60 50	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 6.0	140 TBD 40 30	175 TBD 50 40	250 TBD 60 50	ns
C	Maximum Capacitance — ON/OFF Control and Enable Inputs	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 — —	 35 1.0	 35 1.0	 35 1.0	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$				%
		V_{IS} = 4.0 V_{PP} sine wave	2.25	– 2.25	0.10	
		V_{IS} = 8.0 V_{PP} sine wave	4.50	– 4.50	0.06	
		V_{IS} = 11.0 V_{PP} sine wave	6.00	– 6.00	0.04	

* Limits not tested. Determined by design and verified by qualification.

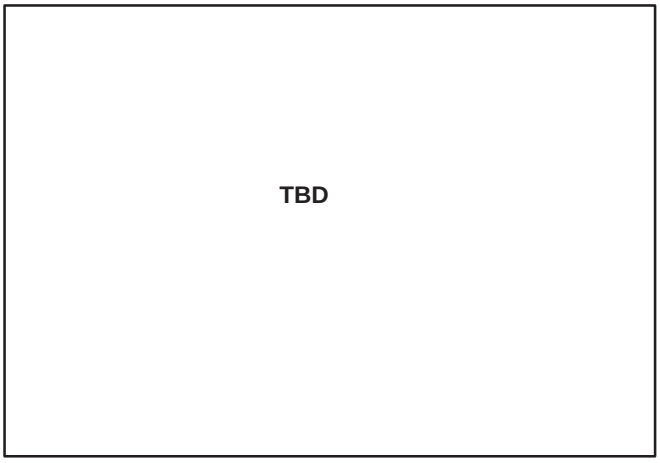


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V

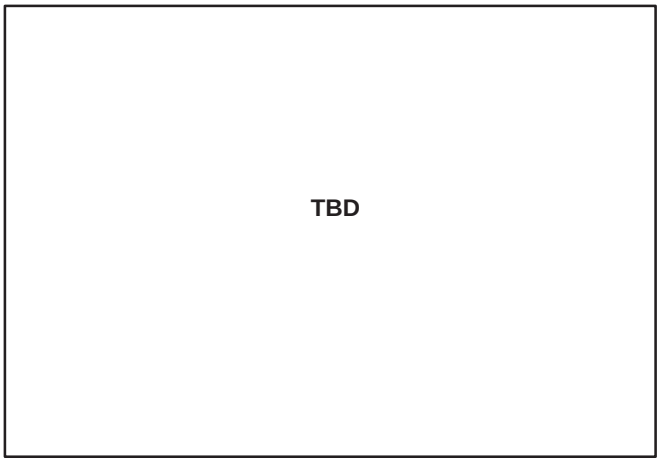


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 3.0 V

TBD

Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

TBD

Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

TBD

Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

TBD

Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

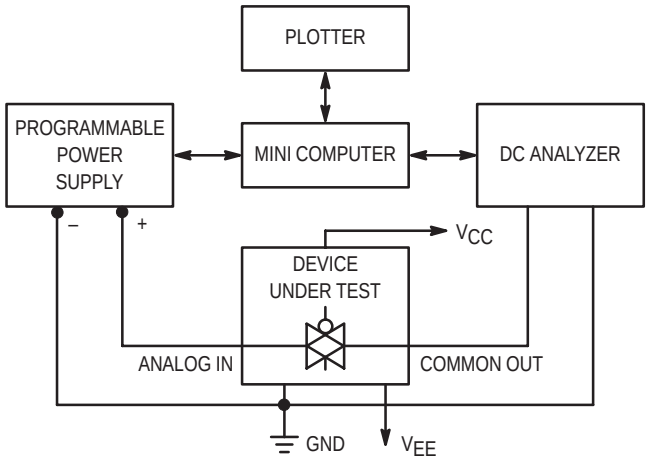


Figure 2. On Resistance Test Set–Up

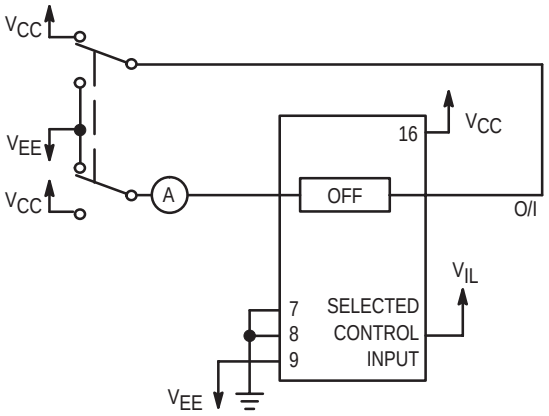


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

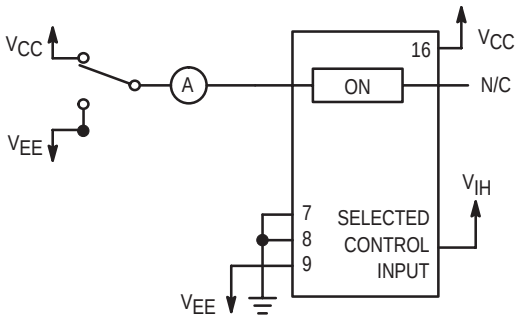
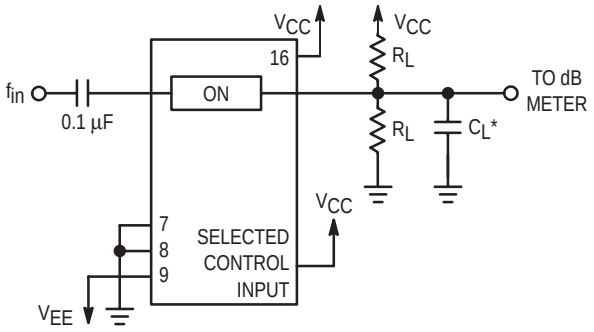
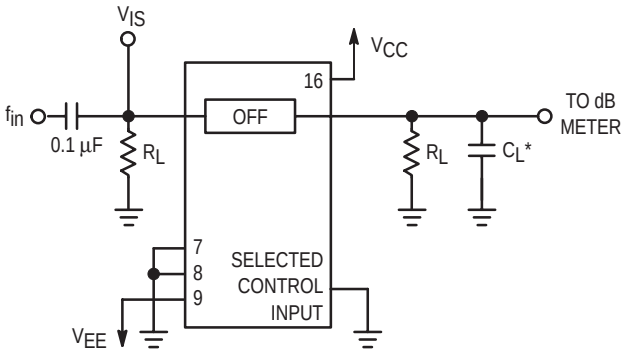


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



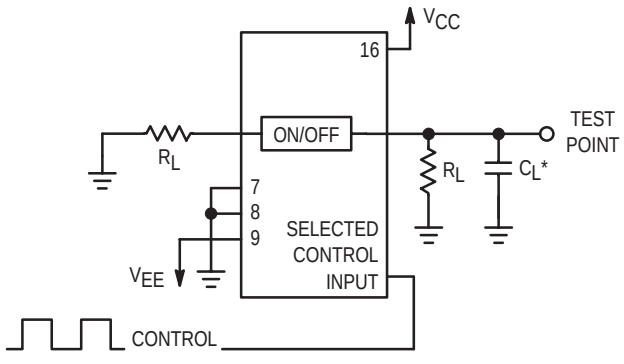
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Control to Analog Out, Test Set–Up

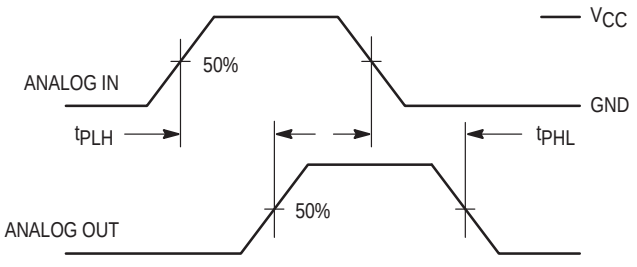
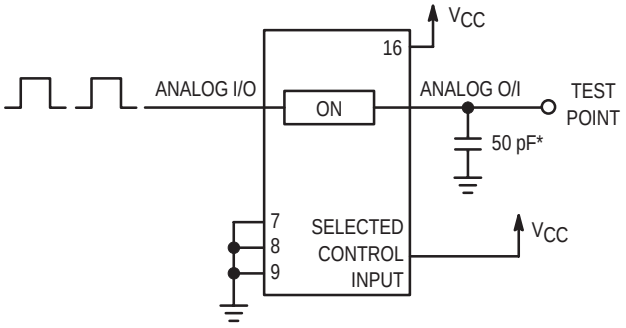


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

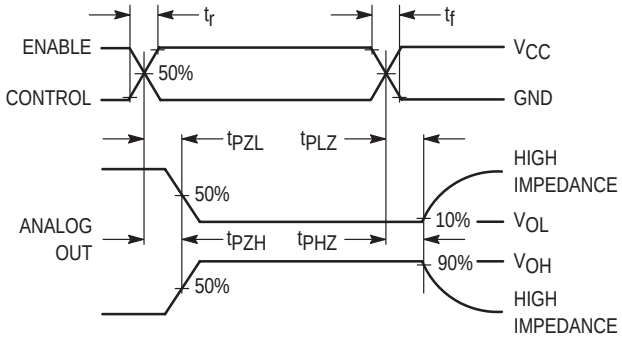
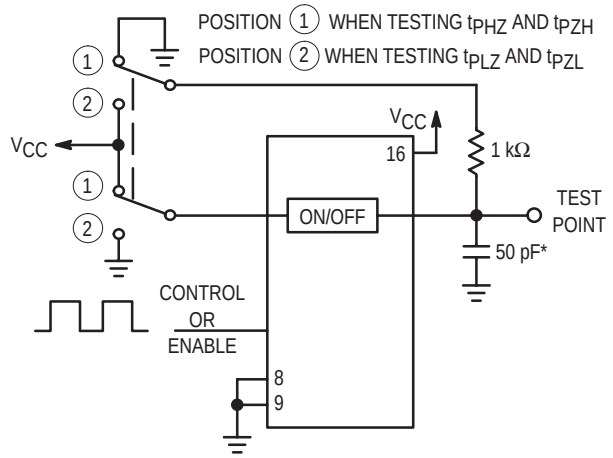
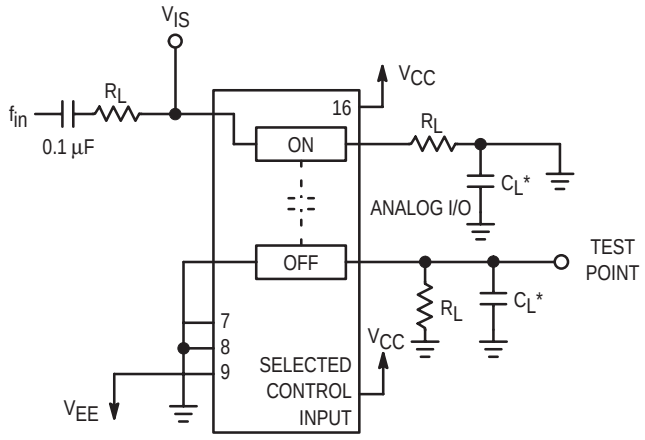


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up (Adjacent Channels Used)

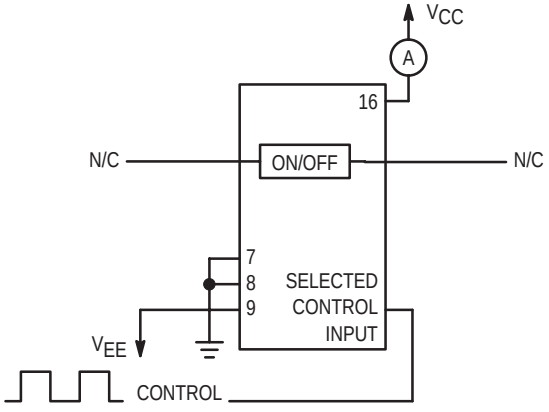
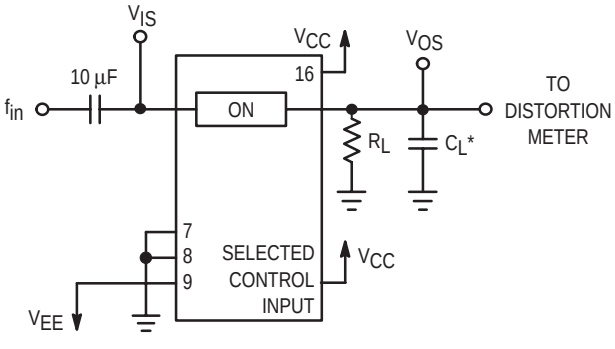


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

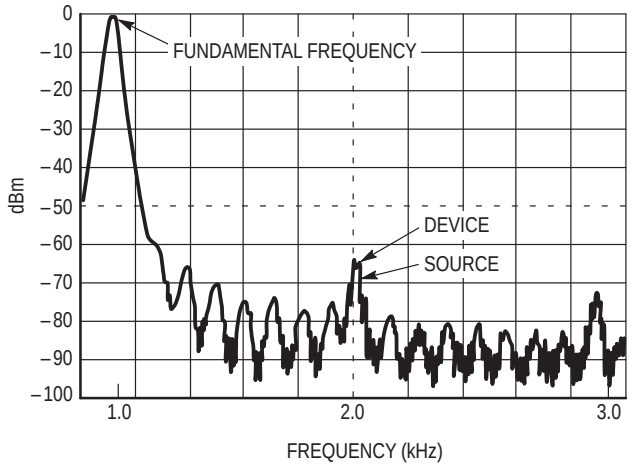


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In the example below, the difference between V_{CC} and V_{EE} is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn–on devices ideally suited for precise dc protection with no inherent wear out mechanism.

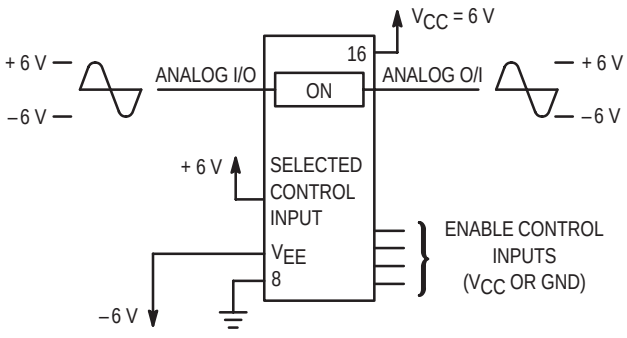


Figure 16.

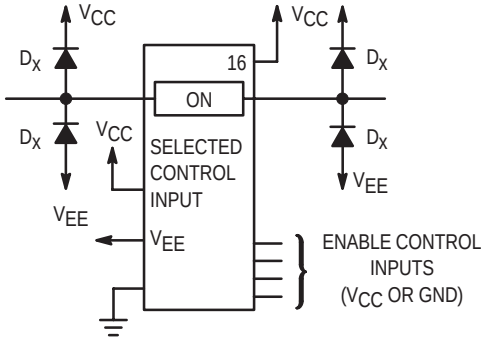
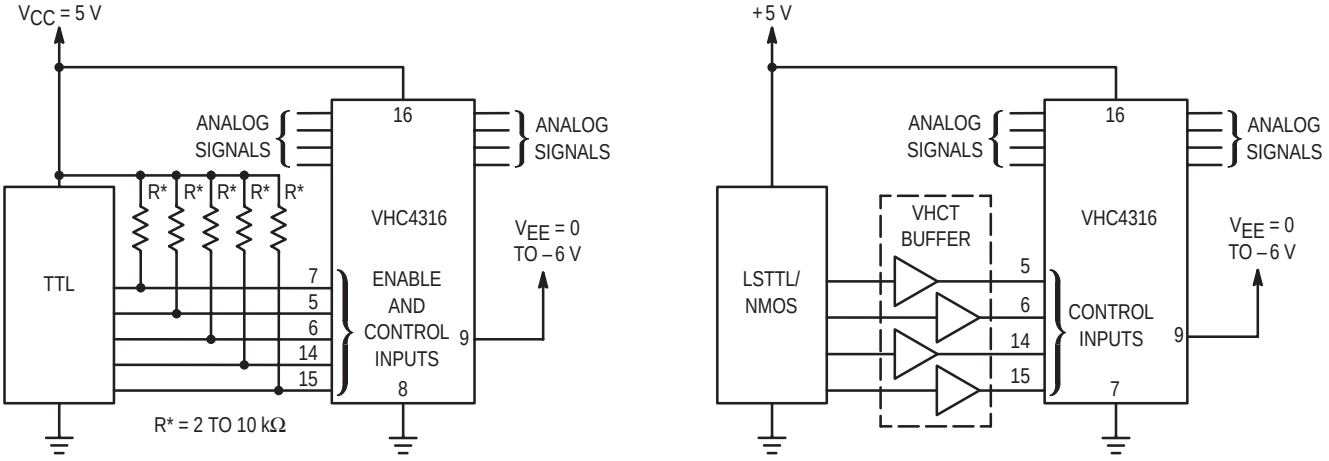


Figure 17. Transient Suppressor Application



a. Using Pull–Up Resistors **b. Using HCT Buffer**

Figure 18. LSTTL/NMOS to HCMOS Interface

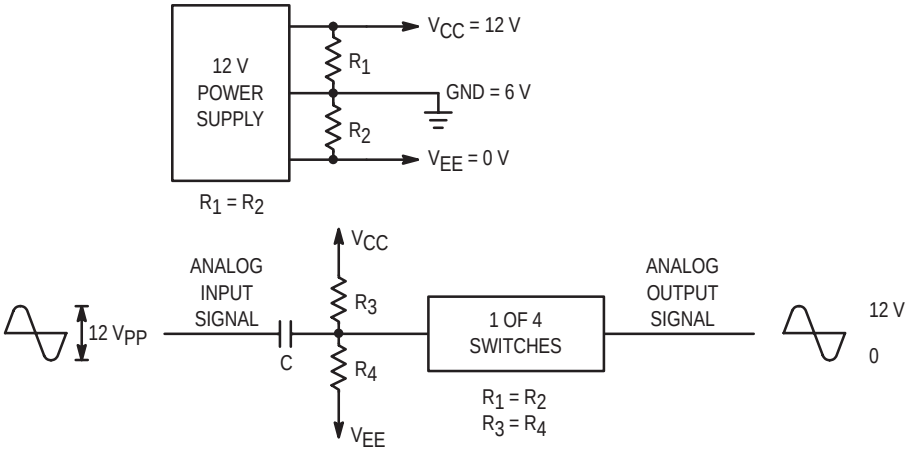


Figure 19. Switching a 0–to–12 V Signal Using a Single Power Supply (GND ≠ 0 V)

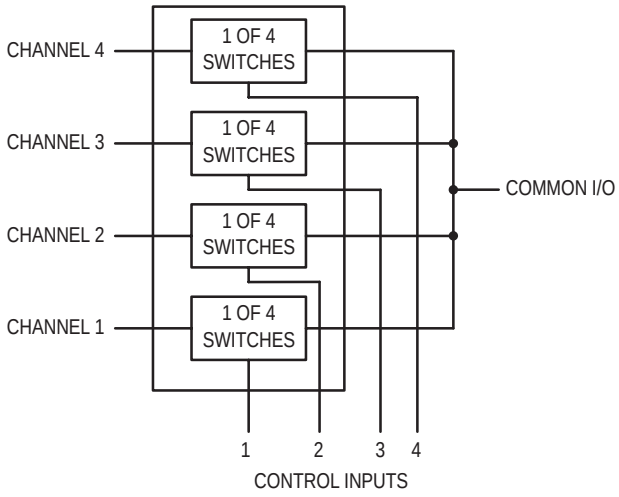


Figure 20. 4–Input Multiplexer

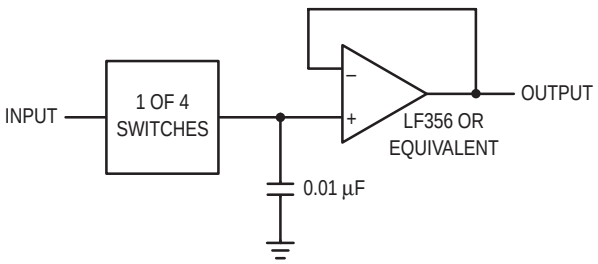


Figure 21. Sample/Hold Amplifier

Advance Information

Analog Multiplexer/ Demultiplexer with Address Latch

High–Performance Silicon–Gate CMOS

MC74VHC4351

The MC74VHC4351 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

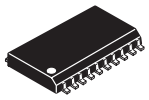
The Channel–Select inputs determine which one of the Analog Inputs/ Outputs is to be connected, by means of an analog switch, to the Common Output/Input. The data at the Channel–Select inputs may be latched by using the active–low Latch Enable pin. When Latch Enable is high, the latch is transparent. When either Enable 1 (active low) or Enable 2 (active high) is inactive, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

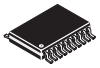
This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

For multiplexers/demultiplexers without latches, see the VHC4051, VHC4052, and VHC4053.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal–Gate Types
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 222 FETs or 55.5 Equivalent Gates



DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04

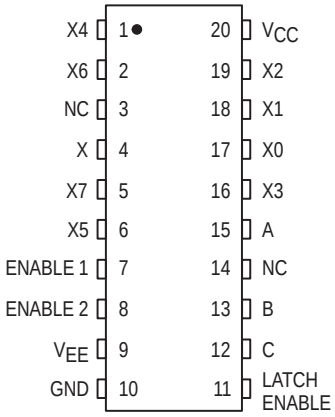


DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

ORDERING INFORMATION

MC74VHCXXXXDW	SOIC Wide
MC74VHCXXXXDT	TSSOP

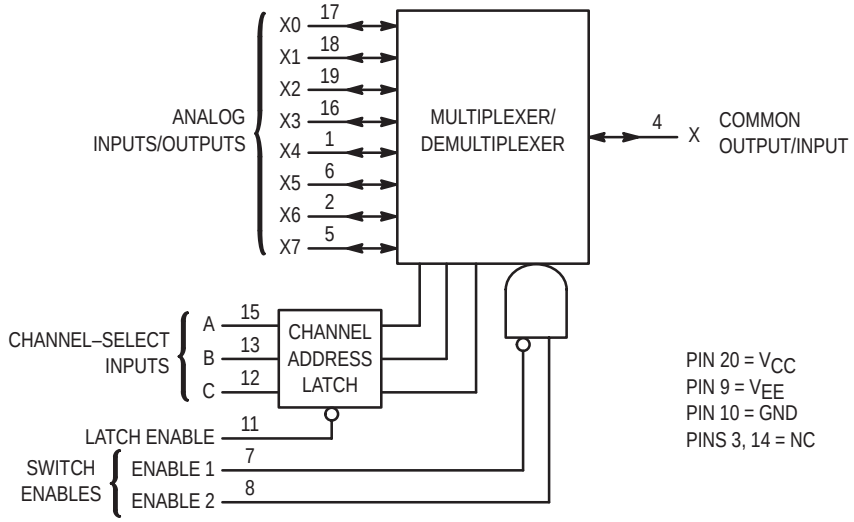
PIN ASSIGNMENT
MC74VHC4351



NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM
MC74VHC4351
Single–Pole, 8–Position Plus Common Off and Address Latch



FUNCTION TABLE
MC74VHC4351

Control Inputs					ON Channel (LE = H)*
Enable		Select			
1	2	C	B	A	
L	H	L	L	L	X0
L	H	L	L	H	X1
L	H	L	H	L	X2
L	H	L	H	H	X3
L	H	H	L	L	X4
L	H	H	L	H	X5
L	H	H	H	L	X6
L	H	H	H	H	X7
H	X	X	X	X	None
X	L	X	X	X	None

X = don't care

* When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage		V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)		– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin		± 25	mA
P_D	Power Dissipation in Still Air	SOIC or TSSOP†	750 500	mW
T_{stg}	Storage Temperature		– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated. See Applications Information.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Ref. to GND) (Ref. to V_{EE})	2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage	(Ref. to GND)	– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		—	1.2	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time, Channel Select or Enable Inputs (Figure 9a)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND Enables = V_{CC} or GND V_{IS} = V_{CC} or GND V_{EE} = GND V_{IO} = 0 V V_{EE} = – 6.0	 6.0 6.0	 1 4	 10 40	 40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to V_{EE} I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	TBD 190 120 100	TBD 240 150 125	TBD 280 170 140	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	TBD 150 100 80	TBD 190 125 100	TBD 230 140 115	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) I_S ≤ 2.0 mA	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	TBD 30 12 10	TBD 35 15 12	TBD 40 18 14	Ω

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC} – V_{EE}$ Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	µA
	Maximum Off–Channel Leakage Current, Common Channel	$V_{in} = V_{IL}$ or V_{IH} $V_{IO} = V_{CC} – V_{EE}$ Switch Off (Figure 4)	6.0	– 6.0	0.2	2.0	4.0	
I_{on}	Maximum On–Channel Leakage Current, Channel to Channel	$V_{in} = V_{IL}$ or V_{IH} Switch to Switch = $V_{CC} – V_{EE}$ (Figure 5)	6.0	– 6.0	0.2	2.0	4.0	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	370 TBD 74 63	465 TBD 93 79	550 TBD 110 94	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	60 TBD 12 10	75 TBD 15 13	90 TBD 18 15	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Analog Output (Figure 12)	2.0 3.0 4.5 6.0	325 TBD 65 55	410 TBD 82 70	485 TBD 97 82	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	290 TBD 58 49	365 TBD 73 62	435 TBD 87 74	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	345 TBD 69 59	435 TBD 87 74	515 TBD 103 87	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O (Enable 1 = V_{IH}, Enable 2 = V_{IL})	—	35	35	35	pF
	Common O/I	—	130	130	130	
	Feedthrough	—	1.0	1.0	1.0	

C_{PD}	Power Dissipation Capacitance (Per Package) (Figure 19.)*	Typical @ 25°C, V_{CC} = 5.0 V	pF
		45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Channel–Select to Latch Enable (Figure 12)	2.0 3.0 4.5 6.0	100 TBD 20 17	125 TBD 25 21	150 TBD 30 26	ns
t_h	Minimum Hold Time, Latch Enable to Channel Select (Figure 12)	2.0 3.0 4.5 6.0	0 TBD 0 0	0 TBD 0 0	0 TBD 0 0	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 12)	2.0 3.0 4.5 6.0	80 TBD 16 14	100 TBD 20 17	120 TBD 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times, Channel–Select, Latch Enable, and Enables 1 and 2	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Condition	V_{CC} V	V_{EE} V	Limit* 25°C 74VHC	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 80 80 80	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 – 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40	
—	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	V_{in} ≤ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A Enable = GND R_L = 600 Ω, C_L = 50 pF	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 25 105 135	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	35 145 190	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 0.10 0.08 0.05	%

* Limits not tested. Determined by design and verified by qualification.

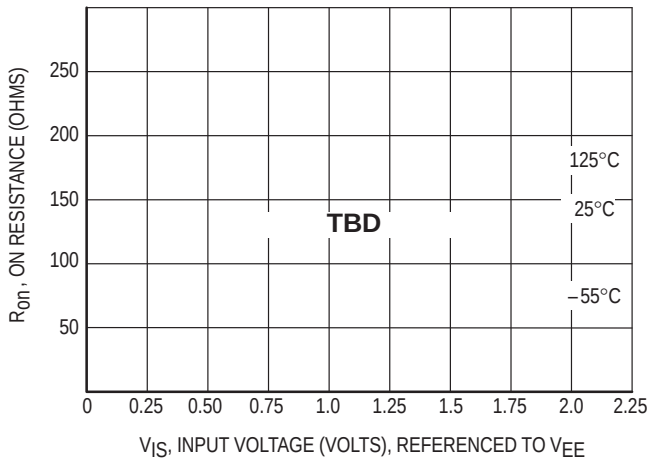


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V

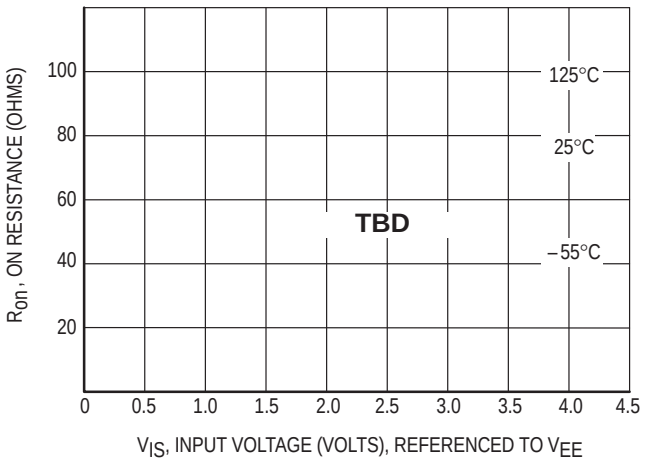


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 3.0 V

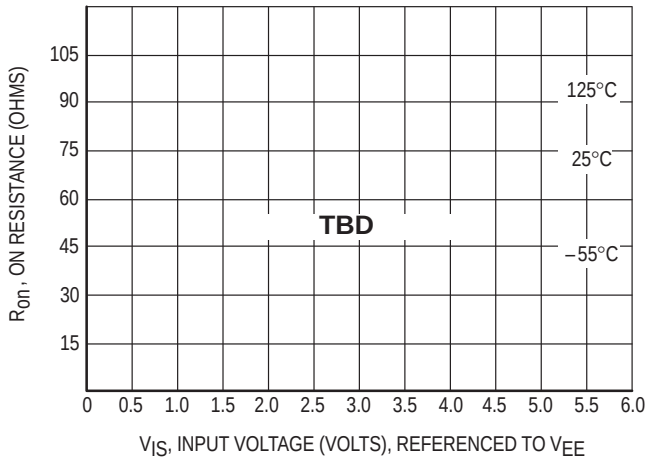


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

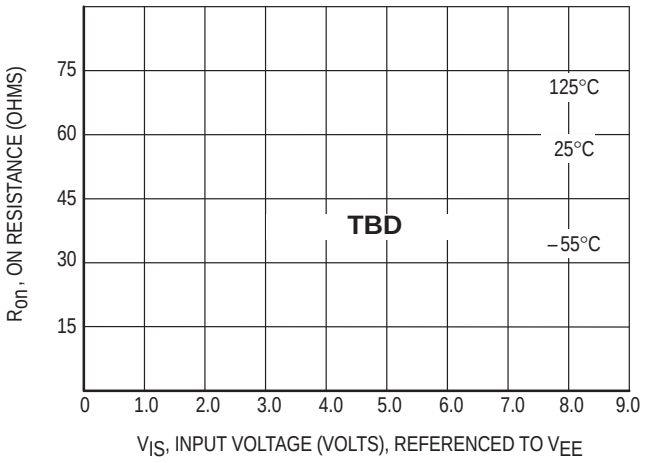


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

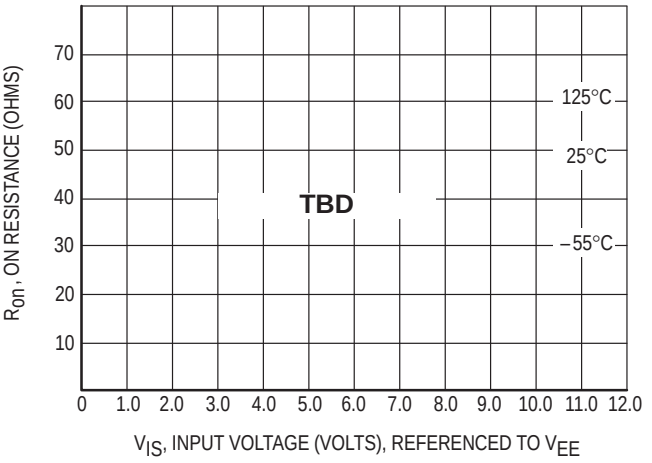


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

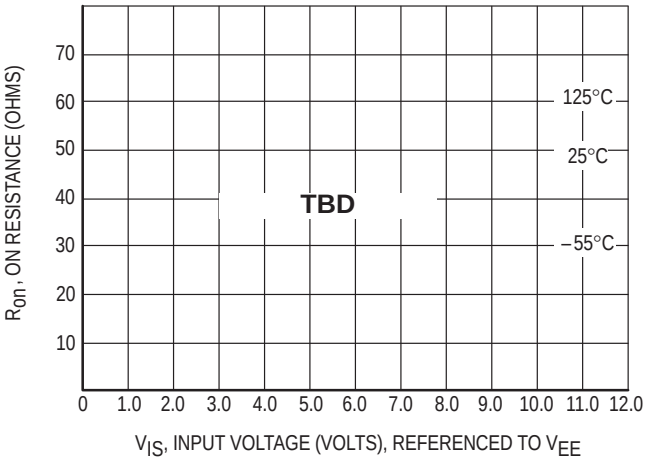


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

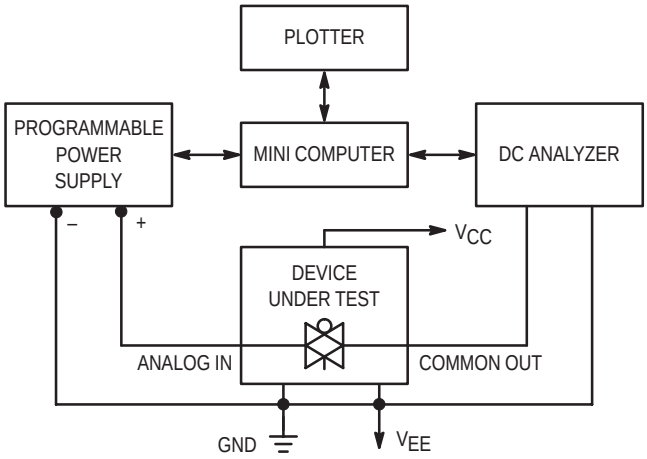


Figure 2. On Resistance Test Set–Up

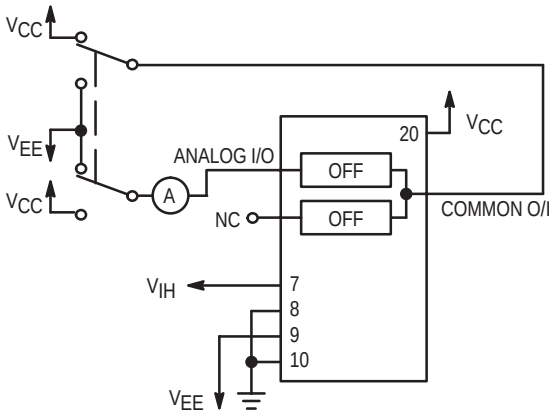


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

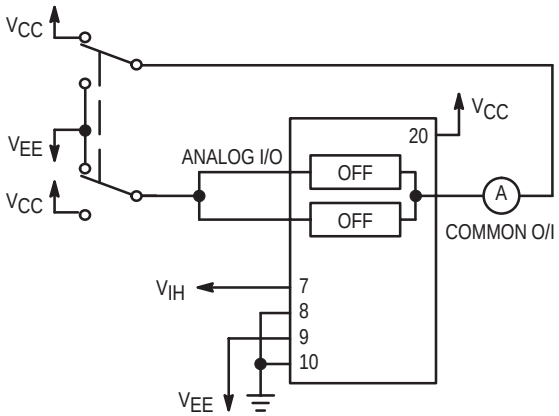


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

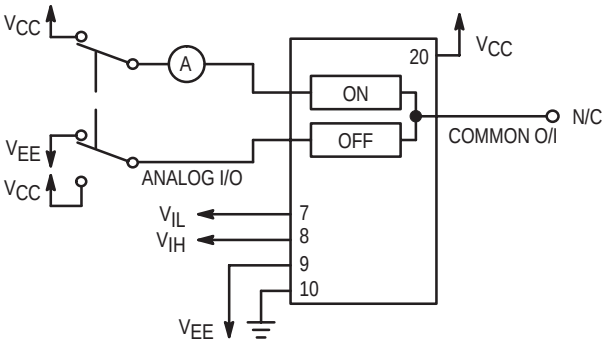
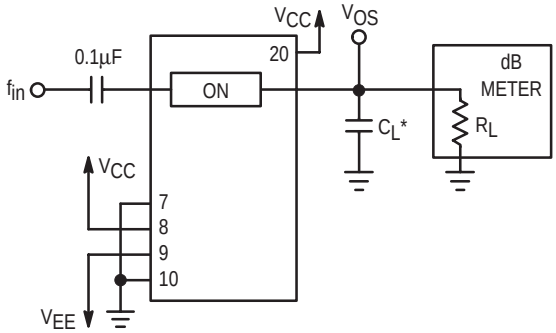
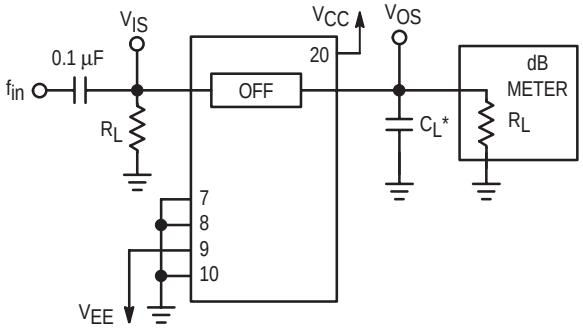


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up



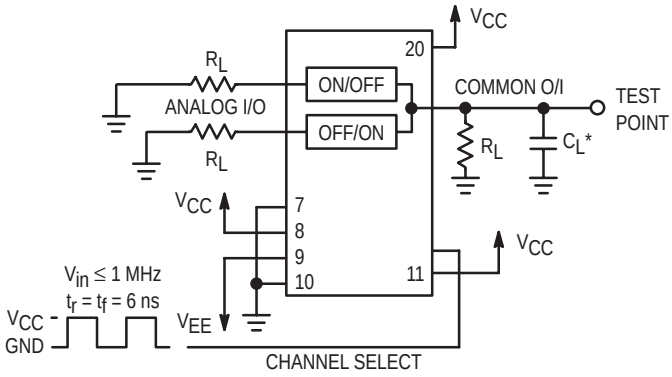
*Includes all probe and jig capacitance.

Figure 6. Maximum On Channel Bandwidth, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Off Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

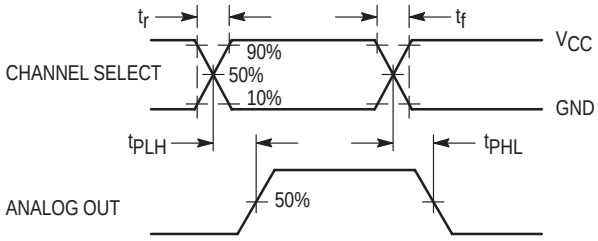
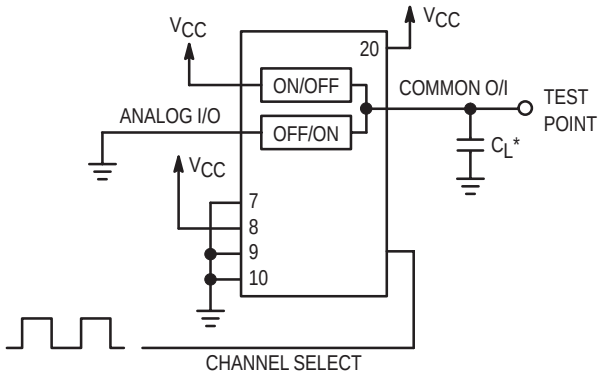


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

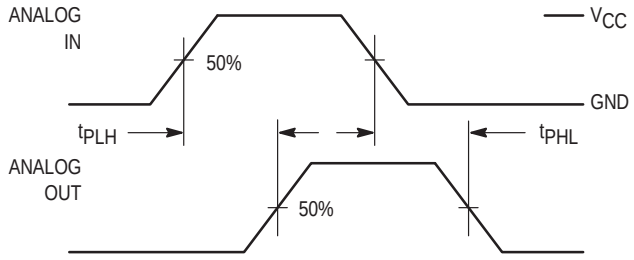
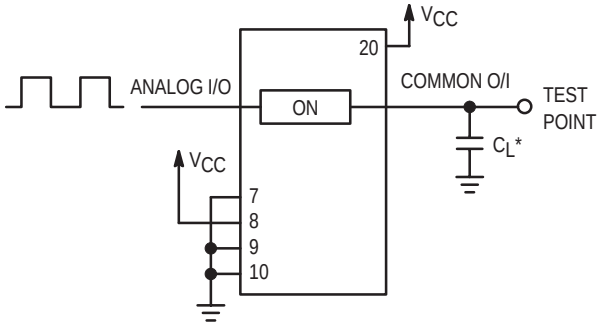


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

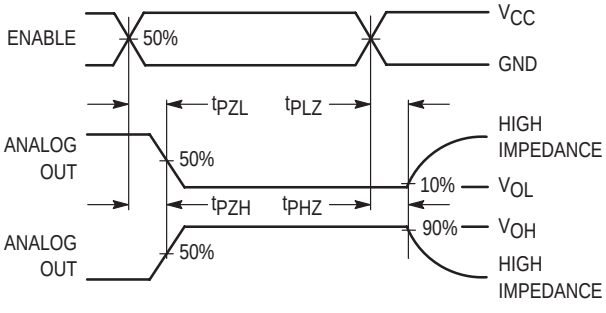


Figure 11a. Propagation Delay, Enable 1 or 2 to Analog Out

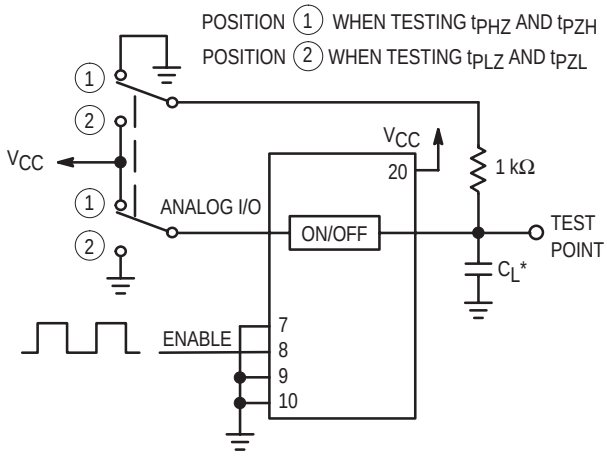


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

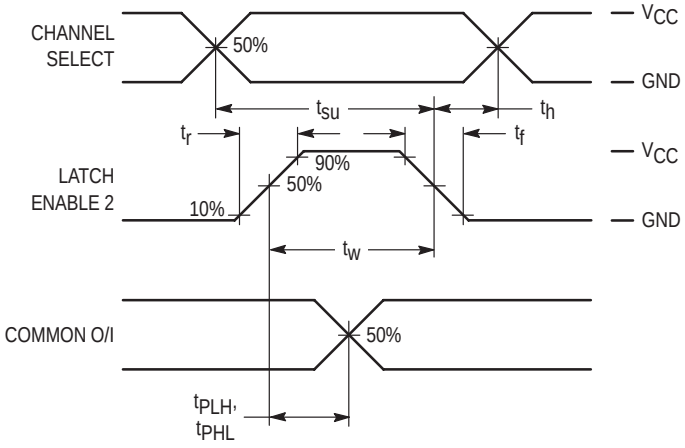
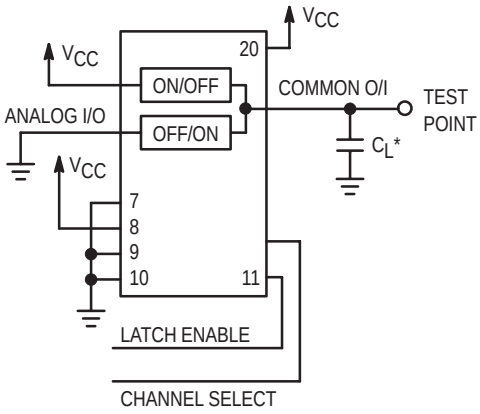


Figure 12a. Propagation Delay, Latch Enable to Analog Out



*Includes all probe and jig capacitance.

Figure 12b. Propagation Delay, Test Set–Up Latch Enable to Analog Out

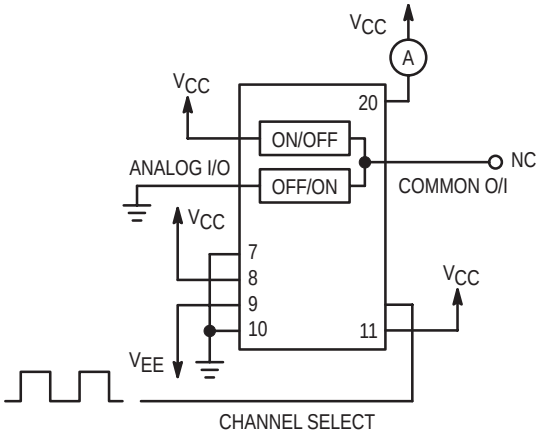
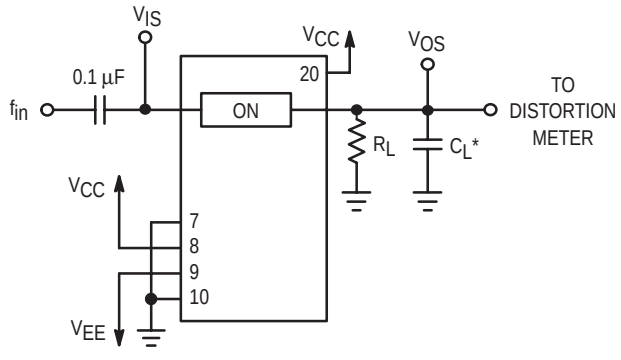


Figure 19. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance.

Figure 14a. Total Harmonic Distortion, Test Set-Up

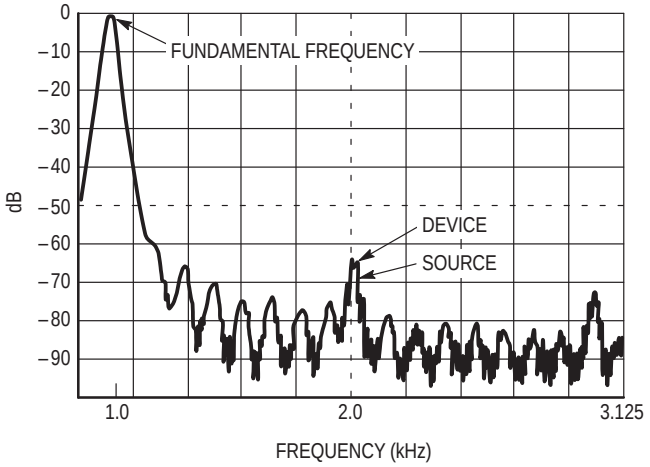


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = + 5 V = logic high

GND = 0 V = logic low

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration in Figure 15, a maximum analog signal of ten volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts

V_{EE} – GND = 0 to – 6 volts

V_{CC} – V_{EE} = 2 to 12 volts

and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

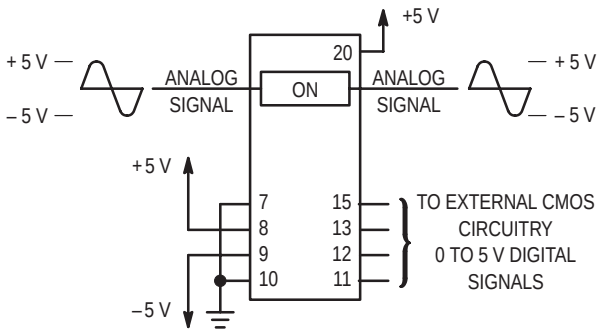


Figure 15. Application Example

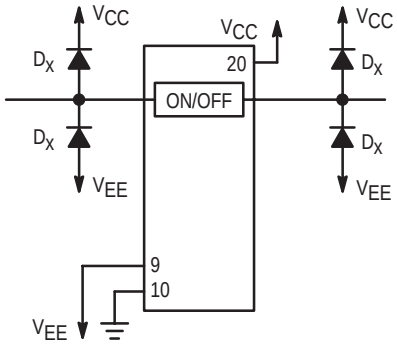
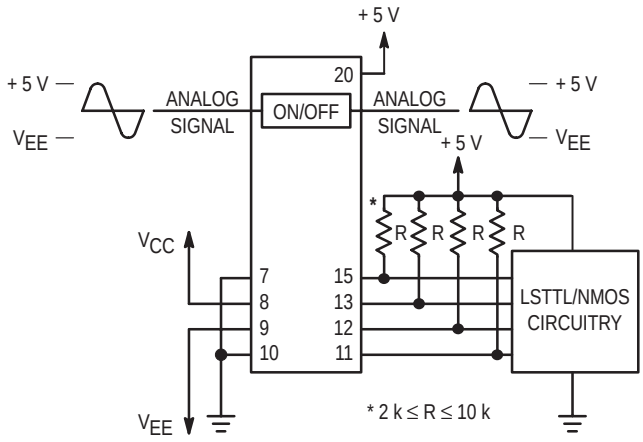
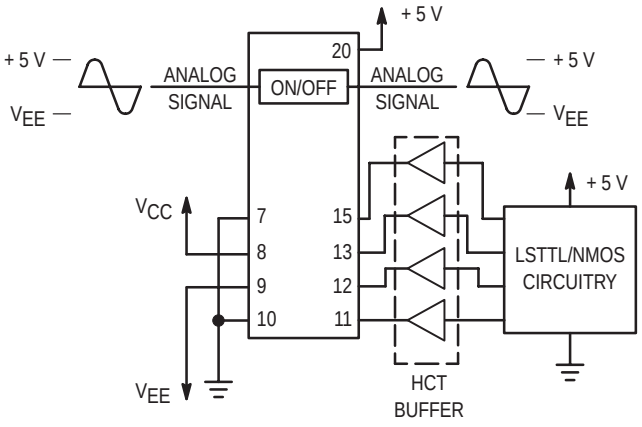


Figure 16. External Germanium or Schottky Clipping Diodes



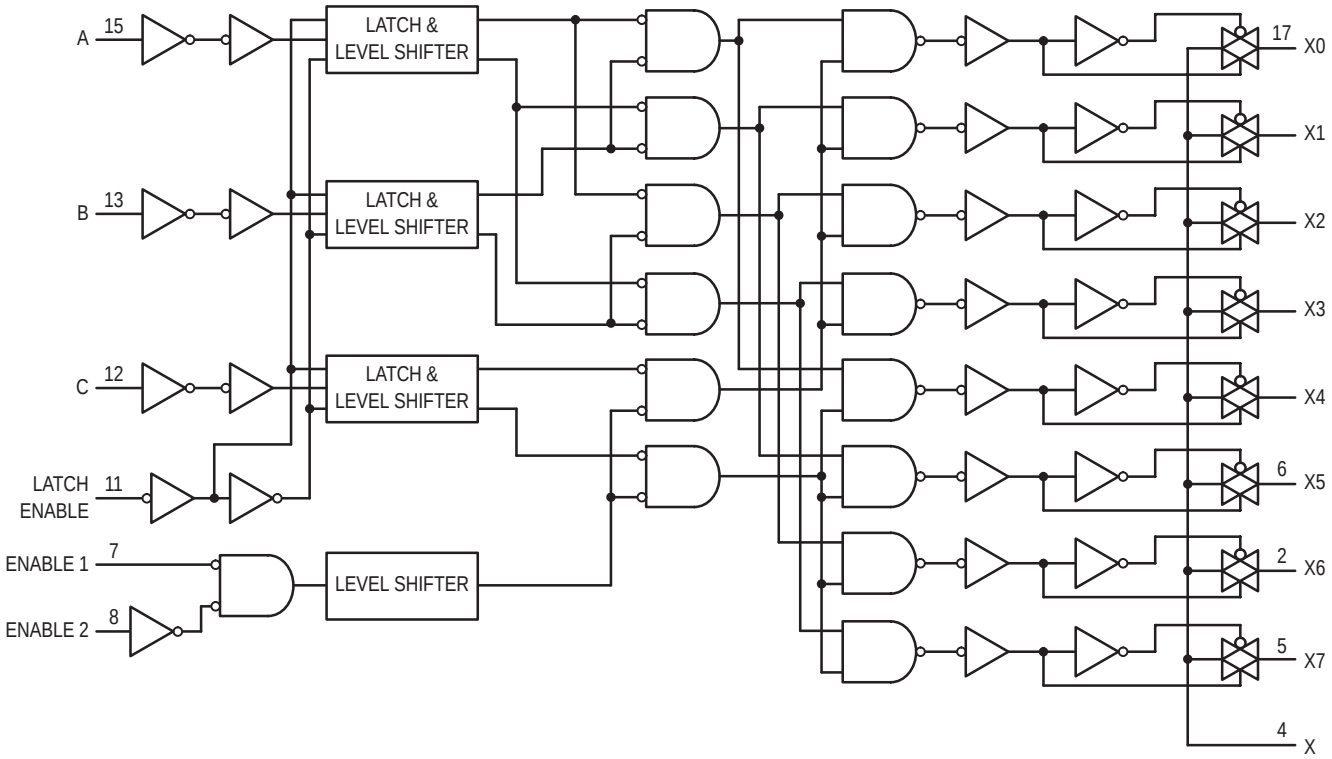
a. Using Pull–Up Resistors



b. Using HCT Interface

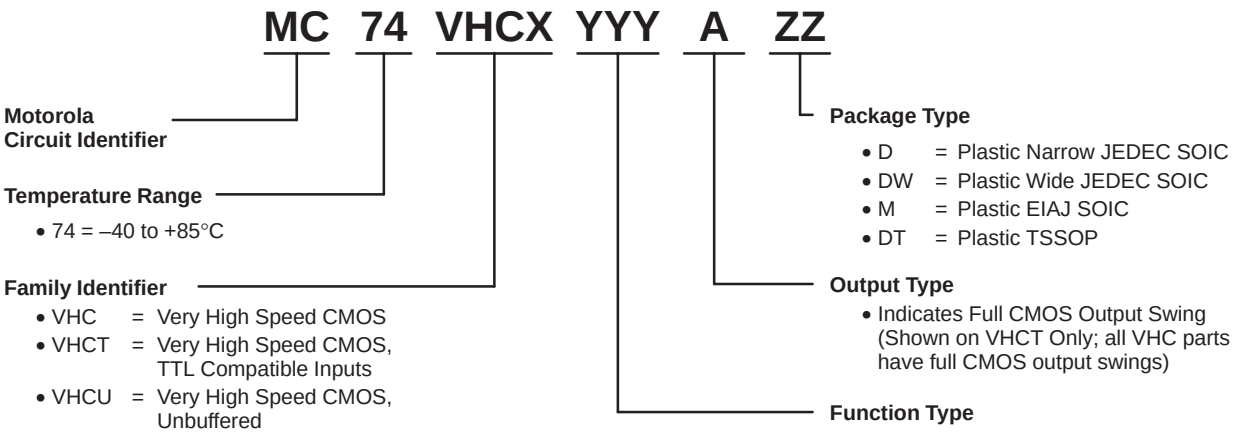
Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

FUNCTION DIAGRAM VHC4351



Ordering Information

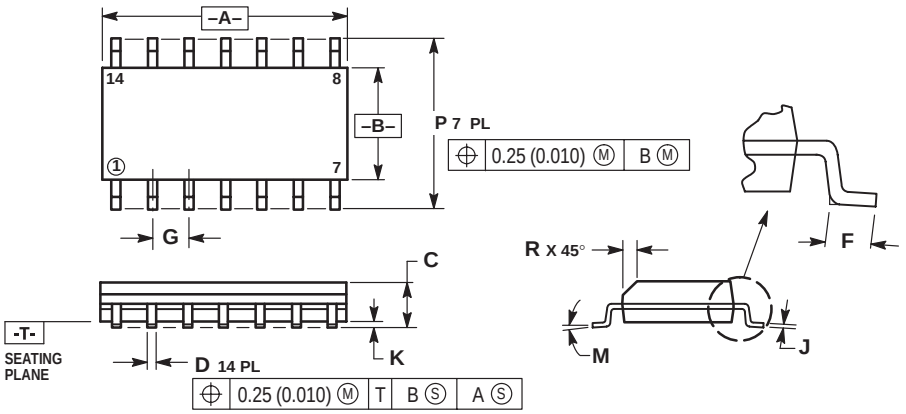
Device Nomenclature



Case Outlines

14-Pin Packages

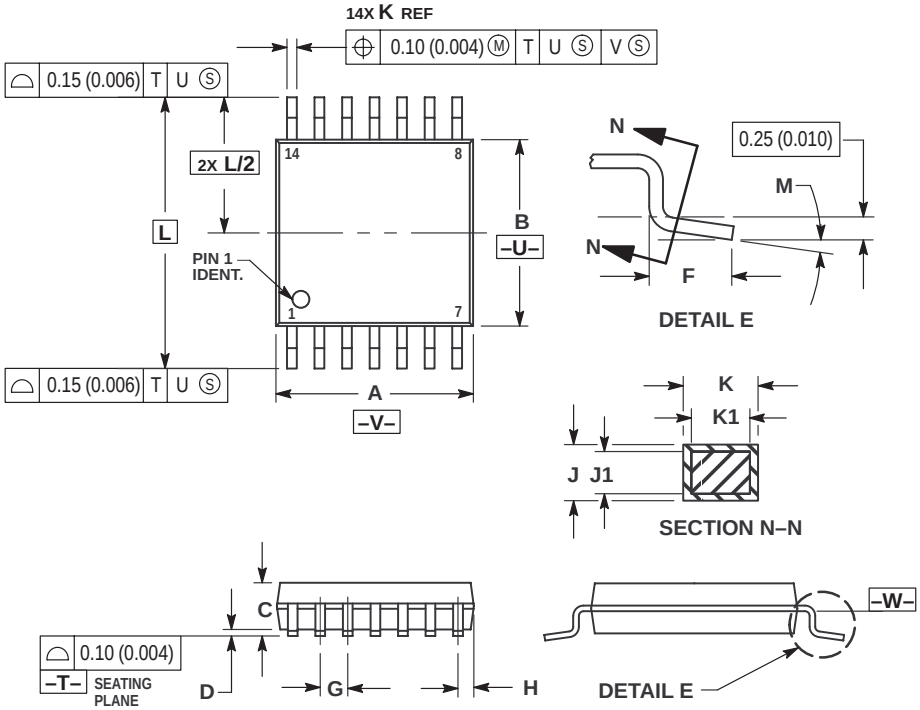
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

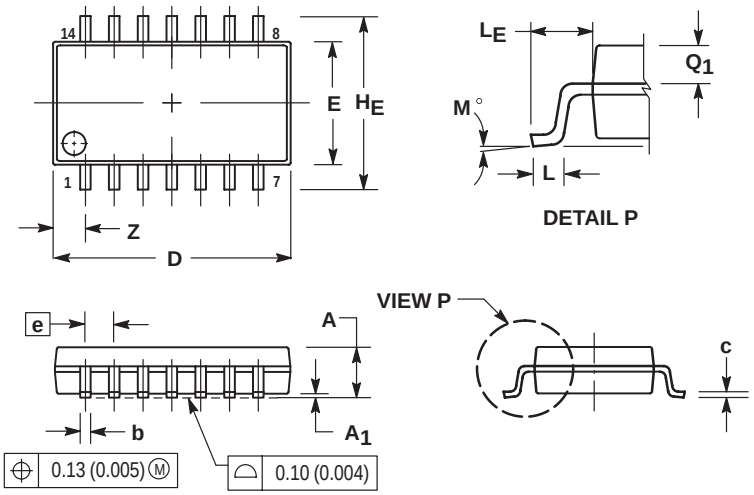


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

14-Pin Packages (continued)

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O

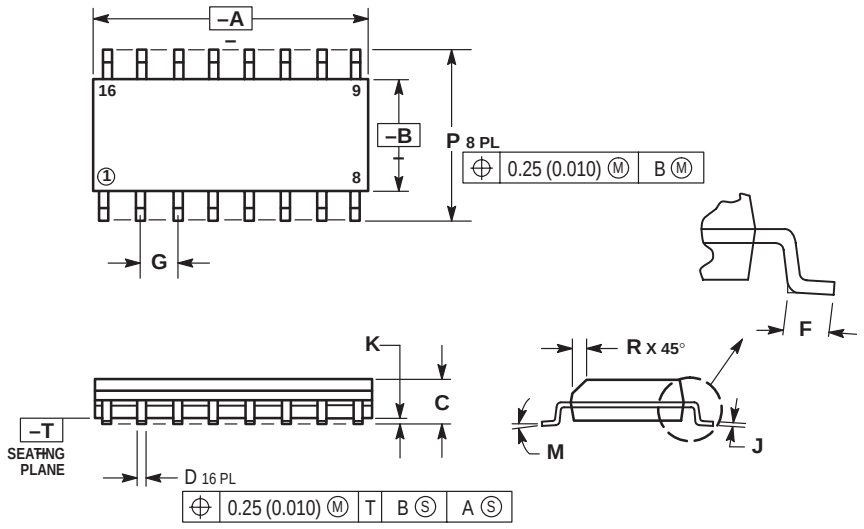


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

16-Pin Packages

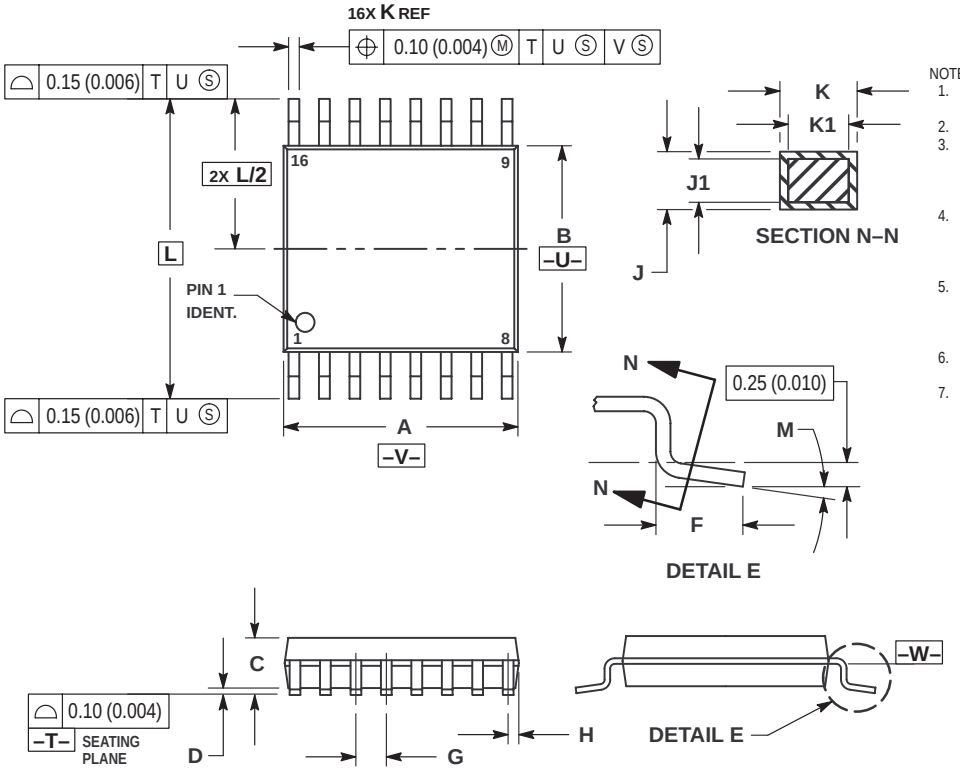
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O

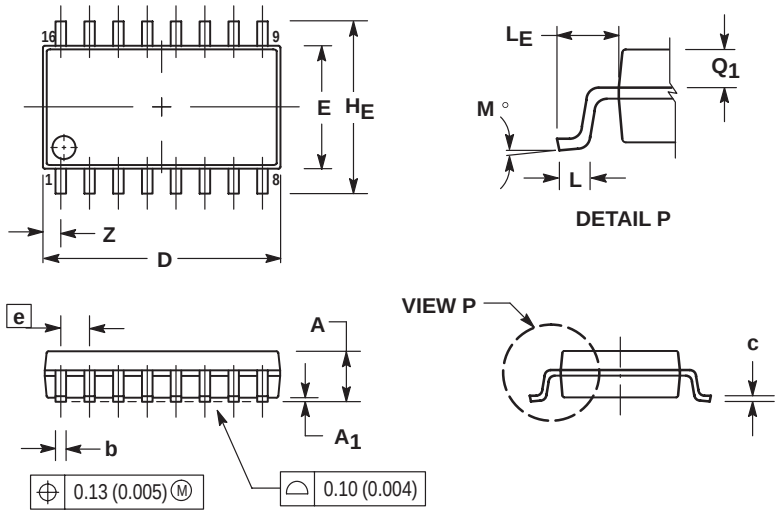


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

16-Pin Packages (continued)

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 966–01
ISSUE O

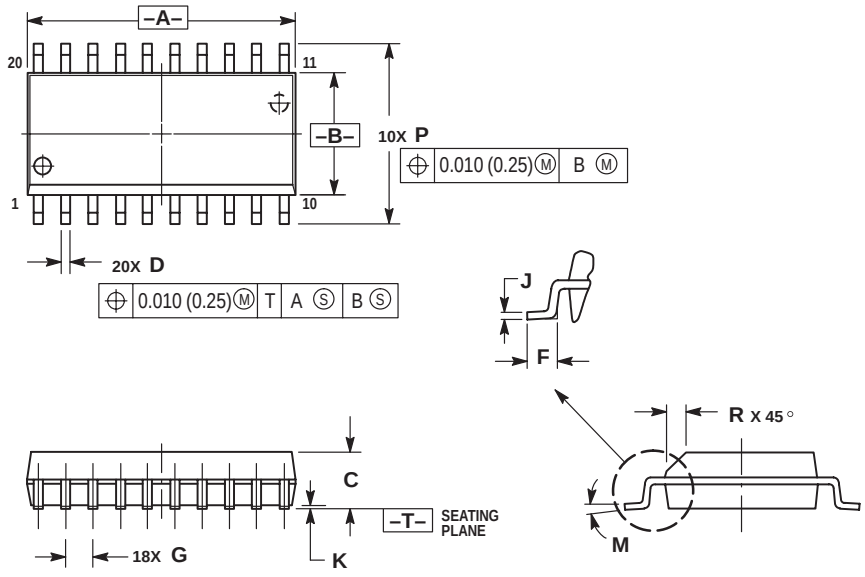


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

20-Pin Packages

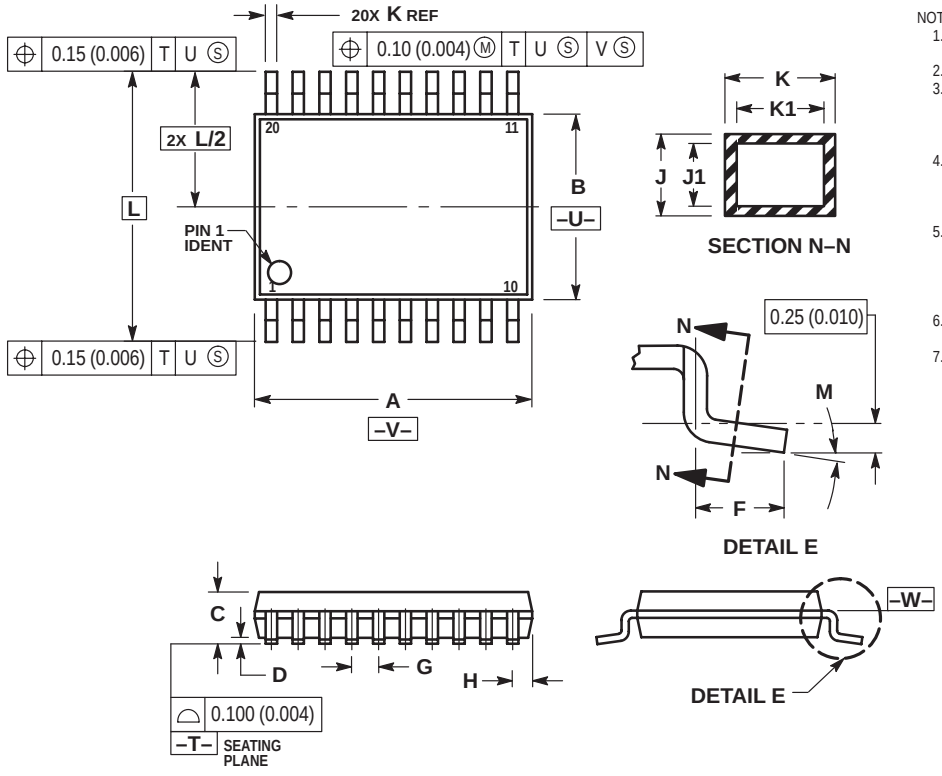
DW SUFFIX
PLASTIC SOIC WIDE PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A

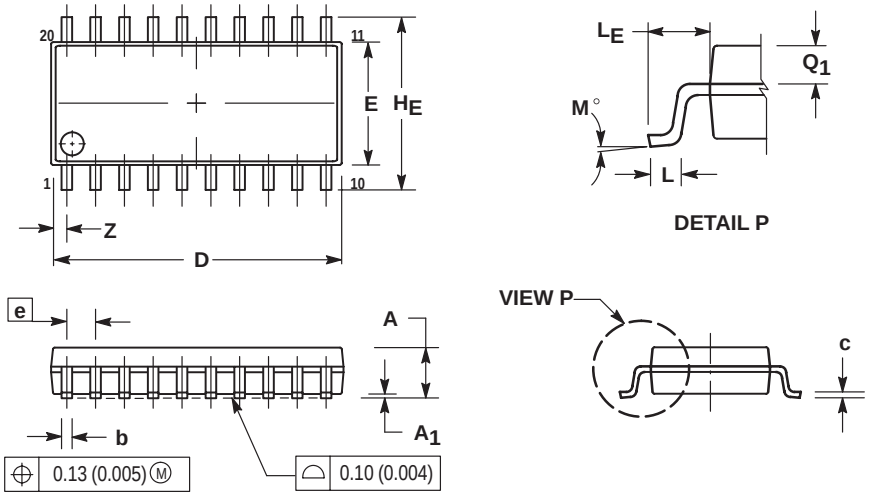


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

20-Pin Packages (continued)

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	——	2.05	——	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	——	0.81	——	0.032

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