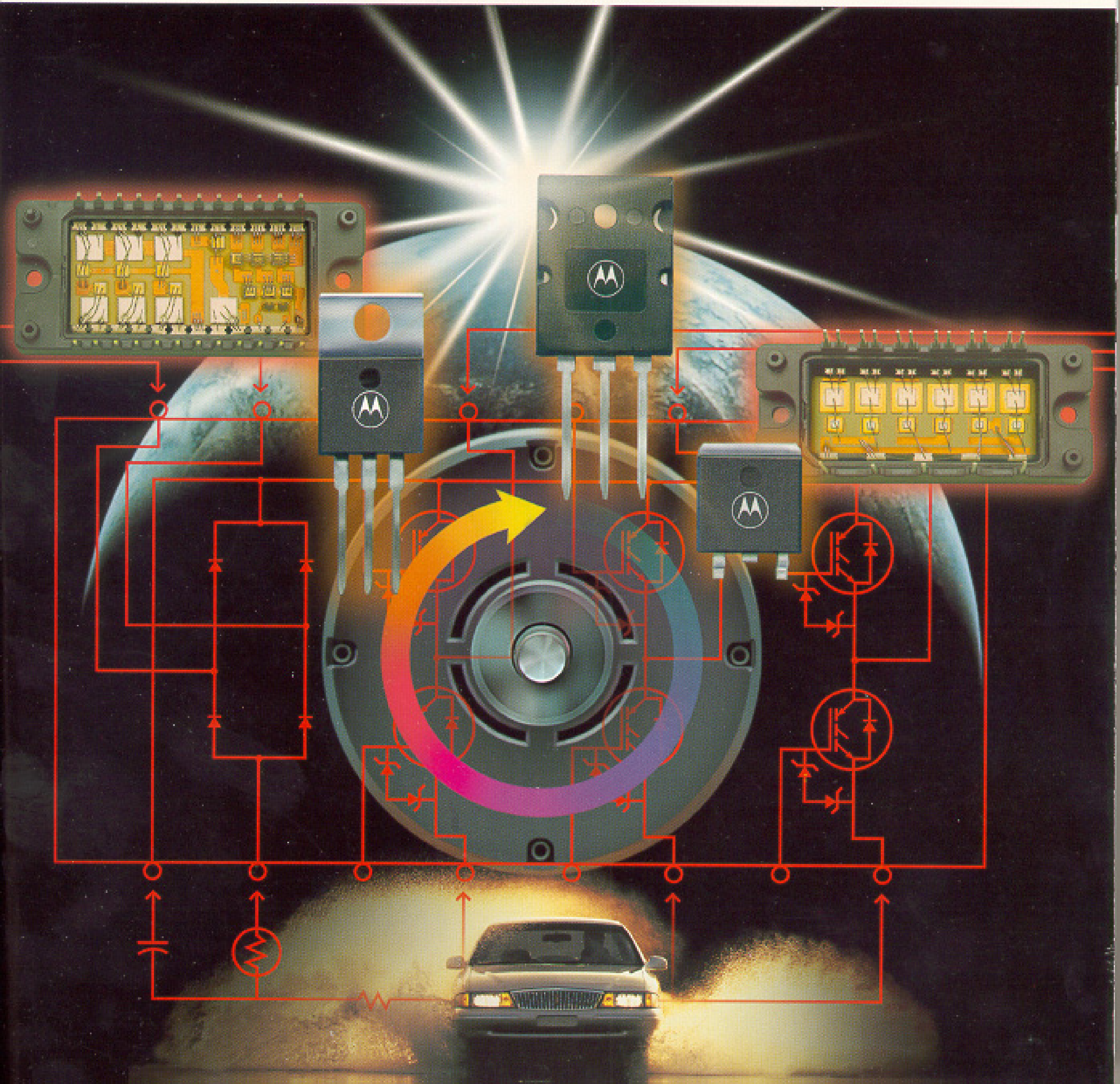
MOTOROLA

DL 202/D

IGBT

Insulated Gate Bipolar Transistor Device Data



IGBT Device Data

Insulated Gate Bipolar Transistor Device Data

Chapter One

Alphanumeric Index

Alphanumeric Index of Part Numbers

The following index provides you with a quick page number reference for complete data sheets. Contact your local Motorola Sales Office for data sheets not referenced in this index.

Chapter Two

IGBT Products and Gate Driver Selector Guides

In Brief . . .

Motorola adds Insulated Gate Bipolar Transistors (IGBTs) to its line of world class power transistors. As a supplier of microcontrollers, integrated circuits, discrete and power modules, we strive to offer our customers system solutions. Our IGBT portfolio consists of devices for automotive applications, lighting, motor drives and power conversion. Advancements in silicon and packaging technologies have led to the following:

- State of the art IGBTs co–packaged with fast, soft recovery diodes up to 1200 volts.
- Ignition IGBTs with integrated gate and collector voltage protection.
- IGBTs with an integrated diode for high frequency lighting applications.
- Surface mount IGBTs with free wheeling diodes.
- New high power packages, E–POWER™ and VersaPower™ in three phase configurations.

Table of Contents

The Discrete IGBT and Power Module Data Sheet

INTRODUCTION

Motorola prides itself in having the most complete and accurate data sheets in the industry. For consistency, data sheet templates have been established for each technology and or application grouping. This insures that the best approach is used in describing the performance characteristics of each device for the applications they are used in. Additionally, this allows for the automation of the data sheet generation process which has lead to a reduction in new product introduction cycle time as well as providing more accurate and repeatable data.

HEADLINE INFORMATION

Motorola's IGBT part numbering system contains coded information describing technology, package, current and voltage information. A complete explanation of the nomenclature for discrete and power module IGBTs are contained in Figures 1 and 2 respectively.

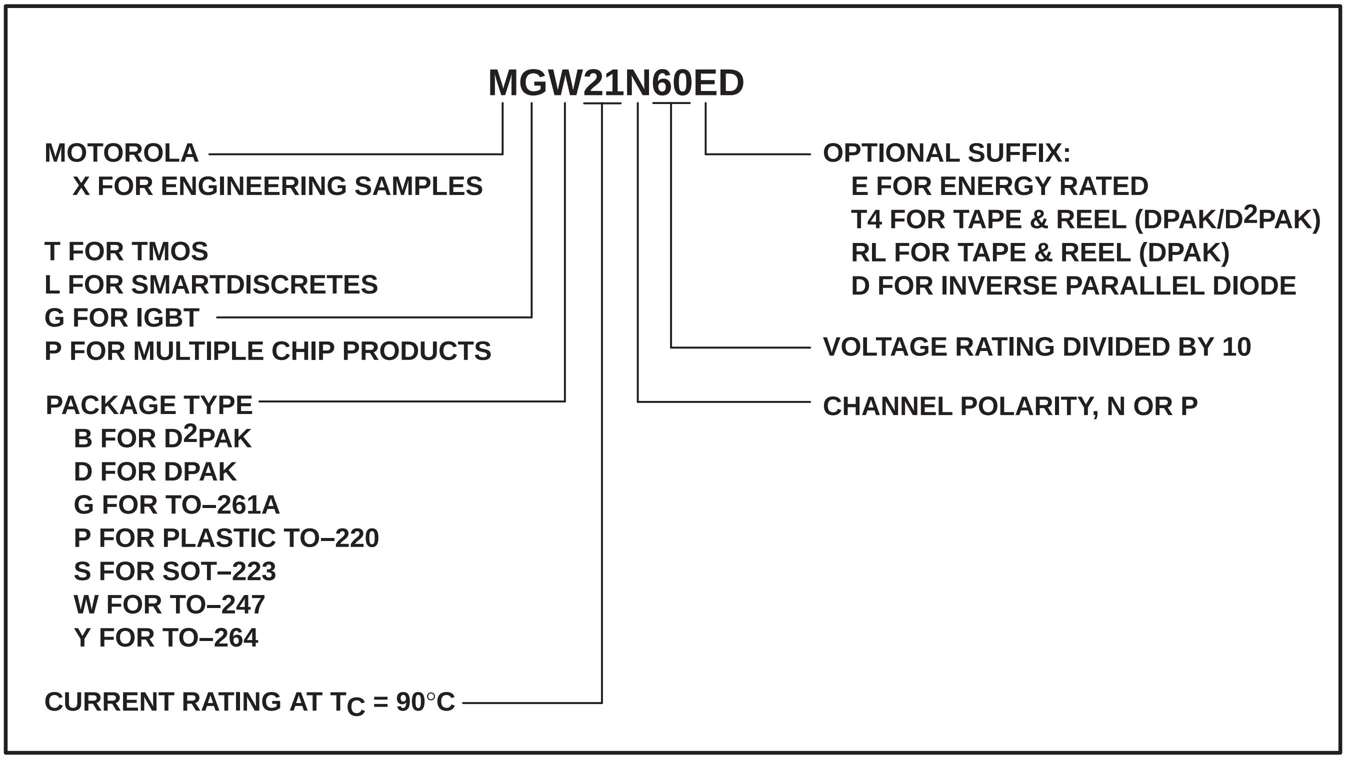


Figure 1. Motorola Discrete IGBT Numbering System

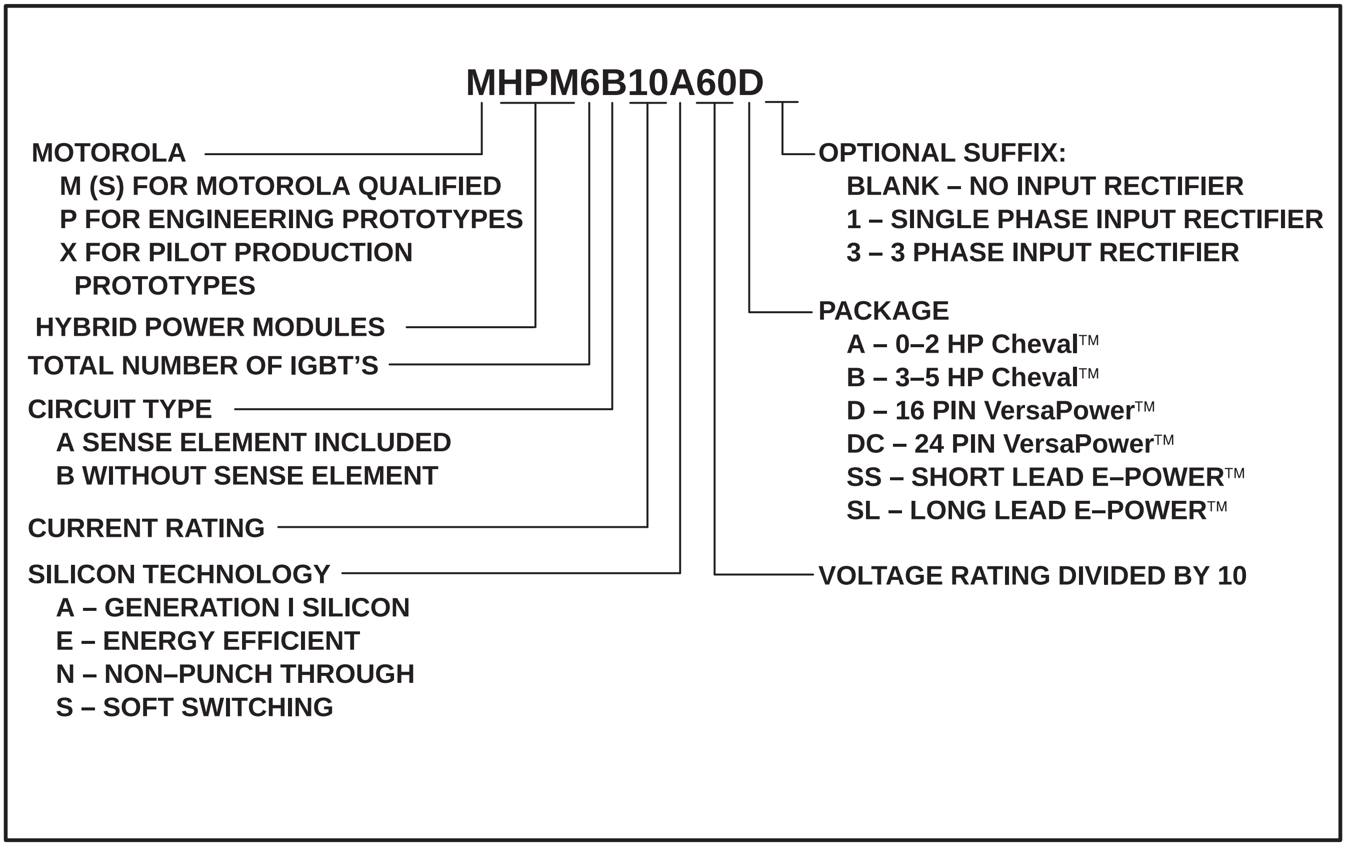
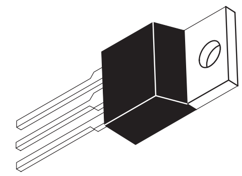


Figure 2. Motorola Module Part Numbering System

IGBTs



Insertion Mount IGBTs

Table 1. TO–220

$V_{(BR)CES}$ (V)	Device	I_C @ 90°C (A)	$V_{CE(on)}$ @ I_C typ (1)		E_{off} typ (3) (µJ/A)	t_{sc} min (3) (µS)	P_D (1) (W)
			(V)	(A)			
600	MGP4N60E	4.0	2.0	3.0	60	10	62.5
	MGP4N60ED						
	MGP7N60E	7.0		5.0	70		81
	MGP7N60ED						
	MGP11N60E	11		8.0	60		96
	MGP11N60ED						
	MGP14N60E	14		10	63		112
	MGP21N60E	21	2.1	20	65		142
	MGP15N60U	15	1.7	8.0	63	N/A	96
	MGP20N60U	20		10			112
380	MGP15N38CL	15 (1)	1.8 (4)				136
400	MGP15N40CL						
430	MGP15N43CL						
135	MGP20N14CL	20 (1)					150
350	MGP20N35CL		1.4 (5)				
400	MGP20N40CL						
630	MGP20N63CL		1.7 (5)				180
600	MGP2N60D	0.9	1.6	0.9			75

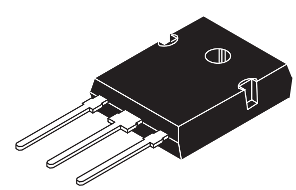


Table 2. TO–247

$V_{(BR)CES}$ (V)	Device	I_C @ 90°C (A)	$V_{CE(on)}$ @ I_C typ (1)		E_{off} typ (3) (µJ/A)	t_{sc} min (3) (µS)	P_D (1) (W)
			(V)	(A)			
600	MGW14N60ED	14	2.0	10	60	10	112
	MGW21N60ED	21	2.1	20	65		142
1200	MGW12N120	12	3.5	10	150		125
	MGW12N120D						
	MGW20N120	20	2.9	20	160		174

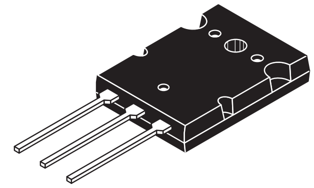


Table 3. TO–264

$V_{(BR)CES}$ (V)	Device	I_C @ 90°C (A)	$V_{CE(on)}$ @ I_C typ (1) (V)	(A)	E_{off} typ (3) (µJ/A)	t_{sc} min (3) (µS)	P_D(1) (W)
1200	MGY20N120D	20	2.9	20	160	10	174
	MGY25N120	25	3.0	25	216		212
	MGY25N120D						

(1) T_C = 25°C unless otherwise specified
(2) Power rating when mounted on an FR–4 glass epoxy PC board with the minimum recommended footprint.
(3) T_C = 125°C
(4) Maximum Value at T_J = 150°C
(5) T_J = 150°C
D suffix on part number indicates free wheeling diode is copackaged with IGBT

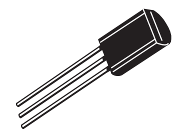


Table 4. TO–226AE

$V_{(BR)CES}$ (V)	Device	I_C @ 90°C (A)	$V_{CE(on)}$ @ I_C typ (1) (V)	(A)	E_{off} typ (3) (µJ/A)	t_{sc} min (3) (µS)	P_D(1) (W)
600	MGS05N60D	0.3	1.6	0.3	16.2	N/A	1.0
	MGS13002D						

Surface Mount IGBTs

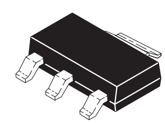


Table 5. SOT 223

$V_{(BR)CES}$ (V)	Device	I_C @ 90°C (A)	$V_{CE(on)}$ @ I_C typ (1) (V)	(A)	E_{off} typ (3) (µJ/A)	t_{sc} min (3) (µS)	P_D(1) (W)
600	MMG05N60D	0.3	1.6	0.3	N/A	N/A	1.0

(1) T_C = 25°C unless otherwise specified
(2) Power rating when mounted on an FR–4 glass epoxy PC board with the minimum recommended footprint.
(3) T_C = 125°C
D suffix on part number indicates free wheeling diode is copackaged with IGBT

Hybrid Power Modules

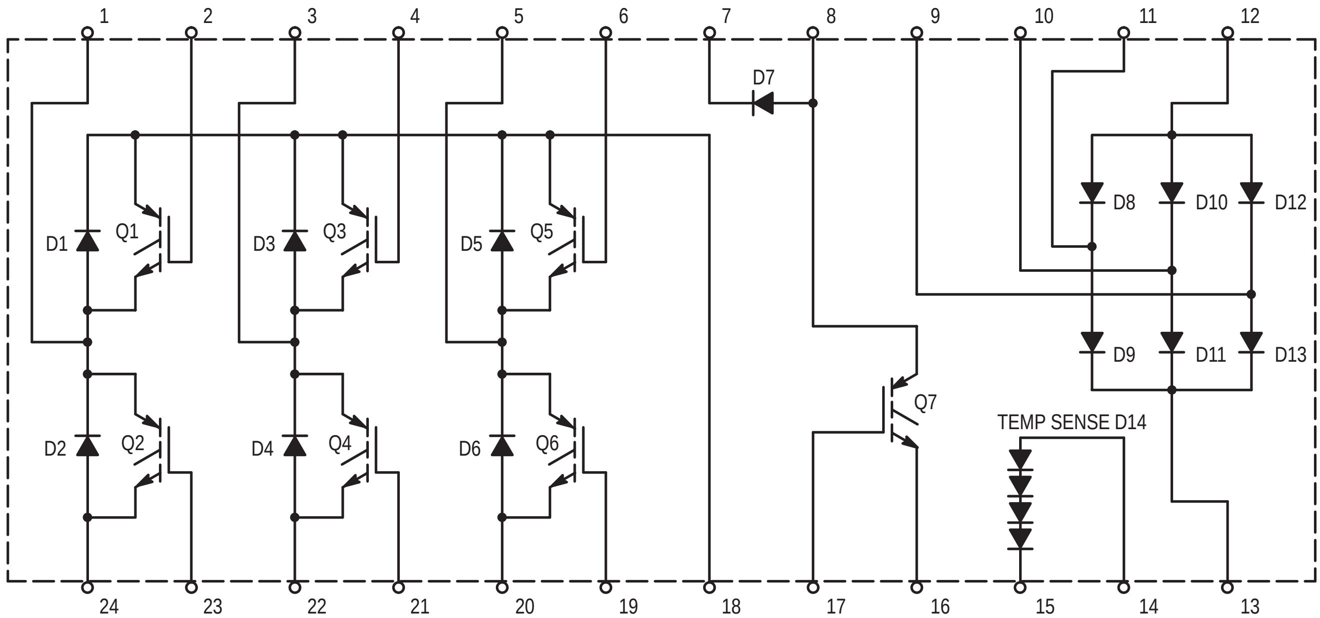


Table 6. Three Phase Inverter with a Three Phase Input Rectifier Bridge, Brake and Temperature Sense in the 24 Pin VersaPower™ Package

Maximum Ratings		
$V_{(BR)CES}$		
I_C (A)	600 V	1200 V
5		MHPM7A5S120DC3
10	MHPM7A10E60DC3	MHPM7A10S120DC3
15		MHPM7A15S120DC3
20	MHPM7A20E60DC3	
25		MHPM7A25S120DC3
30	MHPM7A30E60DC3	

VersaPower™ Package Features and Benefits

- Combines the IGBTs and diodes needed to construct a three phase inverter bridge arrangement in one package
- Utilizes Motorola's advanced 600 & 1200 V IGBTs with matched soft free–wheeling diodes.
- Motor drives operating directly off–line require reliable and rugged rectifiers for conversion of the ac line voltage to a dc voltage source. This is accomplished with single or three phase bridge circuits for rectification. Because of the transient voltages that occur on the AC power line, high voltage rectifiers are required. In addition, these rectifiers must be capable of withstanding high inrush currents required to charge large filter capacitors. Motorola has put Rectifiers into its VersaPower™ series, specifically to meet these requirements.
- Package gives benefits of an integrated solution in an economical package.
- Temperature sense integrated in module (24 pin).

Hybrid Power Modules

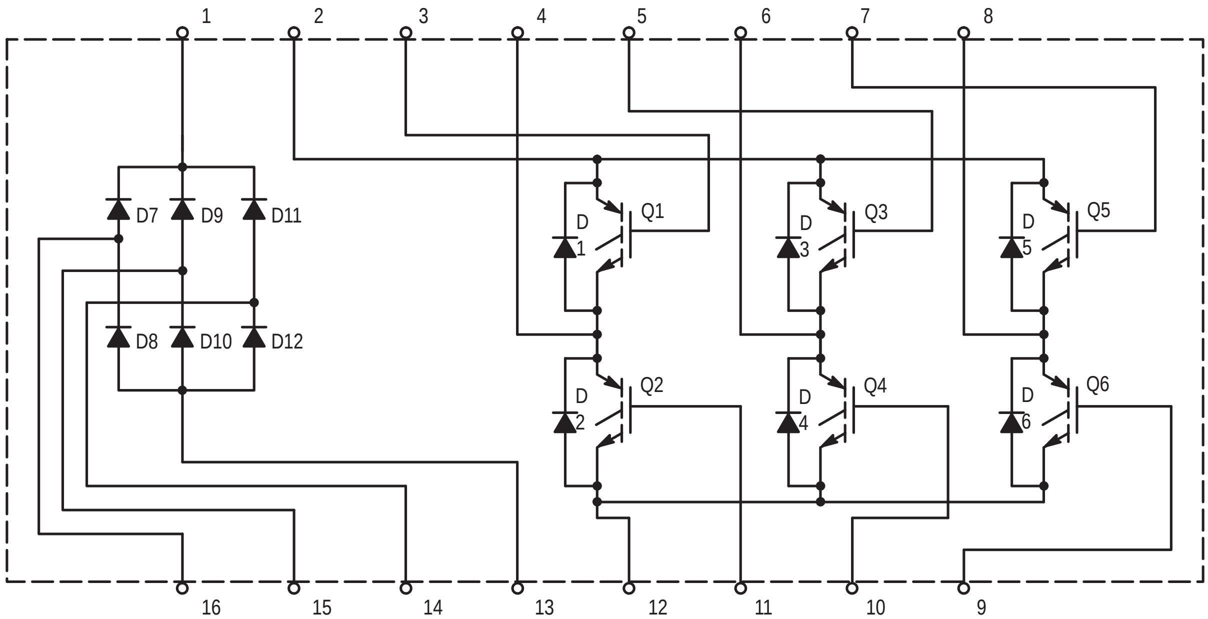


Table 7. Three Phase Inverter with Three Phase Input Rectifier Bridge in the 16 Pin VersaPower™ Package

Maximum Ratings		
$V_{(BR)CES}$		
I_C (A)	600 V	1200 V
7	MHPM6B7E60D3	
10	MHPM6B10E60D3	
15	MHPM6B15E60D3	
10	MHPM6B20E60D3	

Hybrid Power Modules

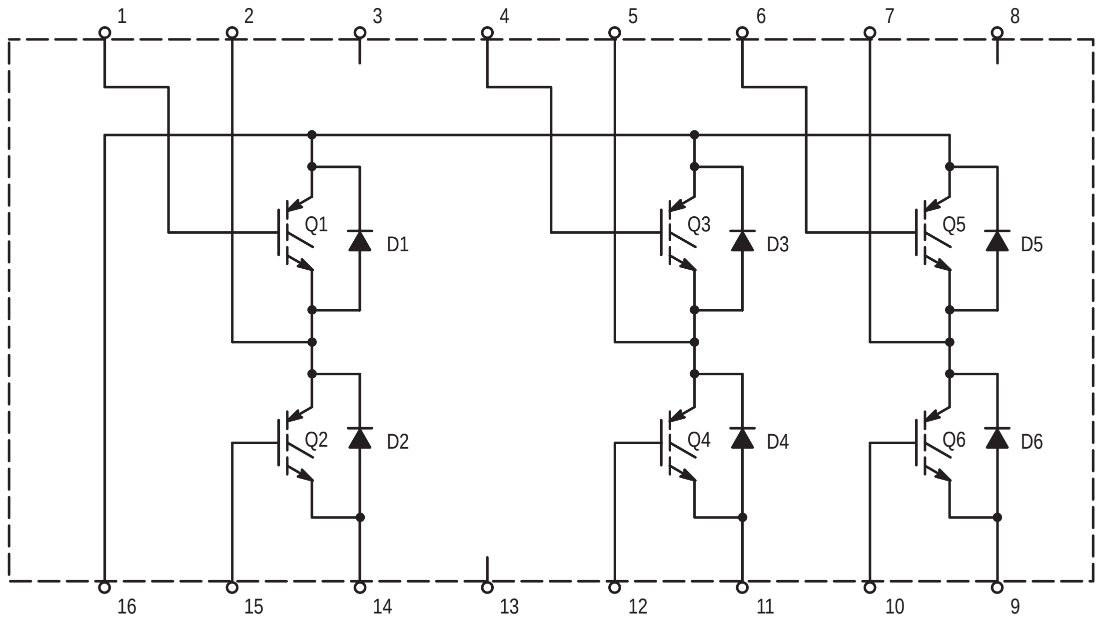


Table 8. Three Phase Inverter (6–Pack) in a 16 Pin VersaPower™ Package

Maximum Ratings		
	$V_{(BR)CES}$	
I_C (A)	**600 V**	**1200 V**
5		MHPM6B5A120D
10	MHPM6B10A60D	MHPM6B10A120D
15		MHPM6B15A120D
20	MHPM6B20A60D	

Hybrid Power Modules

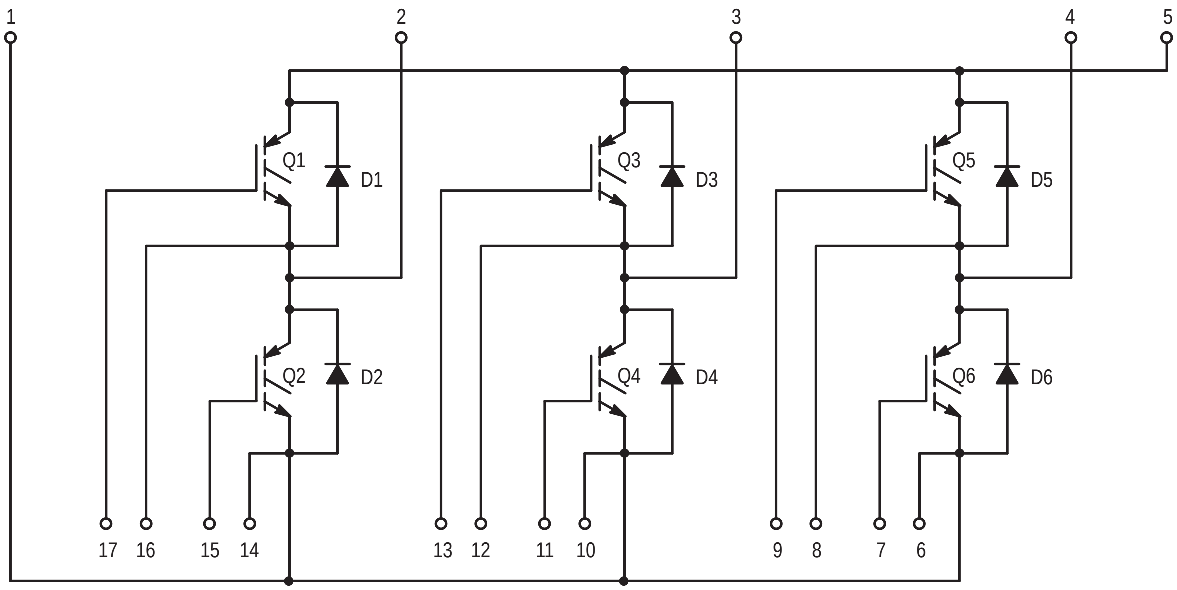


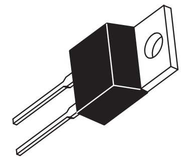
Table 9. E–POWER™ SIX–PACK

Maximum Ratings		
I_C (A)	**$V_{(BR)CES}$ (V)**	**Device**
10	1200	MHPM6B10N120SL & SS
15	1200	MHPM6B15N120SL & SS
25	1200	MHPM6B25N120SL & SS

Benefits of Motorola Integrated Power Stage

- Output Inverter Circuit
- Utilizes Motorola's Advanced 1200 V IGBTs with Matched Soft Free Wheeling Diodes
- Positive and Negative Buss Access to Designer
- European Standard Replacement
- Available in 2 Lead Lengths for PC Board & Other Applications

SWITCHMODE Soft Recovery Power Rectifier

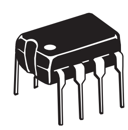


Designed for use as free wheeling diodes in variable speed motor control applications and switching power supplies. These state–of–the–art devices have the following features:

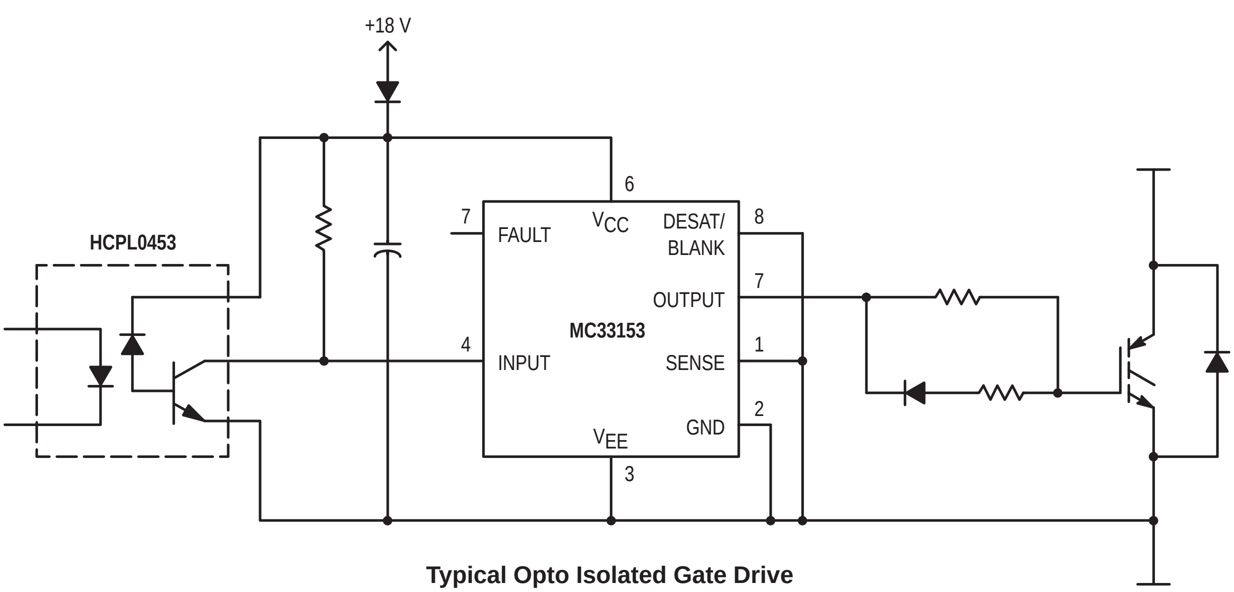
- Soft Recovery with Guaranteed Low Reverse Recovery Charge (Q_{RR}) and Peak Reverse Recovery Current (I_{RRM})
- 150°C Operating Junction Temperature
- Popular TO–220 Package
- Epoxy meets UL94, V_O @ 1/8″
- Low Forward Voltage
- Low Leakage Current
- High Temperature Glass Passivated Junction

MOS Gate Driver

The MC33153 and MC33154 are specifically designed as IGBT drivers for high power applications that include ac induction motor control, brushless dc motor control and uninterruptible power supplies. Designed for driving IGBTs, these devices also offer a cost effective solution for driving power MOSFETs and Bipolar Transistors. Protection features include desaturation, overcurrent sensing, and undervoltage detection. These drivers are available in dual–in–line and surface mount packages and include the following features:



- Undervoltage Lockout Optimized for IGBTs
- Input ties directly to an opto isolator
- High Current Output Stage: 1.0 A Source / 2.0 A Sink (MC33153)
  4.0 A Source / 2.0 A Sink (MC33154)
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Negative Gate Drive Capability
- Active high fault output capability



Typical Opto Isolated Gate Drive

Symbols, Terms and Definitions

The following are the most commonly used letter symbols, terms and definitions associated with IGBTs:

Symbol	Term	Definition
$V_{(BR)CER}$	collector–emitter breakdown voltage with (resistance between gate and emitter)	The breakdown voltage between the collector terminal and the emitter terminal when the gate terminal is (as indicated by the last subscript letter) as follows: R = returned to the emitter terminal through a specified resistance.
$V_{(BR)CES}$	gate short–circuited to emitter	S = short–circuited to the emitter terminal.
$V_{(BR)CEV}$	voltage between gate and emitter	V = returned to the emitter terminal through a specified voltage.
$V_{(BR)CEX}$	circuit between gate and emitter	X = returned to the emitter terminal through a specified circuit.
C_{ce}	collector–emitter capacitance	The capacitance between the collector and emitter terminals with the gate terminal connected to the guard terminal of a three–terminal bridge.
C_{cg}	collector–gate capacitance	The same as C_{res} — See C_{res}.
C_{ge}	gate–emitter capacitance	The capacitance between the gate and emitter terminals with the collector terminal connected to the guard terminal of a three–terminal bridge.
C_{ies}	short–circuit input capacitance, common–emitter	The capacitance between the input terminals (gate and emitter) with the collector short–circuited to the emitter for alternating current. (Ref. IEEE No. 255)
C_{oes}	short–circuit output capacitance, common–emitter	The capacitance between the output terminals (collector and emitter) with the gate short–circuited to the emitter for alternating current. (Ref. IEEE No. 255)
C_{res}	short–circuit reverse transfer capacitance, common–emitter	The capacitance between the collector and gate terminals with the emitter connected to the guard terminal of a three–terminal bridge.
E_{off}	turn–off energy loss	Energy loss during turn–off measured over a period of time that starts with 5% of test voltage and goes on for 5 μs.
E_{on}	turn–on energy loss	Energy loss during turn–on measured from 5% of test current to 5% of test voltage.
E_{ts}	total switching loss	The sum of turn–on and turn–off energy losses.
g_{FE}	common–emitter large–signal transconductance	The ratio of the change in collector current due to a change in gate–to–emitter voltage.
I_C	collector current, dc	The direct current into the collector terminal.
$I_{C(on)}$	on–state collector current	The direct current into the collector terminal with a specified forward gate–emitter voltage applied to bias the device to the on–state.
I_{CES}	zero–gate–voltage collector current	The direct current into the collector terminal when the gate–emitter voltage is zero.
I_G	gate current, dc	The direct current into the gate terminal.
I_{GESF}	forward gate current, collector short–circuited to emitter	The direct current into the gate terminal of an insulated–gate bipolar transistor with a forward gate–emitter voltage applied and the collector terminal short–circuited to the emitter terminal.

Symbol	Term	Definition
I_{GESR}	reverse gate current, collector short–circuited to emitter	The direct current into the gate terminal of an insulated–gate bipolar transistor with a reverse gate–emitter voltage applied and the collector terminal short–circuited to the emitter terminal.
I_E	emitter current, dc	The direct current into the emitter terminal.
P_T, P_D	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages.
Q_g	total gate charge	The total gate charge required to charge the IGBTs input capacitance to $V_{GE(on)}$.
Q_{gc}	gate–to–collector charge	The amount of charge required to charge the gate–to–collector capacitance to a specified value.
Q_{ge}	gate–to–emitter charge	The amount of charge required to charge the gate–to–emitter capacitance to a specified value.
$R_{CE(on)}$	static collector–emitter on–state resistance	The dc resistance between the collector and emitter terminals with a specified gate–emitter voltage applied to bias the device to the on state.
$R_{\theta CA}$	thermal resistance, case–to–ambient	The thermal resistance (steady–state) from the device case to the ambient.
$R_{\theta JA}$	thermal resistance, junction–to–ambient	The thermal resistance (steady–state) from the semiconductor junction(s) to the ambient.
$R_{\theta JC}$	thermal resistance, junction–to–case	The thermal resistance (steady–state) from the semiconductor junction(s) to a stated location on the case.
$R_{\theta JM}$	thermal resistance, junction–to–mounting surface	The thermal resistance (steady–state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	ambient temperature or free–air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.
T_C	case temperature	The temperature measured at a specified location on the case of a device.
t_c	turn–off crossover time	The time interval during which drain voltage rises from 10% of its peak off–state value and drain current falls to 10% of its peak on–state value, in both cases ignoring spikes that are not charge–carrier induced.
T_J	channel temperature	The temperature of the channel of an IGBT.
T_{stg}	storage temperature	The temperature at which the device, without any power applied, may be stored.
$t_{d(off)}$	turn–off delay time	Synonym for current turn–off delay time (see Note 1)*.
$t_{d(off)i}$	current turn–off delay time	The interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the collector current waveform falls to 90% of its on–state amplitude, ignoring spikes that are not charge–carrier induced.
$t_{d(off)v}$	voltage turn–off delay time	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the collector voltage waveform rises to 10% of its off–state amplitude, ignoring spikes that are not charge–carrier induced.

Symbol	Term	Definition
$t_{d(on)}$	turn–on delay time	Synonym for current turn–on delay time (see Note 1)*.
$t_{d(on)i}$	current turn–on delay time	The time interval during which can input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the collector current waveform rises to 10% of its on–state amplitude, ignoring spikes that are not charge–carrier induced.
$t_{d(on)v}$	voltage turn–on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the collector voltage waveform falls to 90% of its off–state amplitude, ignoring spikes that are not charge–carrier induced.
t_f	fall time	Synonym for current fall time (see Note 1)*.
t_{fi}	current fall time	The time interval during which the drain current changes from 90% to 10% of its peak off–state value, ignoring spikes that are not charge–carrier induced.
t_{fv}	voltage fall time	The time interval during which the drain voltage changes from 90% to 10% of its peak off–state value, ignoring spikes that are not charge–carrier induced.
t_{off}	turn–off time	Synonym for current turn–off time (see Note 1)*.
$t_{off(i)}$	current turn–off time	The sum of current turn–off delay time and current fall time, i.e., $t_{d(off)i} + t_{fi}$.
$t_{off(v)}$	voltage turn–off time	The sum of voltage turn–off delay time and voltage rise time, i.e., $t_{d(off)v} + t_{rv}$.
t_{on}	turn–on time	Synonym for current turn–on time (see Note 1)*.
$t_{on(i)}$	current turn–on time	The sum of current turn–on delay time and current rise time, i.e., $t_{d(on)i} + t_{ri}$.
$t_{on(v)}$	voltage turn–on time	The sum of voltage turn–on delay time and voltage fall time, i.e., $t_{d(on)v} + t_{fv}$.
t_p	pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform. **Note:** The two reference points are usually 90% of the steady–state amplitude of the waveform existing after the leading edge, measured with respect to the steady–state amplitude existing before the leading edge. If the reference points are 50% points, the symbol t_w and term average pulse duration should be used.
t_r	rise time	Synonym for current rise time (see Note 1)*.
t_{ri}	current rise time	The time interval during which the drain current changes from 10% to 90% of its peak on–state value, ignoring spikes that are not charge–carrier induced.
t_{rv}	voltage rise time	The time interval during which the collector voltage changes from 10% to 90% of its peak off–state value, ignoring spikes that are not charge–carrier induced.
t_{sc}	short circuit withstand time	The duration a device can withstand a short circuit at a specified temperature and gate bias.

Symbol	Term	Definition
t_W	average pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady–state amplitude of the waveform existing after the leading edge, measured with respect to the steady–state amplitude existing before the leading edge. **Note:** If the reference points are not 50% points, the symbol t_p and term pulse duration should be used.
$V_{(BR)GESF}$	forward gate–emitter breakdown voltage	The breakdown voltage between the gate and emitter terminals with a forward gate–emitter voltage applied and the collector terminal short–circuited to the emitter terminal.
$V_{(BR)GESR}$	reverse gate–emitter breakdown voltage	The breakdown voltage between the gate and emitter terminals with a reverse gate–emitter voltage applied and the collector terminal short–circuited to the emitter terminal.
V_{CC}, V_{GG} V_{EE}	supply voltage, dc (collector, gate, emitter) voltage	The dc supply voltage applied to a circuit or connected to the reference terminal.
V_{CG} V_{CE} V_{GC} V_{GE} V_{EC} V_{EG}	collector–to–gate collector–to–emitter gate–to–collector gate–to–emitter emitter–to–collector emitter–to–gate	The dc voltage between the terminal indicated by the first subscript and the reference terminal indicated by the second subscript (stated in terms of the polarity at the terminal indicated by the first subscript).
$V_{CE(on)}$	collector–emitter on–state voltage	The voltage between the collector and emitter terminals with a specified forward gate–emitter voltage applied to bias the device to the on state.
$V_{CE(sat)}$	collector–to–emitter saturation voltage	Voltage measured from collector–to–emitter at a specified collectorcurrent and gate–to–emitter voltage. Interchangeable with $V_{CE(on)}$ for IGBTs.
$V_{GE(th)}$	gate–emitter threshold voltage	The forward gate–emitter voltage at which the magnitude of the collector current of an enhancement–type insulated gate bipolar transistor has been increased to a specified low value.
$Z_{\theta JA(t)}$	transient thermal impedance, junction–to–ambient	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\theta JC(t)}$	transient thermal impedance, junction–to–case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Note 1: As names of time intervals for characterizing switching transistors, the terms “fall time” and “rise time” always refer to the change that is taking place in the magnitude of the output current even though measurements may be made using voltage waveforms. In a purely resistive circuit, the (current) rise time may be considered equal and coincident to the voltage fall time and the (current) fall time may be considered equal and coincident to the voltage rise time. The delay times for current and voltage will be equal and coincident. When significant amounts of inductance are present in a circuit, these equalities and coincidences no longer exist, and use of the unmodified terms delay time, fall time, and rise time must be avoided. See figures 1 and 2 for reference.

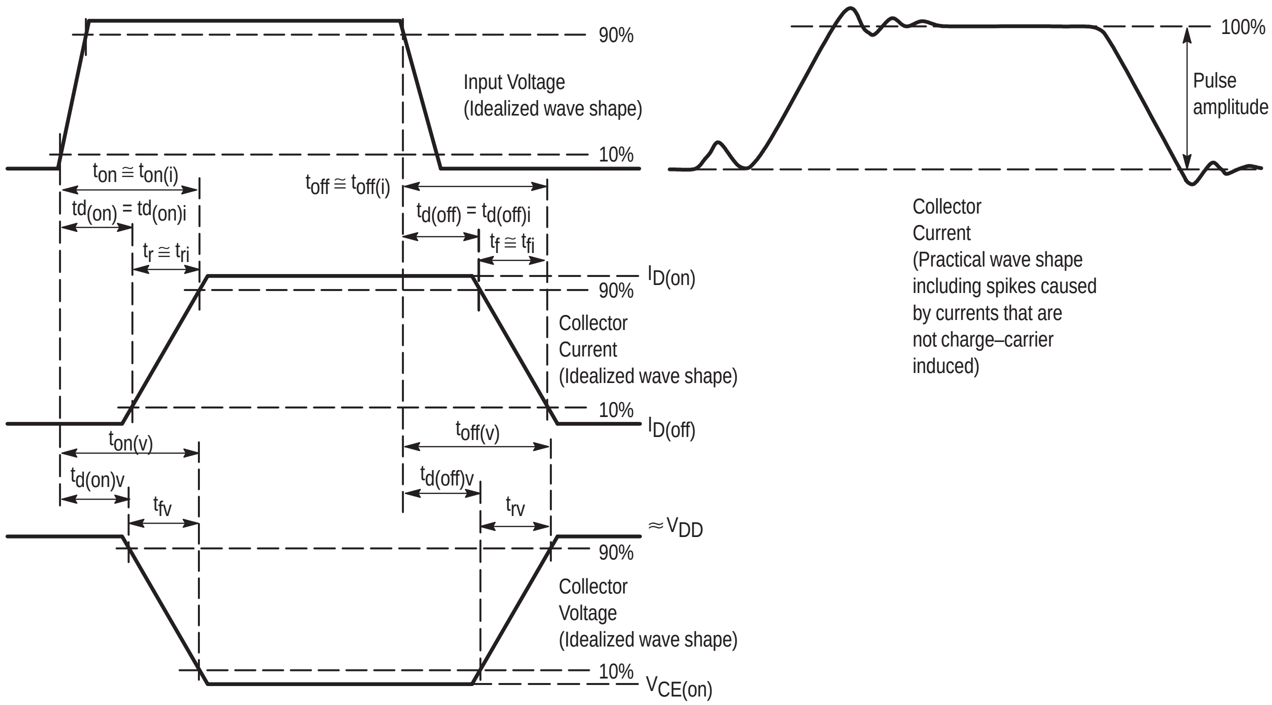
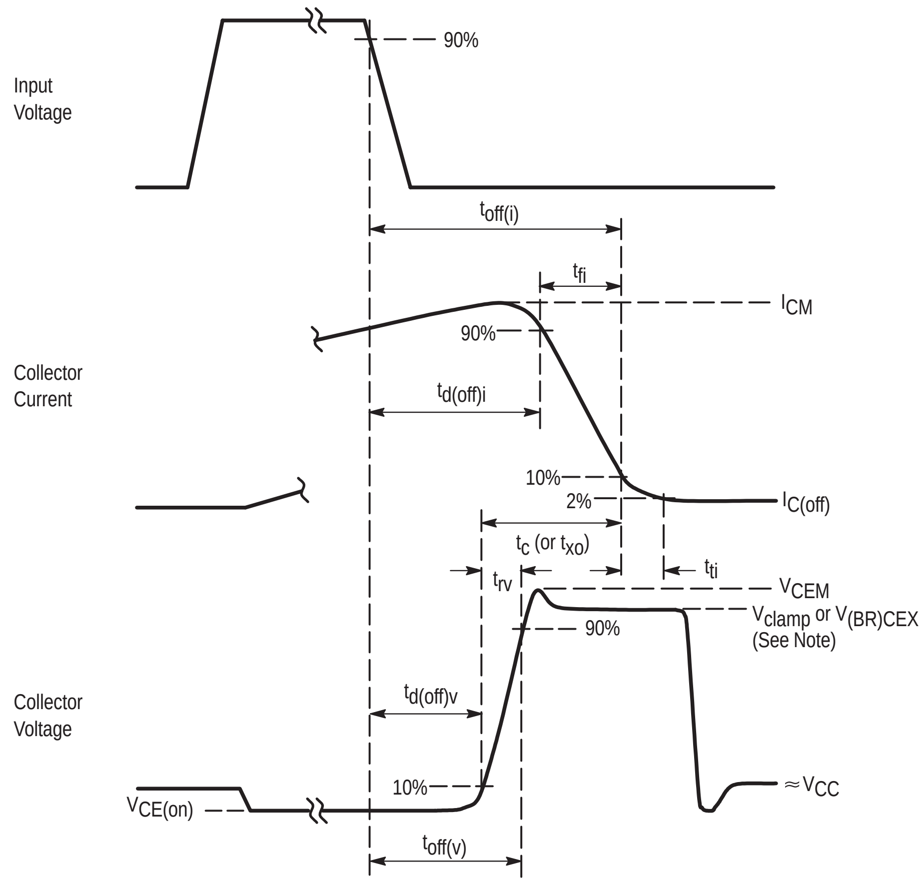


Figure 1. Waveforms for Resistive–Load Switching



NOTE: V_{clamp} (in a clamped inductive–load switching circuit) or $V_{(BR)CEX}$ (in an unclamped circuit) is the peak off–state voltage excluding spikes.

Figure 2. Waveforms for Inductive Load Switching, Turn–Off

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings represent the extreme capabilities of the device. They can best be described as device characterization boundaries and are given to facilitate "worst–case" design.

Collector–to–Emitter Voltage (V_{CES}, V_{CER}) This represents the lower limit of the device's blocking voltage capability from Collector–to–Emitter when the gate is shorted to the source (V_{CES}), or when a 1.0 MΩ Gate–to–Emitter resistor is present (V_{CER}). It is measured at a specific leakage current and has a positive temperature coefficient. The voltage across the IGBT should never exceed this rating in order to prevent breakdown of the Collector–to–Emitter junction.

Maximum Gate–to–Emitter Voltage (V_{GE}) The maximum allowable Gate–to–Emitter voltage. Exceeding this limit may result in permanent device degradation.

Continuous Collector Current (I_{C25}, I_{C90}) The dc current level that will raise the device's junction temperature to its rated maximum while its case temperature is held at either 25°C (I_{C25}), or 90°C (I_{C90}). This can be calculated by the equation:

$$I_{CX} = (T_{JMAX} - T_X) * (V_{CE(on)} @ T_{JMAX}) / R_{\theta JC}$$

where,

T_X	= Case temperature
$V_{CE(on)}$	= Device's "on" voltage
T_{JMAX}	= Device's maximum rated junction temperature
$R_{\theta JC}$	= Device's thermal resistance junction–to–case

Pulsed Collector Current (I_{CM}) The maximum allowable peak collector current the device can safely handle under a 10 μs pulsed condition. This rating takes into consideration the device's thermal limitation as well as $V_{CE(on)}$, wire bond and source metal limitations.

Maximum Power Dissipation (P_D) Specifies the power dissipation limit which takes the junction temperature to its maximum rating while the reference temperature is being held at 25° C. It is calculated by the following equation:

$$P_D = (T_{JMAX} - T_R)/R_{\theta JR}$$

where,

P_D	= Maximum power dissipation
T_{JMAX}	= Maximum allowable junction temperature
T_R	= Reference (case and or ambient) temperature
$R_{\theta JR}$	= Thermal resistance junction–to–reference (case or ambient)

Maximum Junction Temperature (T_{JMAX}) This value represents the maximum allowable junction temperature of the device. It is derived and based off of long term reliability data. Exceeding this value will only serve to shorten the device's long term operating life.

Short Circuit Withstand Time (t_{sc}) The permissible time, for given values of Collector–to–Emitter voltage, gate voltage and starting temperature, that the device can safely handle while in a shorted load condition.

Thermal Resistance ($R_{\theta JC}$, $R_{\theta JA}$) The quantity that resists or impedes the flow of heat energy in a device is called thermal resistance. Thermal resistance values are needed for proper thermal design. These values are measured as detailed in Section 3–8A.

ELECTRICAL CHARACTERISTICS

The intent of this section of the data sheet is to provide detailed device characterization information so that the designer can predict with a high degree of accuracy the behavior of the device in a specific application.

Collector–to–Emitter Breakdown Voltage ($V_{(BR)CES}$) This represents the lower limit of the device's blocking voltage capability from Collector–to–Emitter with the gate shorted to the source. It is measured at a specific leakage current and has a positive temperature coefficient.

Zero Gate Voltage Collector Current (I_{CES}) The direct current into the collector terminal of the device when the Gate–to–Emitter voltage is zero and the collector terminal is reversed biased with respect to the source terminal. This parameter generally increases with temperature as shown in the "Collector–to–Emitter Leakage Current versus Voltage" figure found in the device's data sheet.

Gate–Body Leakage Current (I_{GES}) The direct current flow in the gate terminal of the device when the gate terminal is biased with either a positive or negative voltage with respect to the source terminal and the collector terminal is short–circuited to the source terminal.

Gate Threshold Voltage ($V_{GE(th)}$) The forward Gate–to–Emitter voltage at which the magnitude of collector current has been increased to some low threshold value, usually specified as 250 μa or 1.0 ma. This parameter has a negative temperature coefficient.

Collector–to–Emitter On–Voltage ($V_{CE(on)}$) The dc voltage between the Collector–to–Emitter terminals at a specified collector current and with a Gate–to–Emitter voltage applied to bias the device into the on–state. This parameter has a positive temperature coefficient.

Forward Transconductance (g_{FE}) The ratio of the change in collector current due to a change in Gate–to–Emitter voltage (i.e., $\Delta I_E / \Delta V_{GE}$).

Device Capacitance (C_{ies}, C_{oes}, C_{res}) Power IGBT devices have internal parasitic capacitance from terminal–to–terminal. This capacitance is voltage dependent as shown by the "Capacitance Variation" figure in the device's data sheet. C_{iee} is the capacitance between the Gate–to–Emitter terminals with the collector terminal short–circuited to the source terminal for alternating current. C_{oee} is the capacitance between the Collector–to–Emitter terminals with the gate short–circuited to the source terminal for alternating current. C_{ree} is the capacitance between the Collector–to–Gate terminals with the source terminal connected to the guard terminal of a three–terminal bridge (Ref. IEEE No. 255). Figures 3, 4 and 5 show test circuits used for Power IGBT capacitance measurements.

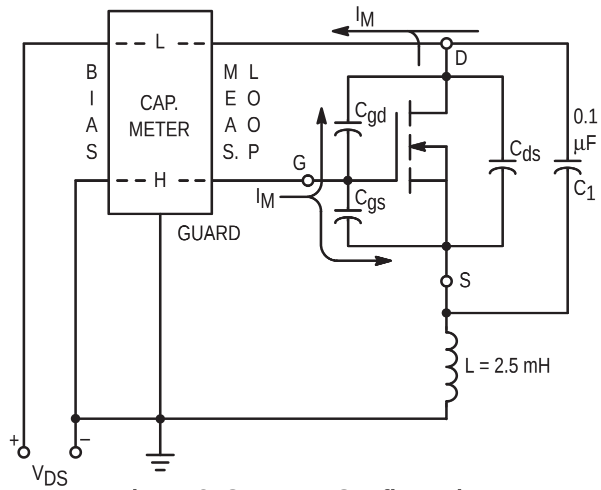


Figure 3. C_{ies} Test Configuration

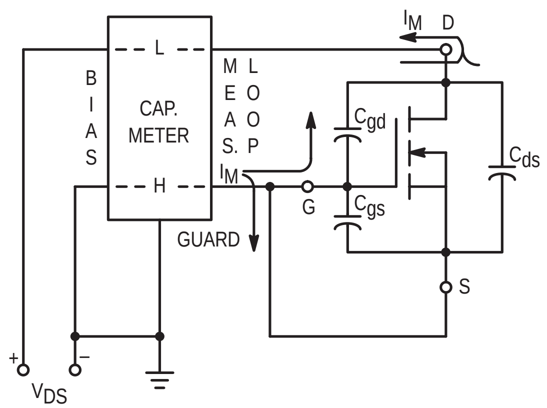


Figure 4. C_{oes} Test Configuration

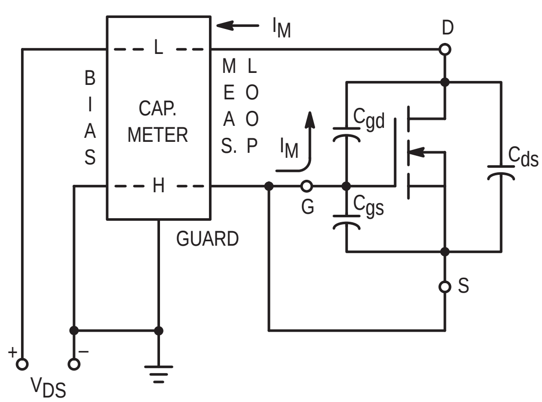


Figure 5. C_{res} Test Configuration

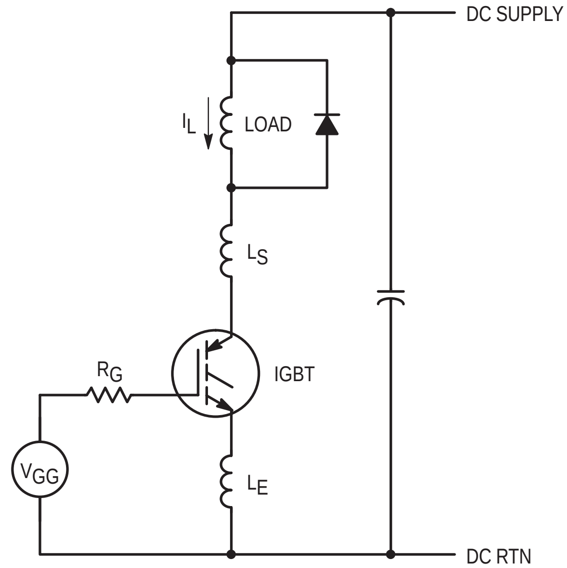


Figure 6. Switching Test Circuit

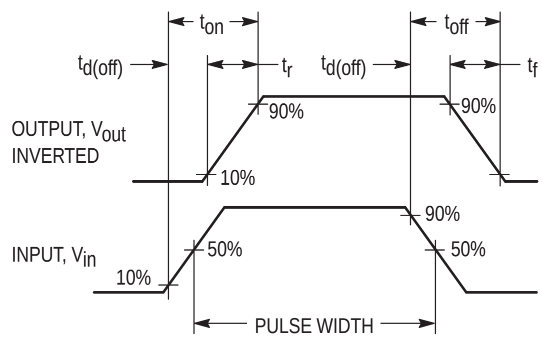


Figure 7. Switching Waveforms

Gate Charge (Q_T, Q_1, Q_2) Gate charge values are used to size the gate drive circuit. Q_T is defined as the total gate charge required to charge the device's input capacitance to the applied gate voltage. Q_1 is defined as the charge required to charge the device's input capacitance C_{GE} to the $V_{GS(on)}$ value required to maintain the test current I_C. Q_2 is defined as the charge time required to charge C_{GD} to the same value as C_{GE}.

InductiveSwitching($t_{d(on)}$,t_r,$t_{d(off)}$,t_f,E_{on},E_{off},E_{ts}) IGBT clamped inductive switching is tested and measured using the inductive switching test circuit as shown in Figure 6. A typical switching waveform showing parameter measurement points is shown in Figure 7. Switching values are listed for both 25°C and 125°C junction temperatures on the data sheet.

Diode Forward Voltage Drop (V_{FEC}) Co–Package IGBT devices contain an integral power diode between the Collector–to–Emitter terminals. The dc voltage between the Emitter–to–Collector terminals when the power diode is forward biased is called the diode forward voltage drop (V_{FEC}).

Reverse Recovery Time (t_{rr}, t_a, t_b, Q_{RR}) Co–Package IGBT devices contain an integral power diode. A power diode is a minority carrier device and thus has a finite reverse recovery time. t_a is defined as the time between the dropping I_S current's zero crossing point to the peak I_{RM}. t_b is defined as the time between the peak I_{RM} to a projected I_{RM} zero current crossing point through a 25% I_{RM} projection as shown in Figure 8. Total reverse recovery time, t_{rr}, is defined as the sum of t_a and t_b. Q_{RR} is defined as the integral of the area made up by the I_{RM} waveform and V_R, the reapplied blocking voltage which forces reverse recovery. A relative softness factor s, is defined as the ratio of t_b to t_a. General purpose rectifiers have a softness factor of around 1.0, fast recovery rectifiers have a softness factor of approximately 0.5 and ultra fast rectifiers are very abrupt and have a softness factor of around 0.2. The tradeoff is the rectifier speed versus softness. The higher the softness factor, the less undesirable induced voltages in switching circuits. Diode reverse recovery values are listed for both 25°C and 125°C junction temperatures on the data sheet.

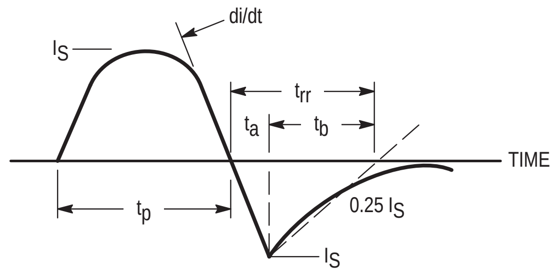


Figure 8. Diode Reverse Recovery Waveform

Chapter Three
Theory and Applications

Page

Section 1
Introduction to Insulated Gate Bipolar Transistors

INTRODUCTION

As power conversion relies more on switched applications, semiconductor manufacturers need to create products that approach the ideal switch. The ideal switch would have: 1) zero resistance or forward voltage drop in the on–state, 2) infinite resistance in the off–state, 3) switch with infinite speed, and 4) would not require any input power to make it switch.

When using existing solid–state switch technologies, the designer must deviate from the ideal switch and choose a device that best suits the application with a minimal loss of efficiency. The choice involves considerations such as voltage, current, switching speed, drive circuitry, load, and temperature effects. There are a variety of solid state switch technologies available to perform switching functions; however, all have strong and weak points.

HIGH VOLTAGE POWER MOSFETs

The primary characteristics that are most desirable in a solid–state switch are fast switching speed, simple drive requirements and low conduction loss. For low voltage applications, power MOSFETs offer extremely low on–resistance, $R_{DS(on)}$, and approach the desired ideal switch. In high voltage applications, MOSFETs exhibit increased $R_{DS(on)}$ resulting in lower efficiency due to increased conduction losses. In a power MOSFET, the on–resistance is proportional to the breakdown voltage raised to approximately the 2.7 power (1).

MOSFET technology has advanced to a point where cell densities are limited by manufacturing equipment capabilities and geometries have been optimized to a point where the $R_{DS(on)}$ is near the predicted theoretical limit. Since the cell density, geometry and the resistivity of the device structure play a major role, no significant reduction in the $R_{DS(on)}$ is foreseen. New technologies are needed to circumvent the problem of increased on–resistance without sacrificing switching speed.

$$R_{DS(on)} \propto V_{DSS}^{2.7} \qquad (1)$$

ENTER THE IGBT

By combining the low conduction loss of a BJT with the switching speed of a power MOSFET an optimal solid state switch would exist. The Insulated Gate Bipolar Transistor (IGBT) technology offers a combination of these attributes.

The IGBT is, in fact, a spin–off from power MOSFET technology and the structure of an IGBT closely resembles that of a power MOSFET. The IGBT has high input impedance and fast turn–on speed like a MOSFET. IGBTs exhibit an on–voltage and current density comparable to a bipolar transistor while switching much faster. IGBTs are replacing MOSFETs in high voltage applications where conduction losses must be kept low. With zero current switching or resonant switching techniques, the IGBT can be operated in the hundreds of kilohertz range [1].

Although turn–on speeds are very fast, turn–off of the IGBT is slower than a MOSFET. The IGBT exhibits a current fall time or “tailing.” The tailing restricts the devices to operating at moderate frequencies (less than 50 kHz) in traditional “square waveform” PWM, switching applications.

At operating frequencies between 1 and 50 kHz, IGBTs offer an attractive solution over the traditional bipolar transistors, MOSFETs and thyristors. Compared to thyristors, the IGBT is faster, has better dv/dt immunity and, above all, has better gate turn–off capability. While some thyristors such as GTOs are capable of being turned off at the gate, substantial reverse gate current is required, whereas turning off an IGBT only requires that the gate capacitance be discharged. A thyristor has a slightly lower forward–on voltage and higher surge capability than an IGBT.

MOSFETs are often used because of their simple gate drive requirements. Since the structure of both devices are so similar, the change to IGBTs can be made without having to redesign the gate drive circuit. IGBTs, like MOSFETs, are transconductance devices and can remain fully on by keeping the gate voltage above a certain threshold.

As shown in Figure 1–1a, using an IGBT in place of a power MOSFET dramatically reduces the forward voltage drop at current levels above 12 amps. By reducing the forward drop, the conduction loss of the device is decreased. The gradual rising slope of the MOSFET in Figure 1–1a can be attributed to the relationship of V_{DS} to $R_{DS(on)}$. The IGBT curve has an offset due to an internal forward biased p–n junction and a fast rising slope typical of a minority carrier device.

It is possible to replace the MOSFET with an IGBT and improve the efficiency and/or reduce the cost. As shown in Figure 1–1b, an IGBT has considerably less silicon area than a similarly rated MOSFET. Device cost is related to silicon area; therefore, the reduced silicon area makes the IGBT the lower cost solution. Figure 1–1c shows the resulting package area reduction realized by using the IGBT. The IGBT is more space efficient than an equivalently rated MOSFET which makes it perfect for space conscious designs.

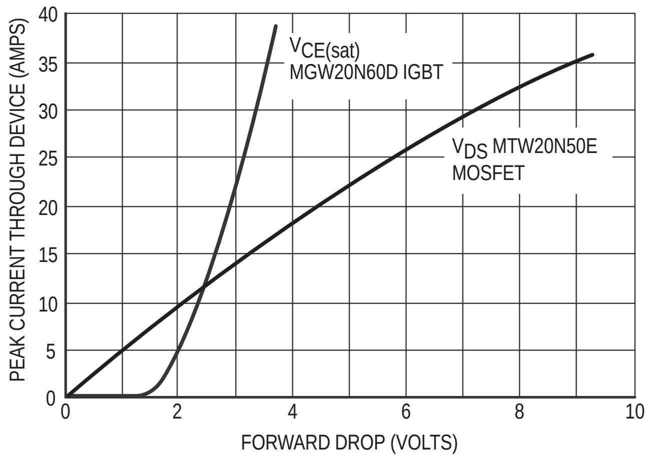


Figure 1–1a. Reduced Forward Voltage Drop of IGBT Realized When Compared to a MOSFET with Similar Ratings

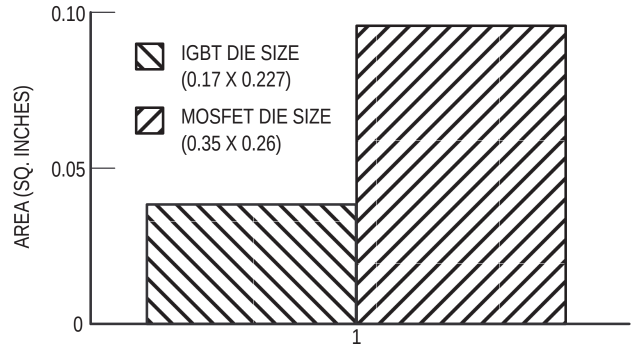


Figure 1–1b. Reduced Die Size of IGBT Realized When Compared to a MOSFET with Similar Ratings

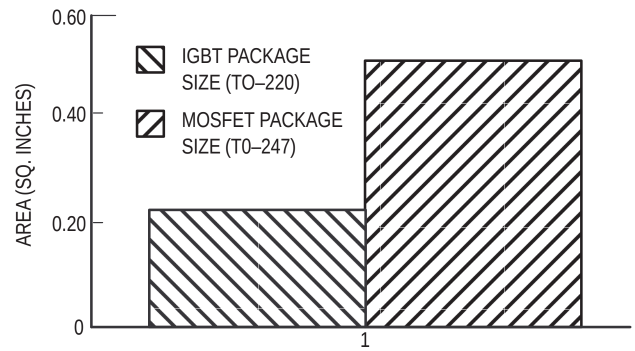


Figure 1–1c. Reduced Package Size of IGBT Realized When Compared to a MOSFET with Similar Ratings

When compared to BJTs, IGBTs have similar ratings in terms of voltage and current. However, the presence of an isolated gate in an IGBT makes it simpler to drive than a BJT. BJTs require that base current be continuously supplied in a quantity sufficient enough to maintain saturation. Base currents of one–tenth of the collector current are typical to keep a BJT in saturation. BJT drive circuits must be sensitive to variable load conditions. The base current of a BJT must be kept proportional to the collector current to prevent desaturation under high–current loads and excessive base drive under low–load conditions. This additional base current increases the power dissipation of the drive circuit. BJTs are minority carrier devices and charge storage effects including recombination slow the performance when compared to majority carrier devices such as MOSFETs. IGBTs also experience recombination that accounts for the current "tailing" yet IGBTs have been observed to switch faster than BJTs.

Thus far, the IGBT has demonstrated certain advantages over power MOSFETs with the exception of switching speed. Since the initial introduction of IGBTs in the early 1980s, semiconductor manufacturers have learned how to make the devices faster. As illustrated in Figure 1–2, some trade–offs in conduction loss versus switching speed exist. Lower frequency applications can tolerate slower switching devices. Because the loss period is a small percentage of the total on time, slower switching is traded for lower conduction loss. In a higher frequency application, just the opposite would be true and the device would be made faster and have greater conduction losses. Notice that the curves in Figure 1–2 show reductions in both the forward drop ($V_{CE(sat)}$) and the fall time, t_f of newer generation devices. These capabilities make the IGBT the device of choice for applications such as motor drives, power supplies and inverters that require devices rated for 600 to 1200 volts.

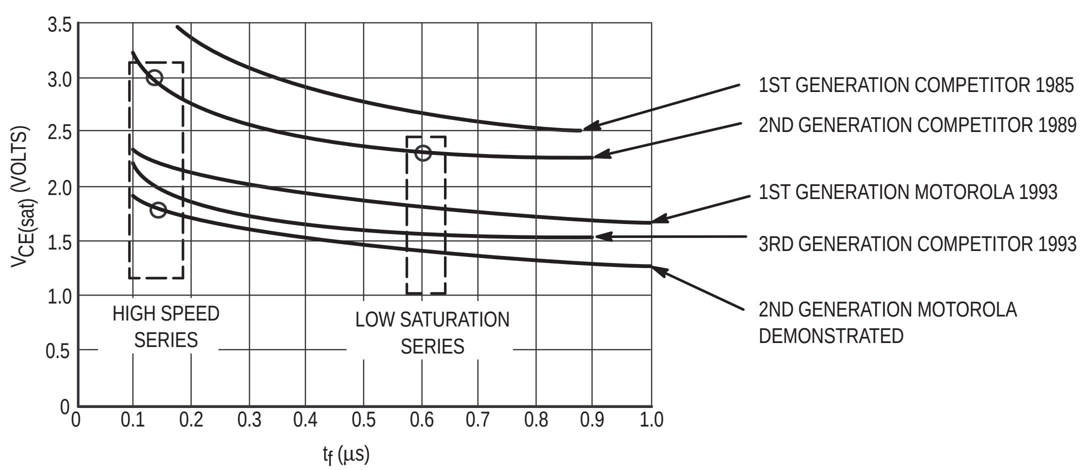


Figure 1–2. Advanced Features Offered by the Latest Motorola IGBT Technologies for Forward Voltage Drop ($V_{CE(sat)}$) and Fall Time (t_f)

CHARACTERISTICS OF IGBTs

Device Structure

The structure of an IGBT is similar to that of a double diffused (DMOS) power MOSFET. One difference between a MOSFET and an IGBT is the substrate of the starting material. By varying the starting material and altering certain process steps, an IGBT may be produced from a power MOSFET mask; however, at Motorola mask sets are designed specifically for IGBTs. In a MOSFET the substrate is N+ as shown in Figure 1–3b. The substrate for an IGBT is P^+ as shown in Figure 1–3a.

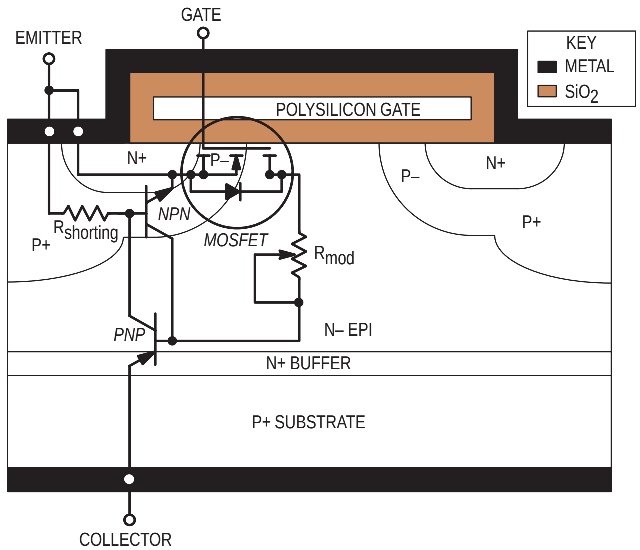


Figure 1–3a. Cross Section and Equivalent Schematic of an Insulated Gate Bipolar Transistor (IGBT) Cell

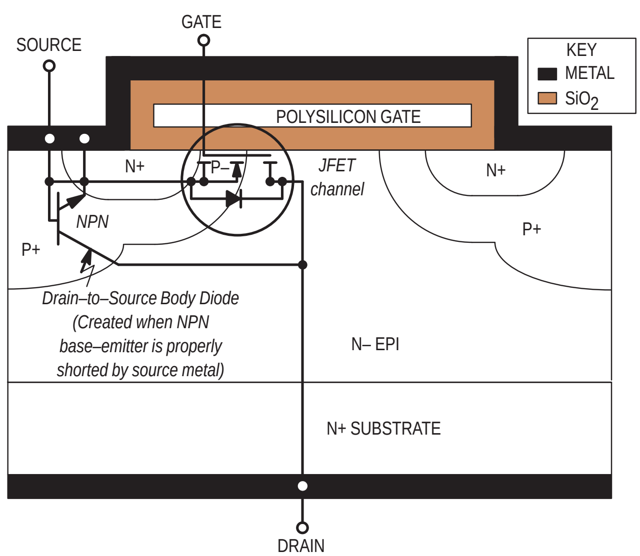


Figure 1–3b. Cross Section and Equivalent Schematic of an Metal–Oxide–Semiconductor Field–Effect Transistor (MOSFET) Cell

The n– epi resistivity determines the breakdown voltage of a MOSFET as mentioned earlier using relationship (1).

To increase the breakdown voltage of the MOSFET, the n– epi region thickness (vertical direction in figure) is increased. As depicted in the classical resistance relationship (2), reducing the $R_{DS(on)}$ of a high voltage device requires greater silicon area *A* to make up for the increased n– epi region.

$$R \propto \frac{1}{A} \qquad (2)$$

Device designers were challenged to overcome the effects of the high resistive n– epi region. The solution to this came in the form of conductivity modulation. The n– epi region to this was placed on the P^+ substrate forming a p–n junction where conductivity modulation takes place. Because of conductivity modulation, the IGBT has a much greater current density than a power MOSFET and the forward voltage drop is reduced. Now the P^+ substrate, n– epi layer and P^+ "emitter" form a BJT transistor and the n– epi acts as a wide base region.

The subject of current tailing has been mentioned several times. Thus far, the device structure as shown in Figure 1–3 provides insight as to what causes the tailing. Minority carriers build up to form the basis for conductivity modulation. When the device turns off, these carriers do not have a current path to exit the device. Recombination is the only way to eliminate the stored charge resulting from the build–up of excess carriers. Additional recombination centers are formed by placing an N^+ buffer layer between the n– epi and P^+ substrate.

While the N^+ buffer layer may speed up the recombination, it also increases the forward drop of the device. Hence the tradeoff between switching speed and conduction loss becomes a factor in optimizing device performance. Additional benefits of the N^+ buffer layer include preventing thermal runaway and punch–through of the depletion region. This allows a thinner n– epi to be used which somewhat decreases forward voltage drop.

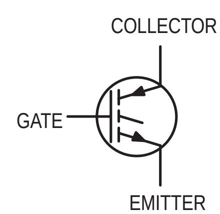


Figure 1–4a. IGBT Schematic Symbol

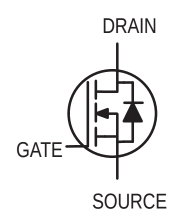


Figure 1–4b. MOSFET Schematic Symbol

The IGBT has a four layer (P–N–P–N) structure. This structure resembles that of a thyristor device known as a Silicon Controlled Rectifier (SCR). Unlike the SCR where the device latches and gate control is lost, an IGBT is designed so that it does not latch on. Full control of the device can be maintained through the gate drive.

To maximize the performance of the IGBT, process steps are optimized to control the geometry, doping and lifetime. The possibility of latching is also reduced by strategic processing of the device. Geometry and doping levels are optimized to minimize the on–voltage, switching speed and achieve other key parametric variations. Because the IGBT is a four–layer structure, it does not have the inverse parallel diode inherent to power MOSFETs. This is a disadvantage to motor control designers who use the anti–parallel diode to recover energy from the motor.

Like a power MOSFET, the gate of the IGBT is electrically isolated from the rest of the chip by a thin layer of silicon dioxide, SiO_2. The IGBT has a high input impedance due to the isolated gate and it exhibits the accompanying advantages of modest gate drive requirements and excellent gate drive efficiency.

Equivalent Circuit of IGBT

Figure 1–4a shows the terminals of the IGBT as determined by JEDEC. Notice that the IGBT has a gate like a MOSFET yet it has an emitter and a collector like a BJT.

The operation of the IGBT is best understood by again referring to the cross section of the device and its equivalent circuit as shown in Figure 1–3a. Current flowing from collector to emitter must pass through a p–n junction formed by the P^+ substrate and n– epi layer. This drop is similar to that seen in a forward biased p–n junction diode and results in an offset voltage in the output characteristic. Current flow contributions are shown in Figure 1–3a using varying line thickness with the thicker lines indicating a high current path. For a fast device, the N+ buffer layer is highly doped for recombination and speedy turn off. The additional doping keeps the gain of the PNP low and allows two–thirds of the current to flow through the base of the PNP (electron current) while one–third passes through the collector (hole current).

$R_{shorting}$ is the parasitic resistance of the P^+ emitter region. Current flowing through $R_{shorting}$ can result in a voltage across the base–emitter junction of the NPN. If the base–emitter voltage is above a certain threshold level, the NPN will begin to conduct causing the NPN and PNP to enhance each other's current flow and both devices can become saturated. This results in the device latching in a fashion similar to an SCR. Device processing directs currents within the device and keeps the voltage across $R_{shorting}$ low to avoid latching. The IGBT can be gated off unlike the SCR which has to wait for the current to cease allowing recombination to take place in order to turn off. IGBTs offer an advantage over the SCR by controlling the current with the device, not the device with the current. The internal MOSFET of the IGBT when gated off will stop current flow and at that point, the stored charges can only be dissipated through recombination.

The IGBT's on–voltage is represented by sum of the offset voltage of the collector to base junction of the PNP transistor, the voltage drop across the modulated resistance R_{mod} and the channel resistance of the internal MOSFET. Unlike the MOSFET where increased temperature results in increased $R_{DS(on)}$ and increased forward voltage drop, the forward drop of an IGBT stays relatively unchanged at increased temperatures.

Switching Speed

Until recently, the feature that limited the IGBT from serving a wide variety of applications was its relatively slow turn–off speed when compared to a power MOSFET. While turn–on is fairly rapid, initial IGBTs had current fall times of around three microseconds.

The turn–off time of an IGBT is slow because many minority carriers are stored in the n– epi region. When the gate is initially brought below the threshold voltage, the n– epi contains a very large concentration of electrons and there will be significant injection into the P^+ substrate and a corresponding hole injection into the n– epi. As the electron concentration in the n–region decreases, the electron injection decreases, leaving the rest of the electrons to recombine. Therefore, the turn–off of an IGBT has two phases: an injection phase where the collector current falls very quickly, and a recombination phase in which the collector current decrease more slowly. Figure 1–5 shows the switching waveform and the tail time contributing factors of a "fast" IGBT designed for PWM motor control service.

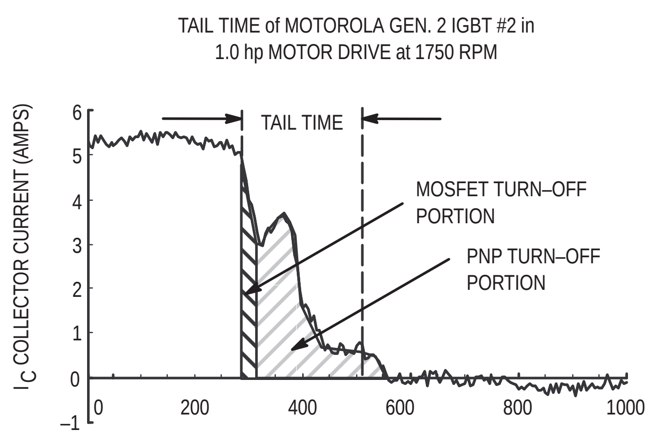


Figure 1–5. IGBT Current Turn–off Waveform

In power MOSFETs, the switching speed can be greatly affected by the impedance in the gate drive circuit. Efforts to minimize gate drive impedance for IGBTs are also recommended. Also, choose an optimal device based on switching speed or use a slower device with lower forward drop and employ external circuitry to enhance turn off. A turn–off mechanism is suggested in a paper by Baliga et al [2].

A FINAL COMPARISON OF IGBTs, BJTs AND POWER MOSFETs

The conduction losses of BJTs and IGBTs is related to the forward voltage drop of the device while MOSFETs determine conduction loss based on $R_{DS(on)}$. To get a relative comparison of turn–off time and conduction associated losses, data is presented in Table 1 where the on–resistances of a power MOSFET, an IGBT and a BJT at junction temperatures of 25°C and 150°C are shown.

Note that the devices in Table 1 have approximately the same ratings. However, to achieve these ratings the chip size of the devices vary significantly. The bipolar transistor requires 1.2 times more silicon area than the IGBT and the MOSFET requires 2.2 times the area of the IGBT to achieve the same ratings. This differences in die area directly impacts the cost of the product. At higher currents and at elevated temperatures, the IGBT offers low forward drop and a switching time similar to the BJT without the drive difficulties. Table 1 confirms the findings offered earlier in Figure 1–1a and elaborates further to include a BJT comparison and temperature effects. The reduced power conduction losses offered by the IGBT lower power dissipation and heat sink size.

Thermal Resistance

An IGBT and power MOSFET produced from the same size die have similar junction–to–case thermal resistance because of their similar structures. The thermal resistance of a power MOSFET can be determined by testing for variations in temperature sensitive parameters (TSPs). These parameters are the source–to–drain diode on–voltage, the gate–to–source threshold voltage, and the drain–to–source on–resistance. All previous measurements of thermal resistance of power MOSFETs at Motorola were performed using the source–to–drain diode as the TSP. Since an IGBT does not have an inverse parallel diode, another TSP had to be used to determine the thermal resistance. The gate–to–emitter threshold voltage was used as the TSP to measure the junction temperature of an IGBT to determine its thermal resistance. However before testing IGBTs, a correlation between the two test methods was established by comparing the test results of MOSFETs using both TSPs. By testing for variations in threshold voltage, it was determined that the thermal resistance of MOSFETs and IGBTs are essentially the same for devices with equivalent die size.

Short Circuit Rated Devices

Using IGBTs in motor control environments requires the device to withstand short circuit current for a given period. Although this period varies with the application, a typical value of ten microseconds is used for designing these specialized IGBT's. Notice that this is only a typical value and it is suggested that the reader confirm the value given on the data sheet. IGBTs can be made to withstand short circuit conditions by altering the device structure to include an additional resistance, R_e, (Figure 1–6) in the main current path. The benefits associated with the additional series resistance are twofold.

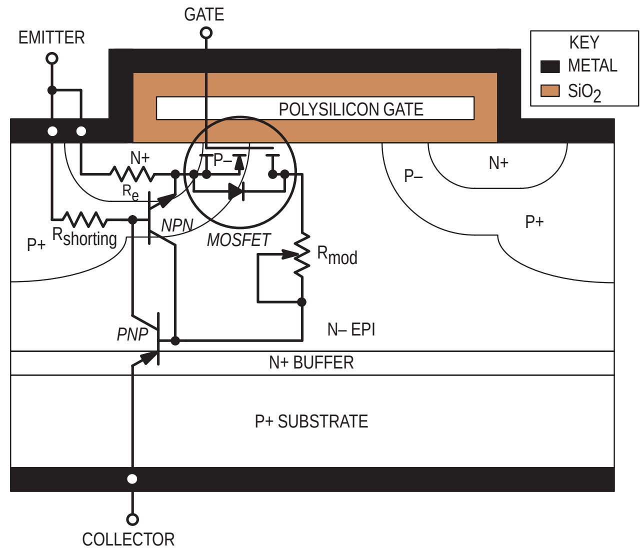


Figure 1–6. Cross Section and Equivalent Schematic of a Short Circuit Rated Insulated Gate Bipolar Transistor Cell

First, the voltage created across R_e, by the large current passing through R_e, increases the percentage of the gate voltage across R_e, by the classic voltage divider equation. Assuming the drive voltage applied to the gate–to–emitter remains the same, the voltage actually applied across the gate–to–source portion of the device is now lower, and the device is operating in an area of the transconductance curve that reduces the gain and it will pass less current.

Second, the voltage developed across R_e results in a similar division of voltage across $R_{shorting}$ and V_{BE} of the NPN transistor. The NPN will be less likely to attain a V_{BE} high enough to turn the device on and cause a latch–up situation.

The two situations described work together to protect the device from catastrophic failure. The protection period is specified with the device ratings, allowing circuit designers the time needed to detect a fault and shut off the device.

Table 10. Advantages Offered by the IGBT When Comparing the MOSFET, IGBT and Bipolar Transistor On–Resistances (Over Junction Temperature) and Fall Times (Resistance Values at 10 Amps of Current)

Characteristic	TMOS	IGBT	Bipolar
Current Rating	20 A	20 A	20 A
Voltage Rating	500 V	600 V	500 V*
$R_{(on)}$ @ T_J = 25°C	0.2 Ω	0.24 Ω	0.18 Ω
$R_{(on)}$ @ T_J = 150°C	0.6 Ω	0.23 Ω	0.24 Ω**
Fall Time (Typical)	40 ns	200 ns	200 ns

* Indicates V_{CEO} Rating
** BJT T_J = 100°C

The introduction of the series resistance R_e also results in additional power loss in the device by slightly elevating the forward drop of the device. However, the magnitude of short circuit current is large enough to require a very low R_e value. The additional conduction loss of the device due to the presence of R_e is not excessive when comparing a short circuit rated IGBT to a non–short circuit rated device.

Anti–Parallel Diode

When using IGBT's for motor control, designers have to place a diode in anti–parallel across the device in order to handle the regenerative or inductive currents of the motor. As discussed earlier, due to structural differences the IGBT does not have a parasitic diode like that found in a MOSFET. Designers found that the diode within the MOSFET was, in fact, a parasitic, i.e., not optimized in the design process, and its performance was poor for use as a current recovery device due to slow switching speed. To overcome the lack of performance, an optimized anti–parallel diode was used across the MOSFET source–to–drain. Placing a packaged diode external to the MOSFET itself created performance problems due to the switching delays resulting from the parasitics introduced by the packages. The optimal setup is to have the diode copackaged with the device. A specific line of IGBTs has been created by Motorola to address this issue. These devices work very well in applications where energy is recovered to the source and are favored by motor control designers.

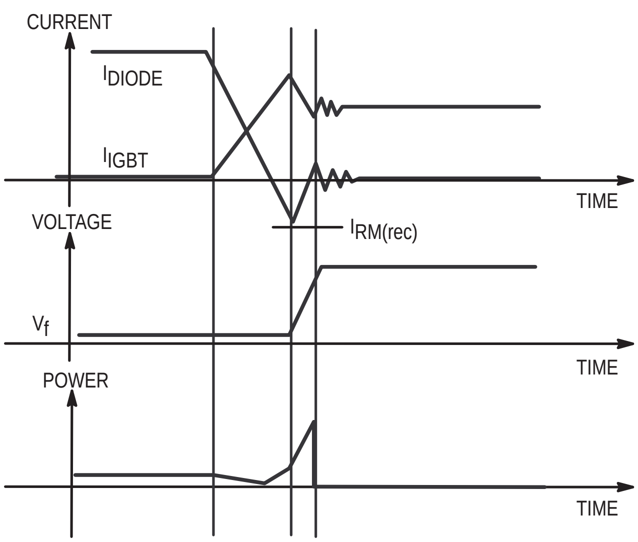


Figure 1–7. Waveforms Associated with Anti–Parallel Diode Turn–off

Like the switching device itself, the anti–parallel diode should exhibit low leakage current, low forward voltage drop and fast switching speed. As shown in Figure 1–7, the diode forward drop multiplied by the average current it passes is the total conduction loss produced. In addition, large reverse recovery currents can escalate switching losses. A detailed explanation of reverse recovery can be found in the Appendix. A secondary effect caused by large reverse recovery currents is generated EMI at both the switching frequency and the frequency of the resulting ringing waveform. This EMI requires additional filtering to be designed into the circuit. By copackaging parts, the parasitic inductances that contribute to the ringing are greatly reduced. Also, copackaged products can be used in designs to reduce power dissipation and increase design efficiency.

APPLICATION OF IGBTs: PULSE WIDTH MODULATED INDUCTION MOTOR DRIVE APPLICATION

Line–operated, pulse–width modulated, variable–speed motor drives are an application well suited for IGBTs. In this application, as shown in Figure 1–8, IGBTs are used as the power switch to PWM the voltage supplied to a motor to control its speed.

Depending on the application, the IGBT may be required to operate from a full–wave rectified line. This can require devices to have six hundred volt ratings for 230 VAC line voltage inputs, and twelve hundred volt ratings for 575 VAC volt line inputs. IGBTs that block high voltage offer fast switching and low conduction losses, and allow for the design of efficient, high frequency drives of this type. Devices used in motor drive applications must be robust and capable of withstanding faults long enough for a protection scheme to be activated. Short circuit rated devices offer safe, reliable motor drive operation.

CONCLUSION

The IGBT is a one of several options for designers to choose from for power control in switching applications. The features of the IGBT such as high voltage capability, low on–resistance, ease of drive and relatively fast switching speeds makes it a technology of choice for moderate speed, high voltage applications. New generations of devices will reduce the on–resistance, increase speed and include levels of integration that simplify protection schemes and device drive requirements. The reliability and performance advantages of IGBTs are value added traits that offer circuit designers energy efficient options at reduced costs.

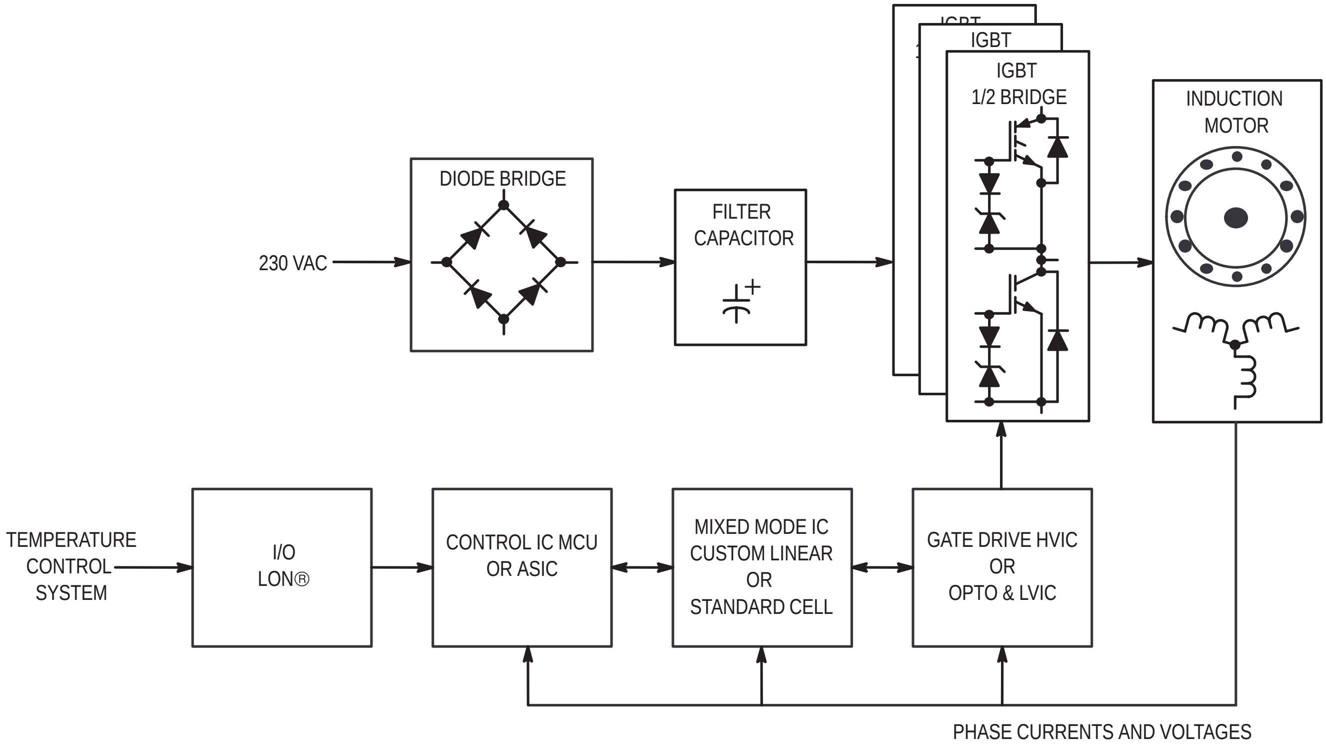


Figure 1–8. Typical Pulse–Width, Modulated, Variable–Speed Induction Motor Drives Are Where IGBT's Offer Performance Advantages

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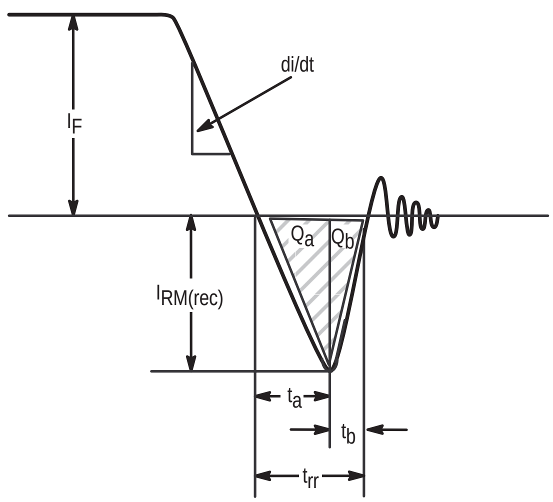
Diode Reverse Recovery Analysis [4]



t_{rr} = total reverse recovery time
t_a = fall time due to stored minority charge
t_b = application and device dependent
$I_{RM(rec)}$ = peak reverse recovery current

Figure 1–9 Reverse Recovery Waveform

A typical reverse recovery waveform is shown in Figure 1–9. The reverse recovery time t_{rr} has been traditionally defined as the time from diode current zero–crossing to where the current returns to within 10% of the peak recovery current $I_{RM(rec)}$. This does not give enough information to fully characterize the waveform shape. A better way to characterize the rectifier reverse recovery is to partition the reverse recovery time into two different regions, t_a and t_b, as shown in Figure 1–9. The t_a time is a function of the forward current and the applied di/dt. A charge can be assigned to this region denoted Q_a, the area under the curve. The t_b portion of the reverse recovery current is not very well understood. Measured t_b times vary greatly with the switch characteristic, circuit parasitics, load inductance and the applied reverse voltage. A relative softness can be defined as the ratio of t_b to t_a. General purpose rectifiers are very soft (softness factor of about 1.0), fast recovery diodes are fairly soft (softness factor of about 0.5) and ultrafast rectifiers are very abrupt (softness factor of about 0.2).

[4] *Source*: “Motor Controls,” *TMOS Power MOSFET Transistor Data, Q4/92, DL135, Rev 4*, (Phoenix: Motorola, Inc., 1992), pp. 2–9–22 to 2–9–23.

Section 2
Device Physics of the IGBT

INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) evolved from the vertical power MOSFET in the mid–1980's. The simple addition of an extra P–N junction to the drain of the MOSFET changes this unipolar device into a Bipolar Junction Transistor. However, because of the MOS gate structure, this BJT is a voltage controlled device.

This combination of a insulated gate input and bipolar output makes the IGBT an excellent power switch for medium frequency (2–20 kilohertz) and medium voltage (200–2000 V) applications. Improvements in device design and semiconductor processing continue to increase the IGBT's frequency and voltage capability. The amperage capability is only limited by the paralleling of large area IGBT's in multiple die modules.

The following sections discuss the design and operation of discrete vertical power IGBT's as large signal switches. Lateral IGBT's are commercially available in integrated circuits, but have higher on–state losses than the vertical structure, and so the lateral IGBT is mostly used for low power applications. Power IGBT's are not generally used for small–signal amplification, so this discussion will emphasize the blocking, conduction, and large–signal switching of the IGBT. Lastly, The Safe Operating Area and temperature effects of the IGBT will be examined.

DEVICE STRUCTURE

Vertical cross–sections of a planar N–channel IGBT are shown in Figure 2–1. Complementary P–channel IGBT's also exist, but have higher on–state losses and latch–up more easily than N–channel IGBT's. These cross–sections show a single IGBT cell, typically 20 to 40 µm wide and capable of conducting 1 to 2 mA, depending on the voltage rating. Like a power MOSFET, thousands of these cells are paralleled on the semiconductor die to achieve the desired current rating. Not shown in Figure 2–1 are the high voltage termination and bonding area for electrically and thermally connecting the IGBT to a three terminal package.

Figure 2–1a shows the basic IGBT vertical structure and its equivalent circuit. Below the MOSFET gate structure, the IGBT is composed of a four layer NPNP semiconductor. The parasitic NPN transistor is designed to be inactive, as its emitter–base junction is shorted out by the MOSFET source metal. Therefore the basic IGBT is a vertical wide–base PNP transistor, with its base drive provided by the surface MOSFET. The simple four layer device of Figure 2–1a has several drawbacks affecting switching and SOA.

To overcome these limitations, most modern IGBT's utilize one of two modified vertical structures. The first of these is the Punch–Thru IGBT shown in Figure 2–1b. PT–IGBT's have an extra N+ region epitaxially grown on the thick P+ substrate prior to the N– epitaxy. During the off–state, the blocking voltage (BV_{ces}) completely depletes the N– region, "punching–thru" to the N+ layer. The additional N+ buffer layer prevents "reach–thru" (voltage collapse from collector to emitter) to the P+ substrate, but allows a relatively thin N– region which minimizes $V_{CE(on)}$ while maximizing $V_{(BR)CES}$. The N+ region also improves the switching speed of the IGBT by reducing excess hole injection from the P+ substrate. The PT–IGBT also has a heavy P+ tub in the emitter region, which improves the VBE shorting of the parasitic NPN, for improved SOA. PT–IGBT's are typically available from 300 V to 1200 V $V_{(BR)CES}$ rating.

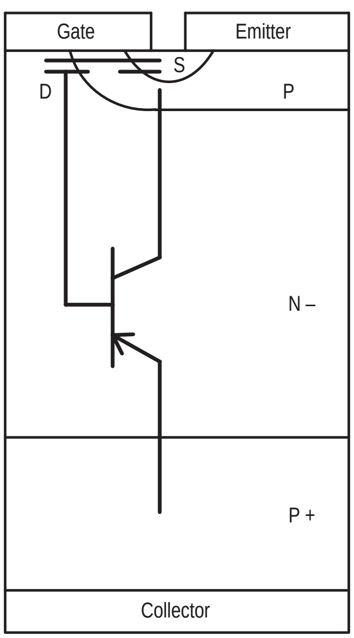


Figure 2–1a. Basic IGBT

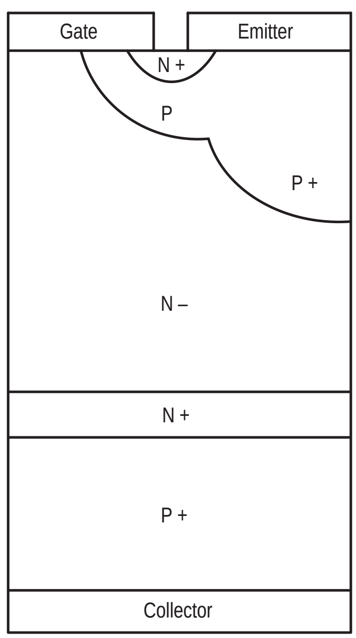


Figure 2–1b. PT–IGBT

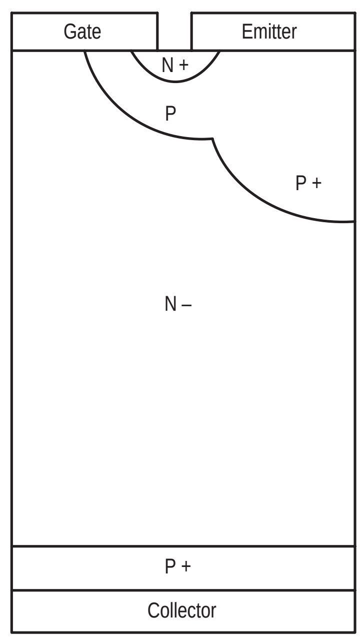


Figure 2–1c. NPT–IGBT

Figure 2–1. Insulated Gate Bipolar Transistors Cross Sections (not to scale)

It is expensive and difficult to grow defect free epitaxy more than 100 μm thick which is required for IGBTs of 1200 V and above. To circumvent this problem, a Non–Punch–Thru IGBT as shown in Figure 2–1c is utilized. NPT–IGBT's have a thicker N– region which is fabricated using N– Float Zone wafers and is wide enough to prevent high voltage punch–thru. A shallow P+ collector is implanted on the backside of the wafer. Precise control of this P+ implant dose and junction depth results in reduced PNP hole injection compared to the PT–IGBT. This precise hole distribution results in a fast switching NPT–IGBT without having to use the lifetime killing processes common in PT–IGBT's. NPT–IGBT's up to 2500 V are becoming commercially available.

A few final comments comparing these structures follow. The basic IGBT and NPT–IGBT are nearly symetrical blocking devices with $V_{(BR)CES} \sim V_{(BR)ECS}$. However, the reverse leakage I_{ECS} is relatively high (mA range), as the backside P–N junction is sawn thru and un–passivated. The PT–IGBT on the other hand is an asymetric blocking device with $V_{(BR)ECS} << V_{(BR)CES}$ due to the presence of the N+ buffer layer. But like the others, it also has a leaky I_{ECS}. Thus, third quadrant operation of most IGBT's is limited to low reverse voltage.

OFF–STATE CHARACTERISTICS

For normal first quadrant operation, the N–channel IGBT emitter is grounded, the collector is at $+V_{CC}$, and the gate V_{GE} controls I_C. IGBT's are enhancement mode devices, that is, they are normally off for $V_{GE} < V_{th} \sim 5$ V. For $V_{GE} = 0$ V, only a small (nA level) leakage current I_{CES} flow at the output, until V_{CE} reaches the avalanche voltage $V_{(BR)CES}$. The upper P–tub/N– junction supports this forward blocking voltage.

Usually the N– region's thickness and resistivity determine the BV_{CES} breakdown voltage. However, as discussed in the next section, the on–state $V_{CE(off)}$ also increases with N–thickness, so IGBT's are designed for the minimum N–thickness necessary for the $V_{(BR)CES}$ rating. For the 1200 V NPT–IGBT, this results in a wafer thickness of about 0.008 inch. Manufacturing silicon wafers less than 0.008 inches thick is difficult, so most IGBT's rated higher than 1200 V are PT–IGBT's.

Besides the N–region, the device designer must consider several other factors that can affect $V_{(BR)CES}$. These include the MOSFET polysilicon gate width (voltage breakdown between the cells), MOSFET P–tub width, depth, and concentration (curvature and punch–thru effects), and the high voltage planar edge termination and passivation. The termination design and passivation process are critical to the long term reliability of any high voltage semiconductor.

ON–STATE CHARACTERISTICS

When $V_{GE} > V_{th}$, the MOSFET channel is inverted and electrons can flow from the N+ source (IGBT emitter) to the N– drain region, if $V_{CE} > \sim 0.8$ V. This $V_{CE(offset)} \sim 0.8$ V must be exceeded to forward bias the backside P–N junction and permit conduction. The MOSFET current $I_D = I_B$, the base current of the vertical PNP. For large V_{CE}, The I_C of the IGBT saturates due to the transconductance of the MOSFET (G_m) and the current gain of the PNP (beta) according to the equation:

$$I_{C(sat)} = G_m \text{ (beta + 1) } (V_{GE} - V_{th})^2$$

Like any MOSFET, G_m is a function of the gate oxide capacitance, electron mobility, and the channel width/length ratio. Being a wide base BJT, the beta of the PNP is strongly dependant on the N– region minority carrier lifetime, the N+ buffer layer profile (if a PT–IGBT), and the backside P+ doping profile (which internally is the emitter of the PNP). Carrier lifetime is customarily reduced during manufacturing to improve the switching speed of the IGBT. This lowers the PNP beta, and increase the linear region $V_{CE(on)}$.

For hard switching application, the linear region $V_{CE(on)}$ is a critical parameter for fast IGBT's, as it determines on–state power dissipation, and is a direct trade–off with the switching losses mentioned above. The $V_{CE(on)}$ in the linear region has three components:

$$V_{CE(on)} = V_{CE(offset)} + V_{(N- \text{ region})} + V_{DS(\text{surface MOSFET})}$$

Provided that a good ohmic contact exists to the collector P+, the slope of the $V_{CE(on)}$ linear region is controlled primarily by the latter two terms. The resistance of the N– region is conductivity modulated by the bipolar action (electron and hole conduction) of the IGBT. This increased conductivity results in significantly lower $V_{CE(on)}$ at a given current density compared to the unipolar MOSFET of equal voltage rating. At $I_C = 100$ A/cm^2, (typically 20A in a TO–220 package), a fast IGBT's $V_{CE(on)}$ is roughly one–third the $V_{DS(on)}$ of a MOSFET at $I_D = 100$ A/cm^2.

Such improvement in on–state voltage drop is not without consequence. The excess hole carriers in the N– region must be injected and removed during turn–on and turn–off, respectively. Thus the IGBT has slower switching capabilty than the MOSFET, as discussed in the next section. The IGBT switching speed/$V_{CE(on)}$ trade–off can be tailored for the operating frequency to minimize total system dissipation. For PT–IGBT's this is usually done by adjusting the final carrier lifetime. For NPT–IGBT's, the backside P+ profile is adjusted to control the excess hole distribution, so that carrier lifetime killing is usually not required. Using these methods, switching fall times of 100 to 300 nsec can be achieved.

Lastly, the third term (V_{DS}), like G_m, is primarily determined by the packing density of the MOSFET cells. A high channel width/length ratio reduces total channel resistance. Also the drain region under the gate is not highly conductivity modulated, so that the polysilicon gate width must be optimized for $V_{CE(on)}$ as well as $V_{(BR)CES}$.

SWITCHING CHARACTERISTICS

IGBT's are often used in PWM inverters with free–wheeling diodes commutating the load current between the power switches. The turn–on switching loss (E_{on}) is dominated by the t_{fv} fall time of the V_{CE} waveform, which exponentially falls to the on–state $V_{CE(on)}$. The t_{fv} exponential time constant is proportional to the minority carrier lifetime and beta of the PNP. The lifetime can be reduced by heavy metal doping or by high energy particle bombardment creating recombination centers in the silicon lattice. The PNP beta can be reduced by increasing the N+ buffer concentration (PT–IGBT) or decreasing the P+ backside effective emitter doping (NPT–IGBT). Use of both lifetime killing and beta reduction, or other novel recombination structures now in development, are expected to push IGBT fall times to the 50 nsec range.

The turn–off switching loss (E_{off}) is dominated similarly by the IGBT's t_{fi} current fall time, which is also proportional to the carrier lifetime and PNP beta. As lifetime and beta are reduced to improve switching losses, the on–state $V_{CE(on)}$ increases due to the reduced conductivity of the N–region. As mentioned before, the device designer must optimize the IGBT's speed / $V_{CE(on)}$ trade–off for the operating frequency of the application. During switching, or during fault conditions, high I_C and V_{CE} are present simultaneously, which leads to the next topic — SOA.

SAFE OPERATING AREA

The Safe Operating Area (SOA) is defined as the loci of points where the load line (V_{CE} and I_C) may safely traverse on the output characteristics of a device at a specified junction temperature and pulse width. BJT's specify two types of SOA: Forward Biased (FBSOA) and Reverse Biased (RBSOA). Since the IGBT base region is floating and cannot be reversed biased, and since the PNP beta is normally so low that PNP $BV_{CEO} \sim BV_{CES}$, the IGBT's FBSOA and RBSOA are similar, although RBSOA is slightly less as explained below.

IGBT SOA capability is a function of many device design parameters, including lifetime, beta, P–tub doping profile, and MOSFET cell geometry. SOA failures can occur via two distinct mechanisms. The first mechanism is a current induced failure, due to excessive hole carriers in the P–tub region, which internally bias on the parasitic NPN, causing latch–up of the parasitic four layer NPNP thyristor. FBSOA is normally a current induced failure. The second mechanism is an electric field induced failure, due to the excessive charge distribution narrowing the depletion region in the N–, which causes avalanche injection and voltage collapse. During RBSOA, the electron (MOSFET) current turns off first, leaving an excess of holes in the N– region. These holes add to the donor charge, effectively reducing the N– resistivity and breakdown voltage. RBSOA is normally an electric field induced failure. Both FBSOA and RBSOA are affected by T_J, which must be keep below the 150°C rating.

A third SOA rating for IGBT's is Short Circuit (SCSOA). During fault conditions such as a shorted load, the IGBT must survive until the protection circuitry detects the fault and shuts down the system. The device must be designed to survive three modes of SCSOA; turning on into the short (mode A), surviving the high I_C, V_{CE} conduction period (mode B), and then turning off safely (mode C).

The failure mechanism in each mode is as follows:

Failure Mode A is FBSOA latch–up induced.
Failure Mode B is simply power dissipation limited.
Failure Mode C is RBSOA avalanche induced.

The standard specification for SCSOA is surviving for 10 μsec at a starting T_J = 125°C, non–repetitively (since T_J will exceed 150°C). Special IGBT cell design featuring hole–bypass or ballast structures are necessary to survive these severe SCSOA conditions.

The fourth and final SOA condition is Unclamped Inductive Switching. IGBT's are much weaker in UIS than power MOSFETs, due to the hole current present in the IGBT. Because of this, IGBT's are usually clamped well below $V_{(BR)CES}$, but large circuit dv/dt can cause momentary spikes and UIS failure. One solution to this problem is to add series R_g to the gate drive circuit, limiting the dv/dt. "Smart" IGBT's are also becoming commercially available with current limiting and temperature sensing, providing SOA protection on chip.

TEMPERATURE CHARACTERISTICS

IGBT's with a T_J maximum rating of 150°C are typically operated with an average T_J of 75 to 125°C. Therefore the temperature dependance of the on–state and switching characteristics are of primary concern in system design. For this discussion, it is assumed that the device designer has optimized the IGBT for safe operation up to 150°C within the SOA ratings. It remains to describe the effect of temperature on $V_{CE(on)}$, E_{on}, and E_{off}.

As discussed before, the $V_{CE(on)}$ is composed of the $V_{CE(offset)}$, the V(N– region), and the $V_{DS(MOSFET)}$. These three components are affected by several semiconductor parameters that are temperature dependent.

PARAMETER TEMP EFFECT (75 to 125°C)

intrinsic carrier concentration	increases
minority carrier lifetime	increases
carrier mobility	decreases

$V_{CE(OFFSET)}$ decreases as the intrinsic carrier concentration increases. V(N– region) varies in a complex way, because the lifetime increase lowers V(N–), while the mobility decrease with raise V(N–). For PT–IGBT's with lifetime killing, the lifetime effect dominates and V(N–) decreases with T_J. For NPT–IGBT's without lifetime killing, the mobility effect dominates and V(N–) increases with T_J. $V_{DS(MOSFET)}$ also varies in a complex way as V_{th} is also temperature dependent. For most applications V_{GE} >> V_{th} (high I_C), so then V_{DS} is dominated by the mobility decrease, and V_{DS} increases with T_J. The combined temperature effects of these three components is as follows. The $V_{CE(on)}$ of PT–IGBT's has a slightly negative temperature coefficient. The $V_{CE(on)}$ of NPT–IGBT's has a slightly positive temperature coefficient. This makes the NPT–IGBT the better choice when paralleling IGBT's, as their positive temperature coefficient improves current sharing.

Both E_{on} and E_{off} increase with temperature, as the lifetime increase causes the IGBT fall time to increase, due to both slower carrier recombination and higher PNP beta. The NPT–IGBT fall time has a higher TC than the PT–IGBT, as the beta increase cause excess carriers which cannot easily recombine in the higher lifetime NPT–IGBT's.

CONCLUSION

The IGBT is becoming the power switch of choice in medium power applications. It's combination of speed, on–voltage, wide SOA, ease of drive, and relatively small temperature coefficients give the IGBT significant advantages over MOSFET's and BJT's.

Section 3
IGBT Gate Drive Considerations

INTRODUCTION

Devices such as BJTs and thyristors require complicated and very inefficient methods of driving the devices due to their low gain and minority carrier device characteristics. In addition, SCRs become difficult to control due to loss of gate control during turn–off. But it is well known that MOSFETs have the simplest gate drive requirements of all the power devices mentioned. The device can be driven with low power, voltage pulses of required polarity. This simplifies the circuit design, and the switching characteristics can be accurately controlled if all of the circuit parameters are well known.

Because IGBTs are much like fast MOSFETs during the switching transitions, and these devices undergo high voltage and high current transitions, its switching characteristics must be understood by the design engineers in order to avoid some of the problems associated with high voltage and high current transitions. In order to give design engineers a thorough overview of the device characteristics, this section reviews some of the switching characteristics within the clamped inductive load circuit. It is shown that the gate drive circuit, circuit layout, and external components play a vital part in controlling the device switching under clamped inductive load. By understanding the device characteristics and the problems associated with rapid di/dt and dv/dt, the designer can avoid some of the common problems.

This paper covers some of the fundamental switching characteristics, and shows how critical the gate drive circuit is in determining the switching characteristics of the IGBTs. Some of the problems associated with rapid di/dt and dv/dt are discussed, and suggestions are presented in order to overcome these problems.

The parameters that aggravate the problems associated with high di/dt and dv/dt have been shown to be DC bus inductance, common emitter inductance (common to gate drive circuitry), large gate return loop area, the series collector inductance, and the antiparallel diode of the clamped inductive load. All of these parameters contribute significantly to the durability and longevity of the devices, and can affect overall system efficiency.

TURN–ON

Because the IGBT is a MOS–gated device, the turn–on switching performance is dominated by the MOS structure of the device. Figure 3–1 shows the clamped inductive load circuit used to analyze the switching characteristics of the IGBT. It is assumed that the inductor initially has a constant steady state current flowing through it, freewheeling through the diode. The inductance Ls is the series parasitic inductance due to the power trace and any wiring between the IGBT's collector and DC bus. The inductance Le is the common emitter inductance seen by both the power return and the gate return.

Ideal switching waveforms describing the clamped inductive load circuit are shown in Figure 3–2. During the time period t0, the gate current charges the constant input capacitance (C_{ies}) with a constant slope, and as is the case with the MOSFET, nothing happens until the gate–source voltage is raised to the threshold voltage V_{th} of the device. During t1, the collector current is redirected from the diode into the device and increases to its steady state value. The current slope is dependent on gate voltage rise time and device forward transconductance. The following expression can be used to express the current slope:

$$\frac{dI_C}{dt} = gm\,\frac{dV_{GE}}{dt}. \qquad (1)$$

The time rate of change in gate–emitter voltage during t1 period is given by:

$$\frac{dV_{GE}}{dt} = \frac{(V_{GG} - V_{plateau})}{R_G \cdot C_{ies}}, \qquad (2)$$

If we substitute equation 4 into equation 1, the rate of change of collector current is expressed as:

$$\frac{dI_C}{dt} = gm\,\frac{(V_{GG} - V_{plateau})}{R_G \cdot C_{ies}}. \qquad (3)$$

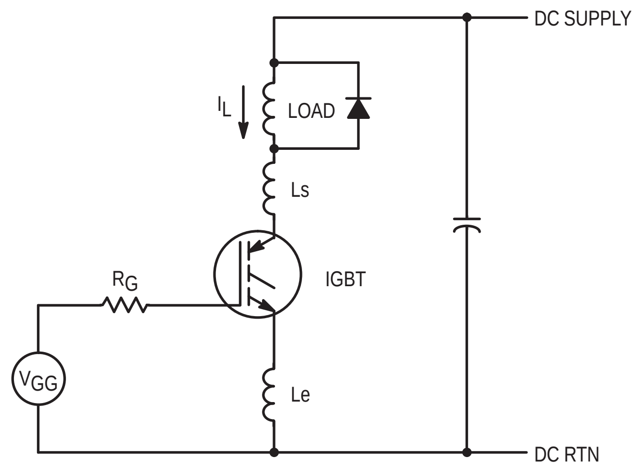


Figure 3–1. Clamped Inductive Load

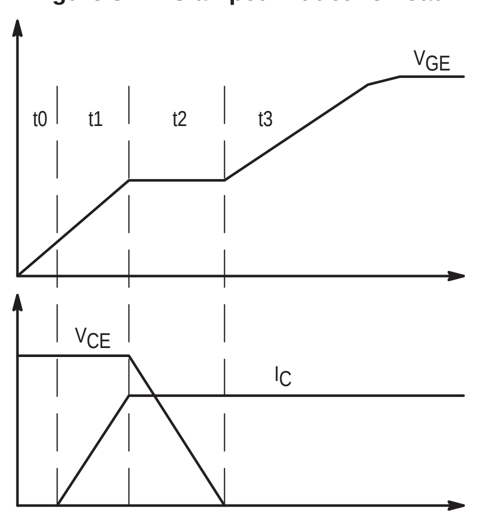


Figure 3–2. Idealized Turn–on Switching of IGBT

During the plateau region t2, the gate–emitter voltage has reached the value which will support the steady state collector current, and the collector–emitter voltage starts to decrease. During this region, gate drive current is discharging the voltage–dependent reverse transfer capacitance at a constant gate current that can be expressed as:

$$ig = \frac{(V_{GG} - V_{plateau})}{R_G} = C_{res} \frac{dV_{CG}}{dt}. \quad (4)$$

where, $$V_{plateau} = V_{th} + \frac{I_C}{gm}, \quad (5)$$

and gm is the forward transconductance of the device at the given steady state collector current I_C and can be obtained using the transfer curve provided by the data sheets. Transconductance is determined by steady state collector current divided by the intercepting gate voltage (I_C/V_{GE}, see Figure 3–3). It should be noted here that the above analysis ignores the change in bipolar current gain as base charge is supplied.

The parameter for input capacitance C_{ies} can be obtained using the capacitance curve provided by the device vendors. Figure 3–4 is a sample curve indicating the capacitance values for input, output, and reverse transfer capacitance C_{res}. A better method of obtaining the capacitance would be to use the gate charge transfer curve. By using the amount of charge needed to turn the device on at a certain operating point, more accurate assessment of gate drive current can be determined. A sample of a gate charge curve for an IGBT is shown in Figure 3–5.

All of the above expressions are presented to show the relationship between the series gate resistance and its effect on the rise time of the device current. Using these equations, the designer can control the current and voltage slope during turn–on. During region t3 the dynamic switching is completed, and a further increase in gate–emitter voltage has no effect on the dynamic characteristics. But, as we will discuss later, the final gate–emitter voltage determines how much turn–on loss is expended by the circuit and determines the magnitude and duration of short circuit current handled by the device.

Turn–On Switching Considerations

In order to reduce the dynamic turn–on loss, the switching time must be very short. This requires that the gate drive be a low impedance type, and be able to provide a large narrow pulse of current to charge the input capacitance which includes the feedback capacitance and gate–emitter capacitance. The turn–on switching time is determined by how quickly the input capacitance C_{ies} is charged. However, the fast switching speed will introduce high di/dt (maximum di/dt is a function of load inductance and the gate drive: 1) where initial di/dt = V/L, and once inductance has charged to its maximum load current, 2) the di/dt will be dominated by the gate drive) which will interact with the lead inductance of the emitter. The control of turn–on di/dt can be seen by observing equation 5. In this equation it is evident that by changing the gate resistor value, the rate of the rise of the device current can be increased. This large di/dt will induce large enough transient voltage across the common emitter inductance and will reduce the available gate voltage causing linearization of the initial collector current rise because of its gate current limiting while increasing the turn–on loss [4]. In order to overcome this problem, a small gate resistance is placed in series with the gate of the device, but remember that the inductance seen by the gate must be minimized. Placing the components as near as possible to the gate–emitter terminals, along with good circuit layout, will reduce much of the unwanted inductance. Also, the gate–emitter current loop must be short. It is good practice to use twisted wire or parallel power paths. Overlapping the power and return paths of the gate drive has the advantage of nullifying magnetic field induced by power trace with the magnetic field induced by the return trace and the effective loop inductance is minimized.

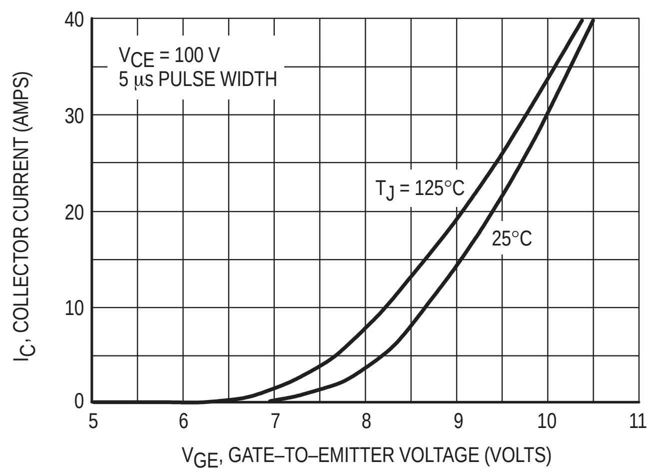


Figure 3–3. Gate–Emitter Voltage Due to Temperature Variation

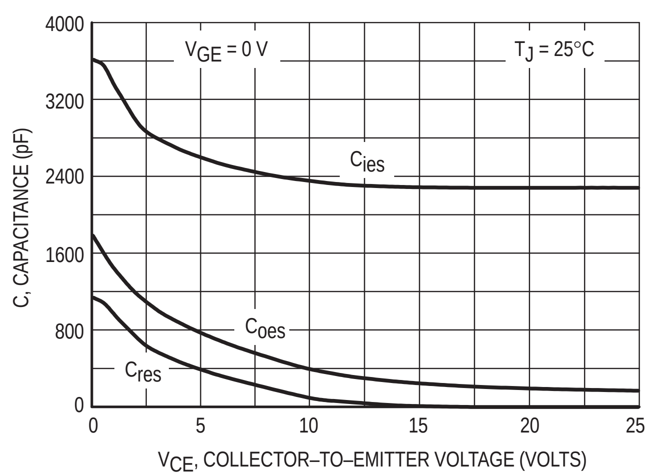


Figure 3–4. IGBT Capacitance Curves

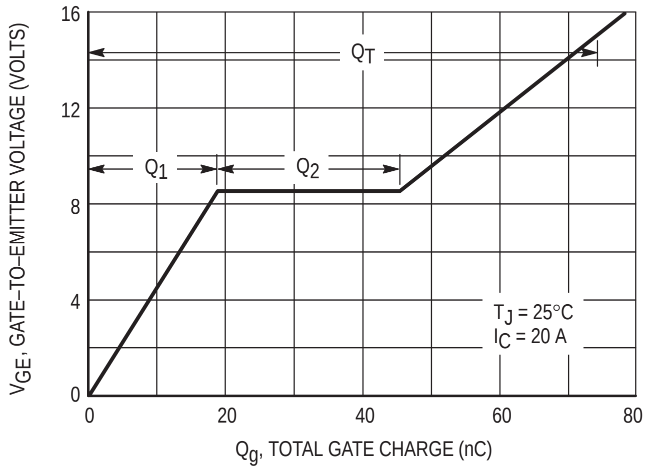


Figure 3–5. Gate Charge Transfer Curve

Rapid di/dt not only limits the available gate voltage, but causes the bus voltage to dip, or decrease due to Ls(di/dt), where Ls is the stray inductance of the power DC bus. During turn–off, the rapid di/dt will cause a large positive voltage to be seen by the device which can exceed the rating of the device. Therefore, it is important to reduce di/dt during turn–on and turn–off duration. A local bypass for the DC bus should be provided as near as possible to the device with a high current, low ESR capacitor. Without these precautions the IGBT may encounter avalanche breakdown due to di/dt induced transient during the turn–off time.

Effect of the Freewheeling Diode

Just as during turn–off, a surge can occur during the recovery of the freewheeling diode. For high di/dt, the reverse recovery of the diode can become very snappy. Because of the stray inductance within the circuit and the device leads, this large di/dt will cause a large dv/dt once the diode is recovered. The high di/dt caused by the snappy recovery of the diode can cause large unwanted voltage transients. Therefore, proper choice of the freewheeling diode is absolutely critical in the performance of the device. A snappy recovery can be controlled or eliminated by increasing the gate resistance R_G, but this will increase the turn–on time, and the efficiency of the circuit will suffer. Therefore, an ultrafast diode with a soft recovery must be chosen. Otherwise a snubber must be used to control the snappy recovery of the diode.

TURN–OFF

The turn–off of the IGBT is initiated by removing the voltage across the gate–emitter just as for MOSFETs. Figure 6 shows idealized turn–off waveforms for switched inductive load. The first part of the turn–off process is the delay time ($t_{d(off)}$), which is the effect of the time required for the gate drive to pull V_{GE} from its full value to the level at which the collector voltage begins to increase. Nothing is observed while gate voltage is decreased, until the gate voltage reaches the value required to keep the collector steady state current to flow. During t5, the collector voltage rises, and its rate of rise can be controlled by the gate resistance R_G:

$$\frac{dV_{CE}}{dt} = \frac{V_{plateau}}{C_{res} \cdot R_G}. \qquad (6)$$

Equation 6 assumes that the gate resistance is large enough that the output capacitance is not the limiting factor.

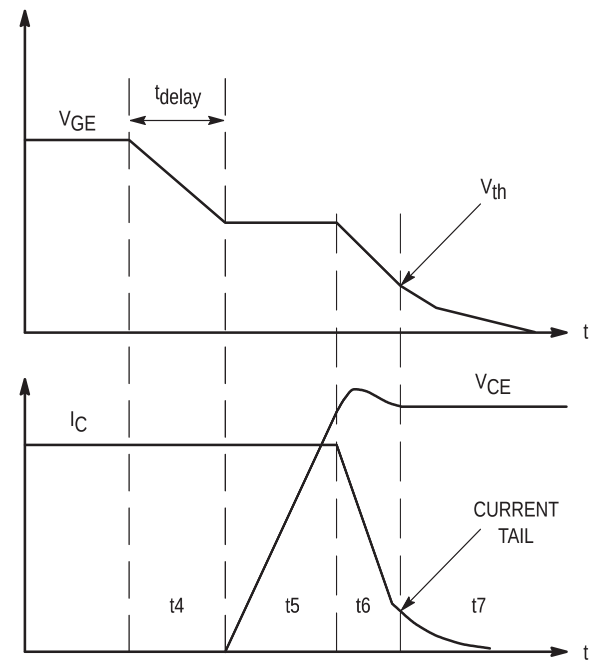


Figure 3–6. Idealized Turn–off Switching for IGBT

At t6, the collector voltage has reached the bus voltage V_{DD}, the freewheeling diode starts to conduct, and collector current starts to decay. Because of the high di/dt, the collector voltage rises beyond the bus voltage due to L(di/dt) overshoot. The region, t6, is the initial fall time, and this is the time required for the gate drive circuit to remove the charge that flows into the gate from the gate–to–drain capacitance as V_{DS} increases during turn–off. This period is greatly influenced by the gate drive design and its drive impedance, R_G. For small gate resistance, period t6 is determined by the clamp inductance. This period is defined as the time it takes for Ic to drop from 90% of its full current down to approximately the 10% level (this will include the tail). This period is greatly influenced by the gate drive design and its drive impedance, R_G, and the effect of R_G on the collector current fall time is expressed as:

$$\frac{dI_C}{dt} = gm \frac{V_{plateau}}{R_G \cdot C_{ies}}. \qquad (7)$$

The time period t7 shows an abrupt decrease in current slope. This current slope is due to the recombination of the minority carriers in the wide base region of the integral BJT. This recombination process produces what is frequently termed as the “current tail.” This current tail limits the operation frequency of the IGBTs, and the size and length of this current tail is determined by the device design and process technology.

Turn–Off Considerations

Just as with the MOSFETs a negative bias can be applied to the gate in order to speed up the turn–off. This does not mean that the recombination of minority carriers in the wide base region will be increased, but it helps to speed up the turn–off of the MOSFET portion, and thus turns off the base of the integral PNP bipolar transistor quicker. The rapid turn–off will cause a high dv/dt.

The problem associated with high dv/dt is that it can introduce current through the capacitance to the base of the internal parasitic NPN bipolar transistor (only in a bad device), thereby causing the device to latch on. Once the device is latched on, the gate–control is lost and the device cannot be turned off without removing the power to the collector terminal of the device (see Figure 3–2). A small gate–emitter resistance can be added to the terminals to bypass the dv/dt problem. Also a series resistor should be used when negative gate bias is applied during the turn–off process. The negative bias should be left on while the device is turned off. This will protect the device from the false turn–on due to the dv/dt problem. Optimum values of the resistors can be found by trying different values of the resistor in the circuit to be used or by simulation.

Effect of the Current Tail

The t7 interval, as discussed earlier, is a result of minority carrier recombination in the bipolar PNP structure. IGBT is a minority carrier device during the forward conduction, and as such the highly resistive region (n– epitaxial layer) is highly injected with minority carriers. This minority carriers must be removed before the device stops conducting completely. The turn–off speed of the device is therefore determined by the integral bipolar open base turn–off. This tailing effect is the direct result of the internal base of the PNP structure which cannot be accessed by the external means; and as a result, we cannot discharge the excess minority carriers by reverse biasing the gate. The controlled rate at which the minority carriers recombine is a function of device design and process technology. This current tail contributes to limit operational frequency and introduces large switching energy to be dissipated by the device. How fast the minority carriers recombine determines how long the current tail is and the turn–off speed of the device.

GATE DRIVE REQUIREMENTS

From the previous discussion of switching characteristics of the IGBT, the following have arisen as the important factors that need to be considered when designing the gate drive:

1. Reduce the gate–emitter current loop by separating the power return and gate return
2. Use a twisted wire if possible and overlap the power traces of gate drive if PCB is used
3. Make the gate drive connection as short as possible to the device being used so as to reduce any parasitics
4. Use a series gate resistor, R_G to limit di/dt and dv/dt
5. Use a negative bias if possible to reduce any dv/dt problems

CONCLUSION

IGBTs are excellent candidates for high power applications. However, when switching high voltage and high current, care must be taken in the beginning stage of the design to ensure that circuit layout will support the high di/dt and dv/dt. Some equations have been provided so that by using appropriate gate resistors, di/dt and dv/dt can be controlled.

It was observed that the gate drive is a vital element in obtaining the maximum performance of the device. Through the correct use of gate drive the designer can overcome some of the common problems associated with high voltage high current switching: 1) accurately control di/dt and dV_{CE}/dt problems, and 2) avoid latching of the parasitic thyristor. Using a negative bias at the gate reduces the chance of false turn–on and latching of the device. Not only was the gate drive vital in determining the switching loss, but the freewheeling diode in a clamped inductive load introduces turn–on switching losses. It is of utmost importance that an ultrafast diode with soft recovery type be chosen.

Layout of the circuit was vital in overcoming some of the switching problems. The ground loop of the gate drive must be separated from the power return so that the common emitter inductance does not interrupt the turn–on process. The twisted wires or parallel power tracts should be used for the gate drive. In order to reduce any unwanted supply bus inductance, it was suggested that a bypass capacitor with low inductance and low ESR be connected right at the device level, or just as in gate drive, the supply bus tracks can be paralleled. By following some of these recommendations, many of the common problems associated with high current and high voltage switching can be dramatically reduced.

Section 4
Effect of Gate–Emitter Voltage on Turn–On Loss and Short Circuit Capability

INTRODUCTION

Unlike the MOSFETs and BJTs, the magnitude of the gate–emitter supply voltage of an IGBT has a significant impact on the performance of the device. The magnitude of the gate voltage impacts the turn–on loss and short circuit survival capability of the devices. In this section some of the impacts of the gate–emitter voltage on the device performance will be examined.

TURN–ON LOSS

As mentioned before, the turn–on characteristics of IGBTs are similar to those of a MOSFET. In MOSFETs, once the gate–source voltage has reached the value to support the steady–state drain current, a further increase in V_{GS} has no significant role in the circuit, but it does greatly affect the switching speed of the device. The magnitude of the gate–emitter voltage significantly affects the magnitude of the turn–on loss during the transition.

Figure 4–1 depicts measured data that shows the relationship between gate–emitter voltage and turn–on loss with a constant R_G, 20 ohms. As shown by the curves, larger gate–emitter voltage reduces the turn–on loss of the device. This can be explained by the fact that for a given gate resistor, the gate current available increases with the increase in the gate voltage. Therefore, the input capacitance of the device is charged at a faster rate which can account for less loss. The longer it takes the device to turn on, the more energy is dissipated by the device. For given collector currents, increase in gate–emitter voltage reduces turn–on loss.

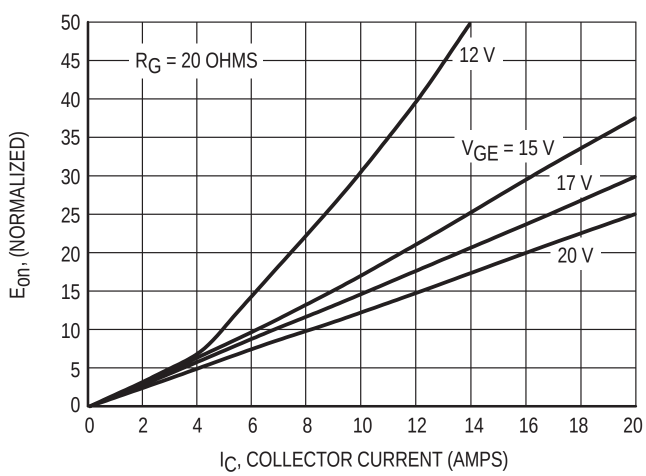


Figure 4–1. Turn–on Loss with Different Gate–Emitter Voltage

SHORT CIRCUIT FAULT OPERATION

A major concern in inverter applications is the ability to survive a short circuit fault condition. During the short circuit fault, the device is exposed to the supply voltage across the device, while the gate potential is at full operating value (see Figure 4–2). Because of the high gain characteristic of the IGBTs, the collector current will rise to some undetermined value limited by the gate–emitter voltage. During this time the device will have a large amount of energy across the device, and if the energy is beyond the capability of the device it will be destroyed due to thermal breakdown. For the bad devices, the large current can cause parasitic NPN bipolar transistor to turn on and cause the device to latch, wherein the gate control will be lost.

One point to note here is that the IGBTs are less sensitive to second breakdown due to hot spot formulation unlike the BJTs. In understanding this, it is clear that the device should be able to survive a short circuit condition if the energy delivered to the device is maintained below some value that is tolerable to the device.

There are many different ways to protect the device from the short circuit condition for some duration. Remember that the device does not turn off when a short circuit occurs, but rather limits the amount of the energy dissipated by the device by limiting the collector current. This provides enough time for the external protection circuits to be activated. Therefore it is of utmost importance that the device be able to survive a short circuit fault condition. The most effective way to provide the short circuit survivability would be to inherently build current sensing capability into the device, but as of now, no manufacturer has any device which has built–in current sense for short circuit detection. IGBTs produced by Motorola are capable of short circuit survivability of 10 µs minimum.

Another method of increasing the short circuit survivability is to decrease the gate voltage when the short circuit across the device is observed. Figure 4–3 data shows the relationship between the gate voltage, short circuit current, and the short circuit survival time period. As shown in Figure 4–3, it is clear that the smaller gate voltage limits the current at lower value and increases the short circuit time duration.

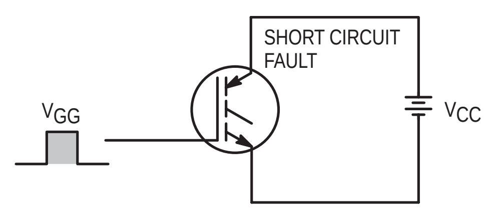


Figure 4–2. Equivalent Short Circuit Condition

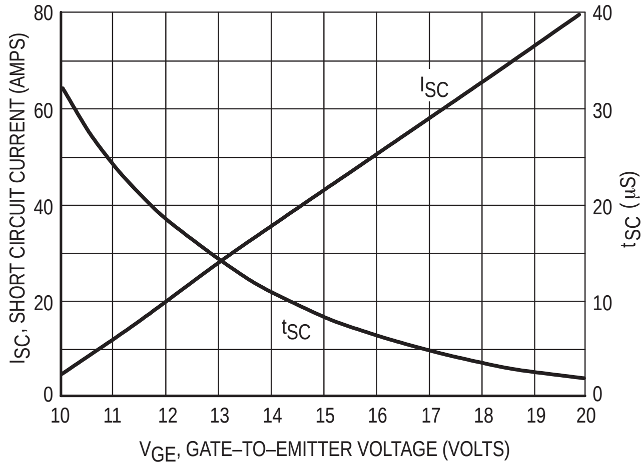


Figure 4–3. Short Circuit Response of IGBT

SUMMARY

IGBTs are high current and high voltage devices. Because of their use in high power applications, it is important that some of the key behavior of the device is understood by the user in order minimize switching losses and to prolong their lifetime.

In most cases, the turn–on loss of the device in a clamped inductive load is dependent on the performance of the free–wheeling diode, and is a function of the diode's reverse recovery time. But as we have discussed, the magnitude of the gate–emitter voltage can be optimized in order to reduce the turn–on loss of the device. But on the other hand, the designer needs to understand that the high gate–emitter voltage reduces the short circuit survivability of the device.

Using these two relationships, the designer can choose the best voltage value which will meet their design requirements.

Section 5
Forward Conduction and Turn–Off Behavior of IGBTs at High Temperature and Its Contributions to Static and Dynamic Turn–Off Loss

INTRODUCTION

IGBTs have been introduced to overcome the high on–state voltage of MOSFETs and slow switching frequency of BJTs. But because IGBTs possess dual device characteristics, their behavior is not easily understood. In high current applications, the on–state voltage becomes a major issue, and, in other cases switching losses may be the major concern. In this section the on–state voltage characteristics and dynamic turn–off will be discussed. It is shown that the unique characteristics of the IGBTs allow the designer to operate the device to obtain low conduction loss. But also shown are that dynamic turn–off losses must be taken into consideration with variation in temperature.

During the turn–off at high temperatures close attention must be given to: 1) current tail variation, 2) initial current height of the anode current, 3) reduced rate of rise of anode voltage, 4) and increased carrier lifetime. All of these add to the turn–off energy loss and can damage the device if care is not taken.

FORWARD CONDUCTION

Because IGBTs behave like MOSFETs in switching transitions, it can be misunderstood that the device always possesses a positive temperature coefficient (that is, the on–voltage increases at higher temperature). This perception is partially correct. As we shall see the device actually possesses negative temperature coefficient at low current levels.

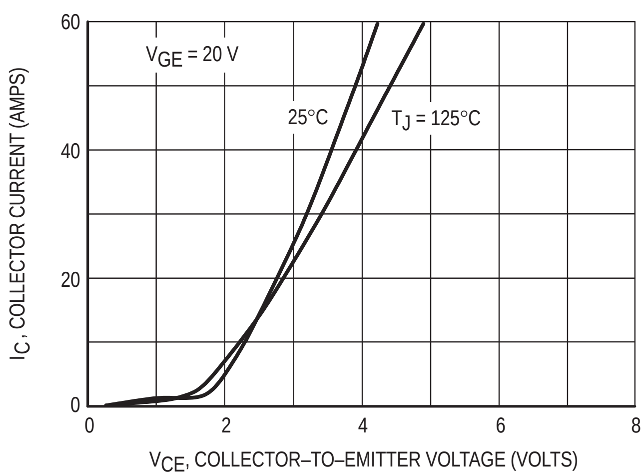


Figure 5–1. IGBT Output Characteristics

IGBTs possess aspects of both MOSFET and BJT characteristics. Figure 5–1 shows the temperature dependence of collector current versus collector–emitter voltage. For low current levels, the device possesses a negative temperature coefficient, and as a result the saturation voltage is decreased with increase in temperature. At some current level, the two curves cross each other and at this crossover point V_{CE} becomes temperature independent. At higher current levels, the device possesses a positive temperature coefficient characteristic and its saturation voltage increases with increase in temperature.

At high temperature, there are a few important things that are happening which contribute to the device on–voltage. It was discussed by Hefner [5] that: 1) the base resistance increases with temperature due to decrease in the mobility of the carriers, 2) emitter–base junction diffusion voltage decreases due to increase in base intrinsic carrier concentration, 3) the drain–source voltage increases slightly with temperature because the decrease in MOSFET transconductance dominates the decreasing threshold voltage for the high gate voltage bias condition.

The on–voltage of the device decreases with temperature at lower current levels because the base resistance and channel resistance is small compared to the change in emitter–base junction diffusion voltage. The BJT characteristics of the device are dominating at this point. But for higher current levels, the base resistance and channel resistance start to become significant enough and dominate the on–voltage of the device, and as a result, introduce the positive temperature coefficient which is a MOSFET effect of the device.

If the operating current is within the negative temperature coefficient region, one can be mistaken in thinking that operating the device at a higher temperature will be much more efficient. This may be true if other factors such as conduction current, thermal environment, circuit layout, and other operating parameters have been considered. But as we will later see, dynamic turn–off must be considered at high temperature operation.

TURN–OFF

Unlike the relatively temperature insensitive forward voltage drop of the device, the turn–off energy loss is increased with temperature. Figure 5–2 shows the dramatic increase in turn–off loss at high temperature. This increase in energy loss is contributed largely by the increase in the current tail. The current tail is a function of the base minority carrier lifetime and is increased with rise in temperature. Not only is current tail length increased, but the storage time, dV_C/dt, and initial anode current tail height is also increased. These effects all contribute to higher turn–off energy loss, and attention should be given by the designers using the IGBTs. By understanding how the device behaves with the temperature at turn–off, the design engineer can better assess the best operating parameters for a given application.

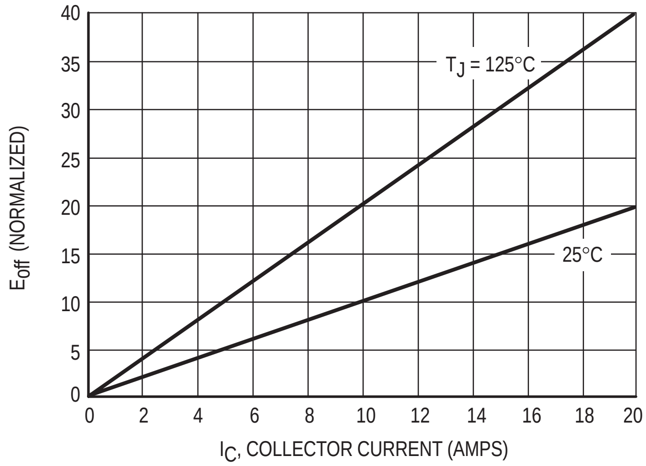


Figure 5–2. Turn–off Energy Loss at Different Temperatures

Current Tail

With an increase in temperature, the mobility of the minority carriers in the wide base is reduced, and the lifetime is increased which prolongs the current tail during the turn–off of the transistor. The increase in the current tail can account for almost 60% of the turn–off loss. Not only is more energy dissipated by the device, this will reduce the operating frequency of the device. Figure 5–3 depicts the anode current during the turn–off. The initial current height is denoted by $I_T(0+)$ and is the time at which the current tail starts to decay exponentially. For devices which do not have the buffer layer, the initial height of current tail remains relatively constant and with temperature only current tail length is increased. But for devices with the buffer layer, this initial tail height increases with the temperature. Both the increased height and length of tail with temperature means that the device will turn off slower.

It was discussed that the $I_T(0+)$ is proportional to the base charge Q, and diffusivity of the device [6]:

$$I_T\ (0+) \propto Q \cdot D \tag{1}$$

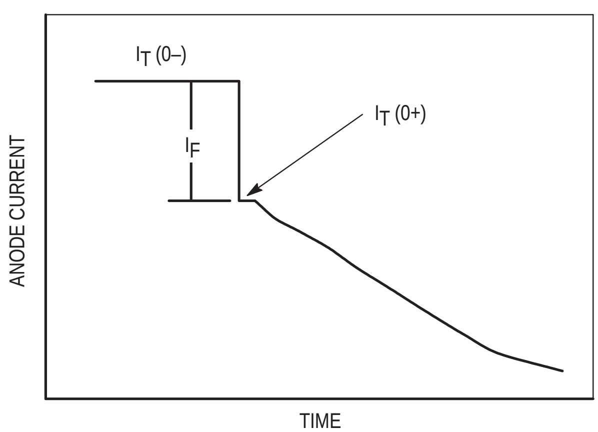


Figure 5–3. Anode Current During Turn–off

For nonbuffered devices, the increase in the base charge with temperature is negated by the corresponding decrease in the diffusivity. But in the buffered devices, the increased charge due to the temperature is greater than the decrease in the diffusivity of the device, and as a result, the initial current magnitude varies with temperature. The variation in initial current height and in current tail length is the major contributor to the turn–off energy loss.

Figures 5–4a and 5–4b show turn–off waveforms at 25°C and 120°C respectively. The data shows that the initial current height and current tail is increased significantly at higher temperatures. This increase in the current tail length and initial current height contributes to a larger turn–off energy loss.

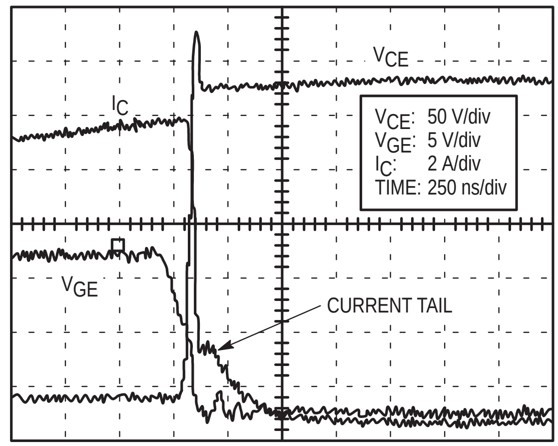


Figure 5–4a. Turn–off Waveforms at 25°C

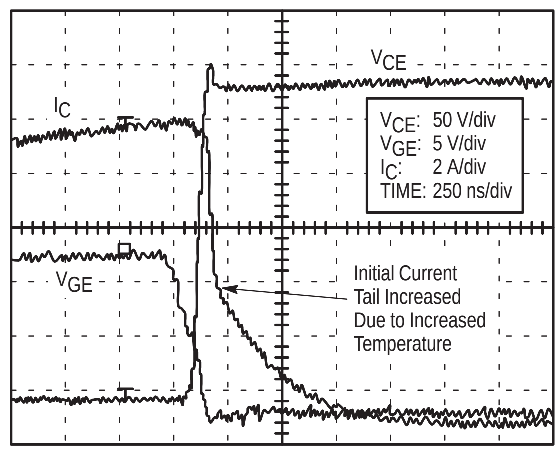


Figure 5–4b. Turn–off Waveforms at 120°C

Collector Voltage Transitions

In the previous paragraphs it has been discussed how the increase in device temperature decreases the mobility and increases the lifetime of a device. This increase in lifetime also increases the current tail length and its associated initial current height. But as we shall see, the rate of rise of the anode voltage is also affected by the temperature due to increase in the lifetime, and adds to total turn–off loss.

Figure 5–5 shows an equivalent schematic of IGBT showing all of the internal circuits associated with the device. During the turn–off, the output capacitance is dominated by the collector emitter redistribution capacitance, C_{cer}. This capacitance is orders of magnitude larger than the depletion capacitance and dominates the effective output capacitance of the IGBT during turn–off. Because this capacitance is charge dependent, its value is varied with change in temperature (charge is varied with temperature). At high temperature, the increase in charge increases the effective output capacitance and thus decreases the rate–of–rise of the collector–emitter voltage. The following equation can be expressed as:

$$I_{base} = \frac{Q}{T_{HL}}. \qquad (2)$$

Current I_{base} is a steady state current level, charge Q is charge present in the base, and t_{HL} is the excess carrier lifetime. With increase in temperature, the whole lifetime is increased due to reduction of mobility of carriers within the base region. The increase in the base lifetime means that the charge must increase in order to provide the unchanged collector current. During the voltage transition, the effective output capacitance and rate–of–rise of the anode voltage must be able to supply the steady–state collector current. Since the capacitance is proportional to the amount of charge present, its value is increased accordingly. Larger capacitance then decreases the rate–of–rise of the anode voltage because it takes longer to charge the bigger capacitance. The rate–of–rise of the collector voltage is an inverse function of the capacitance, and the following expression can be used to describe its dependency on charge and capacitance:

$$\frac{dV_C}{dt} \propto \frac{1}{C_{cer}} \propto \frac{1}{Q} \qquad (3)$$

Storage Time

Other side effects of the decrease in the rate–of–rise of the voltage is that it prolongs the storage time. In a clamped inductive load, the collector voltage must reach its full supply voltage value before the collector current starts to decay (see Figure 5–6). The decrease in dV_{CE}/dt causes the collector current to remain at its full steady–state value much longer, and hence increases the turn–off loss.

FURTHER DISCUSSION ON TEMPERATURE EFFECT

Figure 5–6 shows all of the phenomenon that has been discussed previously. The first thing to note is that the initial current tail magnitude has increased dramatically. But also note that the storage time has been increased due to the decrease in dV_{CE}/dt. As shown in Figure 5–6, dV_{CE}/dt is decreased by a factor of two, and is independent of gate voltage after t6 region (it is assumed that there is no significant variation in gate drive performance with variation in temperature). Notice the lack of voltage overshoot due to decrease in the slopes.

Figures 5–7 and 5–8 are measured data showing the effect of temperature variation during the turn–off. All of the phenomenon discussed are apparent during the turn–off transition. One important factor to remember is that the device was operated only at 50% of its rated voltage. If the collector voltage is increased, the turn–off loss encountered can increase much more which will then increase the junction temperature of the device. (See Figure 5–9.) So special care should be given to the turn–off transition if the device is to operate efficiently under temperature variations.

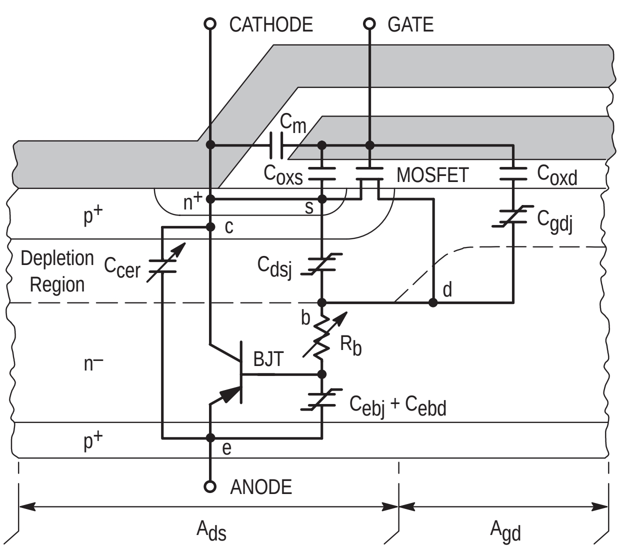


Figure 5–5. IGBT Equivalent Circuit Superimposed on One–half of Symmetric IGBT Cell (Reprinted with permission from NIST)

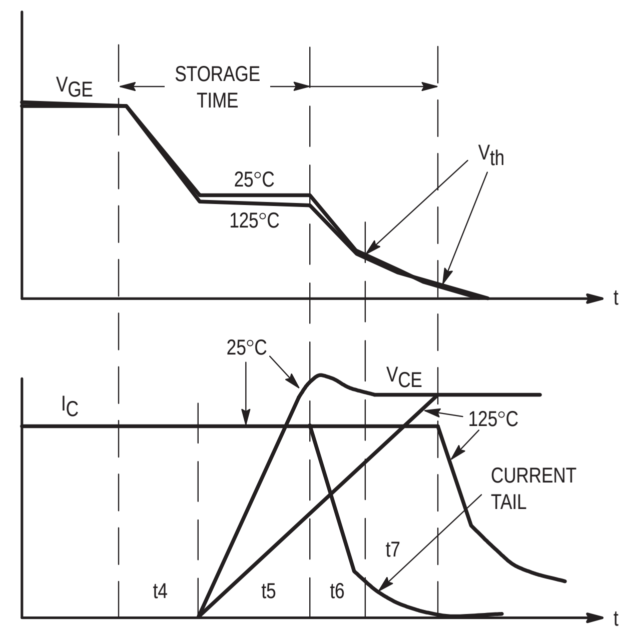


Figure 5–6. Turn–off Behavior of IGBT with Temperature Variations

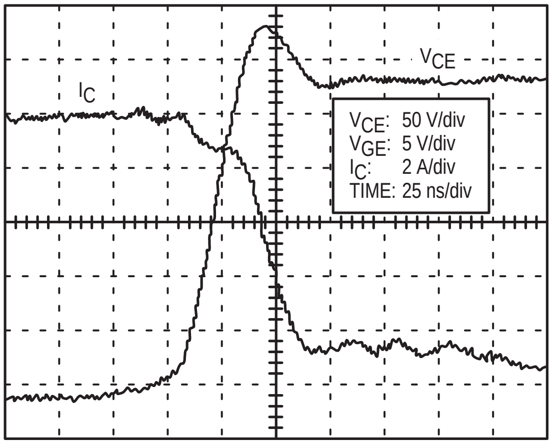


Figure 5–7. Turn–off at 25°C (V_{DD} = 300 Vdc)

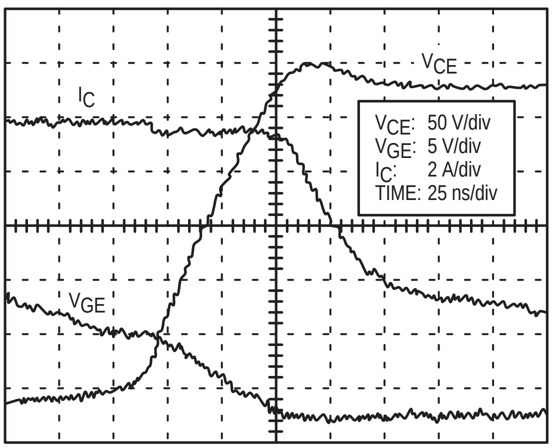


Figure 5–8. Turn–off at 120°C (V_{DD} = 300 Vdc)

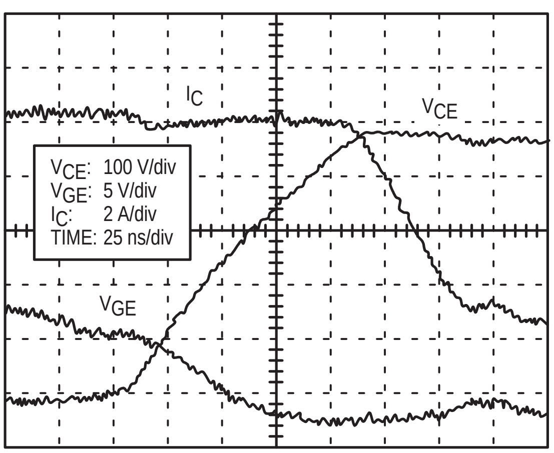


Figure 5–9. Turn–off at 120°C (V_{DD} = 500 Vdc)

CONCLUSION

IGBTs have very unique characteristics which can be utilized to best meet many of the high power switching applications. But unlike BJTs and MOSFETs, it is not straightforward when it comes to designing for temperature variations. One must not only look at the on–state voltage, but one also needs to consider the dynamic behavior of the device with temperature. How well the device temperature is stabilized determines how rugged the device will be. If the environment is such that temperature variation is minimal (and can be guaranteed), the design can be optimized for the on–state voltage because the turn–off energy loss variations will be small. But if the temperature stability is not guaranteed, the designer needs to consider all of the parameters discussed and great care should be given to device junction temperature. The design should be done by derating the part for the worst case condition which the device will confront. If care is not taken, one can be assured of device failure or degraded performance. The following are some of the considerations that should be taken when using IGBTs:

1. Temperature environment of the circuit
2. Device characteristics with temperature variations
3. Increase of storage time
4. Decrease of dV_C/dt
5. Increase in initial current tail height
6. Increase in total current tail length
7. Operating current of the device
8. Operating frequency

Considering these factors will help the design engineers to better utilize all of the benefits of IGBTs.

Section 6
IGBT Paralleling Considerations

INTRODUCTION

Paralleled IGBTs are used extensively in power modules to obtain higher current ratings [3], thermal improvements, and for redundancy. However, the typical process variation of device parameters within a given device type is significant enough to result in uneven static and dynamic current sharing if the paralleled devices are chosen randomly from a given lot of IGBTs of the same type. Design engineers must make sure that the temperature variations do not significantly vary the significant device parameters, and caution must be observed. Aside from the temperature and device parameter variations, it is well known and much has been written about how the circuit layout and its contribution can greatly influence the performance of devices in parallel operation.

In this section the characteristics of IGBTs under parallel operation are shown. The effect of device parameter variations under static and dynamic current sharing are studied, and the effect of temperature and circuit layout are discussed. Then some suggestions are presented on how to overcome the common problems associated with paralleling IGBT devices. It is shown that if the designer considers careful circuit layout, thermal considerations, and pays careful attention to process variations within the given lots, many of the problems associated with the paralleling power IGBT devices can be avoided.

Many of the papers written about parallel operations of IGBTs concern the effect of temperature variations. It is true that temperature is the key role player in the destruction of IGBT devices. But it is unclear as to what or how the temperature is changing the device characteristics. The IGBTs have the dual device (MOSFET and BJT) characteristics, and in order to truly understand the temperature effect on paralleling, it is necessary to understand how the temperature changes the characteristics of each device type. In this way the designer is better informed and will be able to better design for “key” parameters.

PARAMETER VARIATIONS

In order to observe how the dissimilar parameters affect current sharing of the paralleled IGBTs, the parameters lifetime t_{HL}, threshold voltage V_{th}, and transconductance Kp, were varied between two different devices. These parameters were chosen because the normal process variation of these parameters has the most impact on current sharing for parallel operation [7].

The circuit used to simulate and test the parallel operation of IGBTs is shown in Figure 6–1.

The inductors Ls1, Ls2, Le1, and Le2 are the inductances due to lead and power traces. The load resistor RL is used to limit the collector current to a safe level. It is shown that these parasitic components have a significant role in the operation of the IGBTs.

Variations in Lifetime

The effect of lifetime on the IGBT is through the bipolar characteristics of the device. In order to understand how the lifetime variation behaved in parallel operation of IGBTs, two devices with dissimilar lifetimes were observed. Figure 6–2 shows a waveform of collector voltage and collector current of both device types. The difference in lifetime has no effect on turn–on transitions, but the current imbalance during the steady–state region, and turn–off variations are observed. The device with the higher lifetime conducted more current than the device with lower lifetime. Because of this higher lifetime, more charge is stored in the wide base region, and thus decreases the saturation voltage. With its lower $V_{CE(sat)}$, it draws more of the load current. No significant current spike is observed during the turn–off transition, but as expected the device with higher lifetime had a larger current tail because more charge had to be removed.

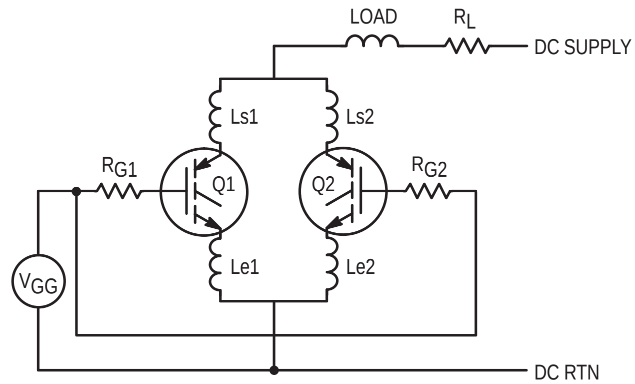


Figure 6–1. Paralleled IGBTs Used in Inductive Load

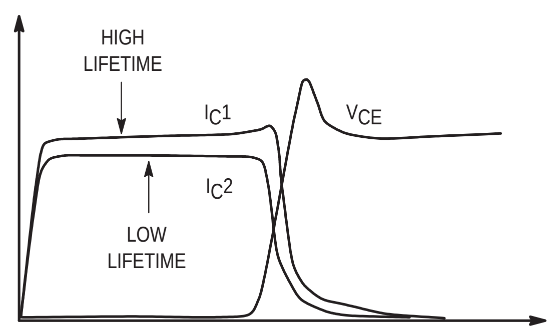


Figure 6–2. Paralleled Operation of IGBTs with Lifetime Variation

Temperature Effect on the Lifetime Variations. With increase in temperature the lifetime increases. Figure 6–2 shows that if the static current sharing is within the tolerable region, there is no problem associated due to lifetime variations. During the turn–off sequence, the length of the current tail of the device with higher lifetime is increased. This increase in current tail will increase the turn–off loss of that device but should not have significant effect on the static current sharing if the parameter variation is minimal. But if the devices have wide variation in the lifetime, the device with the higher lifetime can encounter thermal breakdown (for example, paralleling an ultrafast with a slow IGBT). The thermal effect of the device is overcome by using the same heatsink for both devices and the temperature feedback between the devices will keep the current sharing very constant because the lifetime of both devices will vary together and one will track the other constantly. Because the current tail is the same in a paralleled configuration as for a single device, the destruction of the device due to lifetime variation is the same as for single devices used in a scaled down circuit. If the designer did not consider the temperature effect of the current tail, $V_{CE(on)}$, and the energy loss, the device may fail due to excessive energy dissipated by the device at high temperature. However, in a parallel operation, unless a large quantity of the devices are paralleled for very high current levels, the failure of the device in paralleled operation would be the same as in a single device operation.

Threshold Voltage and Transconductance Variation

Threshold voltage and transconductance are MOSFET characteristics. Two devices with different MOSFET threshold voltages and transconductance were chosen, and the resultant waveform is shown in Figure 6–3. The turn–on delay occurs for the higher threshold voltage device because it takes longer for the gate voltage to charge up the gate–emitter capacitance to its threshold voltage. Not only does the threshold voltage cause the delay, but the lower transconductance will cause delay during the turn–on because the device resistance is higher than the other device until its gate voltage becomes large enough so that the on–state resistance of both devices are primarily determined by the bipolar emitter–base voltages. The static portion of the waveform shows a current imbalance, and the device with the higher transconductance conducts more current because its on–resistance is lower than the other device. At turn–off, a current spike exists for the device with the larger transconductance and smaller threshold voltage. The turn–off current spike in the higher transconductance device occurs because the resistance of the lower transconductance device becomes larger sooner than for the high transconductance device, and the inductor current is transferred to the lower resistance device. The turn–off current spike introduced by variation in transconductance and threshold voltage can be detrimental to the device if its SOA has been exceeded.

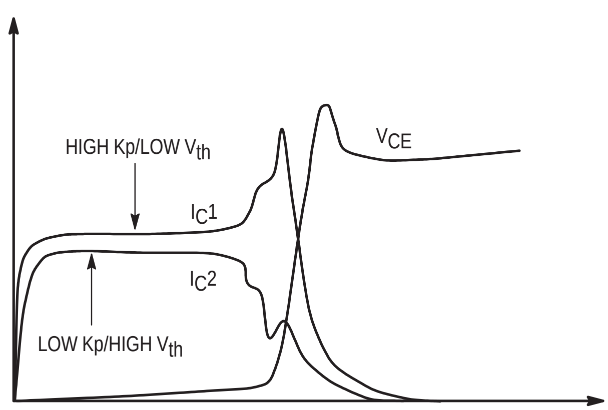


Figure 6–3. Paralleled Operation of IGBTs with Kp and V_{th} Varied

Temperature Dependency of V_{th} and Kp. With an increase in temperature, both of the parameters will be decreased. For a high–gate voltage, the on–state voltage will tend to increase with temperature, but because the IGBT has dual device characteristics, the BJT emitter–base voltage decreases with temperature due to the increase in intrinsic carrier concentration. The decrease in BJT emitter–base voltage will negate the decrease in transconductance, and as a result, the amount of current seen by the device will be changed very little or not at all. But if the current level is high enough, the MOSFET effect will dominate and the device $V_{CE(sat)}$ will increase with temperature. This increase in on–resistance of the device will cause the other device to take more of the current, and thereby always keep the current–sharing well balanced. Unless the parameters are significantly different, static current sharing is well balanced from device to device.

During turn–off, however, the device with higher transconductance will conduct most of the current because the MOSFET channel resistance dominates during switching. If the variation in transconductance is wide enough, one of the devices can be destroyed due to excessive current spike.

Just as for the transconductance, the threshold voltage of the IGBT will decrease with the increase in temperature. Just as variation in transconductance will introduce turn–off current spike, large variation in threshold voltage can cause dynamic current imbalance because one device will turn off faster than the other device. During the static operation, the threshold voltage will have no effect. However, the decrease in transconductance counterbalances the effect of the decrease in threshold voltage, and the current spike is independent of the temperature.

USING COMMON HEATSINK

With common heatsink, the parameter variation in both devices will approximately be equal, and as a result, the dynamic turn–off current imbalance will not be improved significantly if the designer did not pay attention to the V_{th} and Kp. In fact, using a separate heatsink will actually improve the dynamic current sharing for the IGBTs. Static current sharing is greatly improved in IGBTs because the lifetimes of the devices tend to increase proportionally to other devices with temperature. Using a common heatsink will improve the static current sharing, but large dynamic instability can still be introduced if Kp and V_{th} variation is not minimized.

EFFECT OF CIRCUIT LAYOUT

Just as in normal operation of the single device, the circuit layout is very important in the parallel operation of the devices. Large variation in common–emitter inductance has been shown to be the biggest contributor to the cause of dynamic current imbalance of the devices. If one of the device's emitter–ground inductance is large while the other device sees low inductance, a large current spike is observed by the lower inductance device because it turns on much faster than the other. It was discussed earlier that the large emitter inductance introduces large voltage drop and results in clamping of the gate current during the turn–on. So more of the gate current is diverted to the device with lower common–emitter inductance. With the interaction of parasitic capacitors and nonlinear voltage–dependent junction capacitance of the devices, it will oscillate with large common–emitter inductance. This will be sensed by the other device, and they will together oscillate out of phase with each other.

EFFECT OF GATE RESISTANCE

If separate gate resistors are used for each device, it will introduce a variation in delay time (or storage time). The device with longer turn–off time will stay on longer, and the lower storage time device will transfer its current to the other device. This will introduce more power dissipation in one device and introduce thermal instability if separate heat sinks are used.

If careful attention has been given to the circuit layout, and common–emitter inductance has been minimized, using a single–gate resistor for both devices will reduce the turn–off storage time variation because the device with higher storage time will keep the other device conducting to a value which is dependent on the device transconductance.

SUMMARY

Many of the problems associated with paralleling of power devices can be greatly reduced by using IGBTs. It has been shown that the device characteristics of the IGBT device favors parallel operation as opposed to BJTs. Its dual device characteristics can be utilized to give design engineers very satisfactory performance under static and dynamic current sharing of the devices. Problems associated with paralleling IGBTs can be minimized and deterred if careful attention is given to parameter variations, careful circuit layout (minimizing parasitic inductance), and using common heatsinks. Remember that using a common heatsink does not improve the dynamic current imbalance if parameter variations of Kp and V_{th} are large. Static current sharing is increased with the use of common heatsink. Most of the failure of the devices in paralleled operation can be contributed to neglect of device temperature effect and not derating the parts as they should have.

In summary, the following criteria should be met for paralleling IGBTs:

1. Minimize the spread of lifetime, Kp, and V_{th} between the devices to be paralleled
2. Minimize the common–emitter inductance difference
3. Take all the precautions just as if the devices were operating as single devices
4. Use single gate resistors to drive the gates to reduce the storage time variations
5. Use a common heatsink for all of the devices
6. Understand which characteristics will dominate the parallel operation (BJT or MOSFET)
7. Calculate the junction temperature using worst case numbers

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Section 7
Motorola's Motor Control IGBTs and Free–Wheel Diodes

Abstract – Motorola's IGBTs and free–wheel diodes offer significant improvement in operating efficiency and short circuit ruggedness for motor control applications. The E–series IGBTs are based on a technology platform which has achieved superior optimization between conduction and switching losses while simultaneously improving short circuit rating. The ultra–fast–soft (UFS) rectifiers provide best in the class switching speed as well as softness in recovery.

Combined the new generation of copack products provide users with a clear competitive advantage.

INTRODUCTION

Motorola brought into market the new generation of 600 V IGBTs and free–wheel diodes (FWD) in 1997. These stand–alone and copack products were introduced in discrete TO–220 and TO–247 packages, followed by VersaPower™ modules and other packages.

The E–series IGBTs are based on the new technology platform particularly developed to serve ever increasing requirements for motor control applications. The cell structure, fabrication process, and starting material were optimized to obtain the best possible tradeoffs for this application. The triangle shown in Figure 7–1 symbolizes the tradeoff process involved in the design of IGBTs. The three vertices of this triangle represent conduction losses (V_{CEon}), switching losses (E_{off}) and short circuit ruggedness (tsc). While the switching losses are lowered as carrier injection efficiency is increased and the life time is reduced, the conduction losses go exactly the opposite way. They increase. The short circuit withstand capability is improved by incorporating design changes which reduce short circuit current. Just as for switching losses, improvement in short circuit rating is accompanied by increase in conduction losses.

There are however design parameters which help reduce conduction losses without adversely influencing the other two. This was achieved for our new E–series IGBTs. Consequently E–series offer significantly lower conduction losses and short circuit ruggedness while maintaining the ultra fast switching speed of the existing (STD) IGBTs.

E–series IGBTs are also supplied with inherent ESD protection in the form of an integrated gate–emitter zener clamp, adding to the ruggedness of these IGBTs in motor speed control environment.

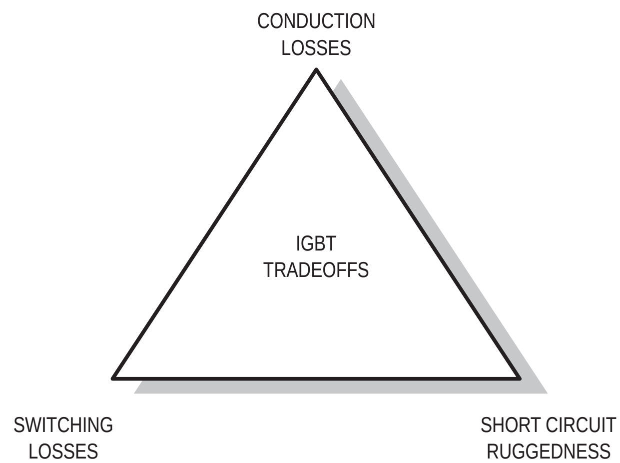

Figure 7–1. IGBT Tradeoff Triangle

The free–wheel diodes are an integral part of motor drive application. Motorola has recently made tremendous strides towards perfecting the speed and softness in the recovery of these diodes. The UFS series rectifiers are optimized for extremely fast switching speed and softer recovery throughout the current range. These characteristics have helped reduce turn–on losses in IGBTs and generation of EMI and other transients by a great margin.

The specific utilization of IGBTs and freewheeling diodes within a motor control system is to provide the inversion function from a DC Bus to a sinusoidal waveform. The AC waveform provided to the load is in the 1.0 Hz to 120 Hz frequency range, and is achieved by switching the IGBTs at PWM frequencies in the range of 4.0 KHz to 20 Khz. Please refer to Figure 7–2.

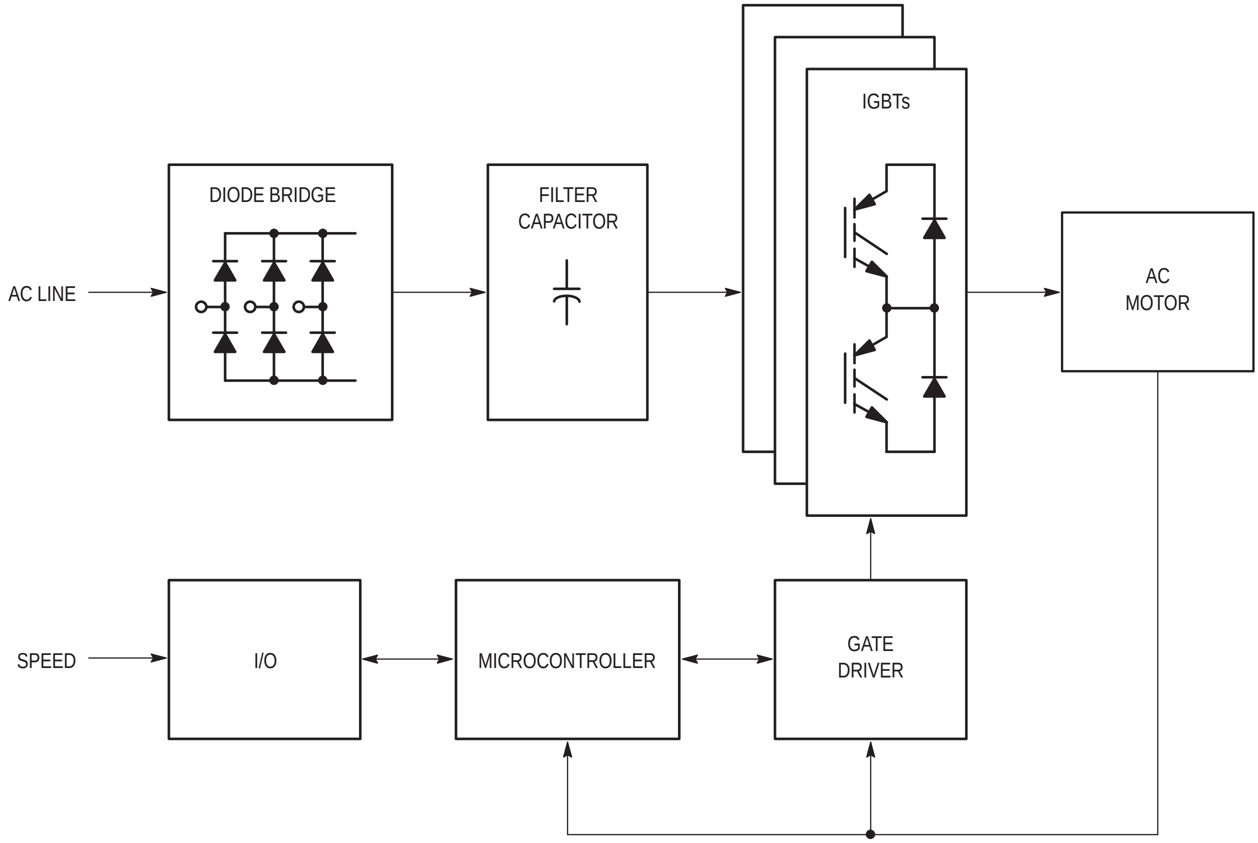

Figure 7–2. Typical IGBT AC Motor Drive Application

Table 1. Typical Switching Losses

	STD 25°C	E–SERIES 25°C	STD 125°C	E–SERIES 125°C
E_{on} (mJ)	1.32	0.51	1.85	0.73
E_{off} (mJ)	0.84	0.84	1.50	1.54
Total (mJ)	2.16	1.39	3.33	2.27

NEW E–SERIES IGBTs

Conduction voltage drop of E–series is compared with the STD IGBTs in Figure 7–3. The graph shows V_{CEon} at 125°C as a function of active–area current density for both technologies.

As seen from this graph, the V_{CEon} of E–series IGBTs is improved by 700 mV at 100 A/cm^2 to 1.95 V typical. That is over 25% improvement in conduction losses! The reduction in typical value of $V_{CE(on)}$ combined with tightening of process related parameter distribution has made it possible to spec E–series IGBTs more aggressively. As discussed earlier, this improvement was achieved without sacrificing the fast switching speed of these motor control IGBTs.

Turn–off switching losses of E–series IGBTs are similar to the STD IGBTs as described in the introduction section. Figures 7–4a & 7–4b show turn–off losses waveforms at 125°C of Standard and E–Series IGBTs, respectively. While the rate of rise of voltage for the E–series is slower, the current tail is much shorter which produces almost equal turn–off losses. The E_{off} measurement at 20 A, 360 V, and 125°C for the E–series MGW21N60ED under test is 1.54 mJ. Table 1 shows the rest of the measurement data for these IGBTs.

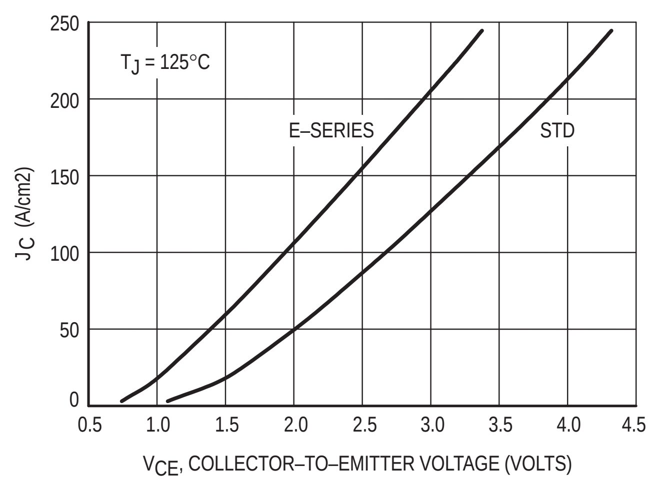

Figure 7–3. IGBT $V_{CE(on)}$ versus J_C

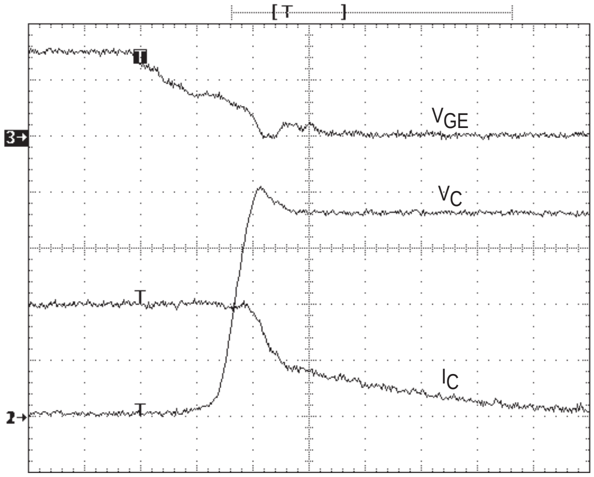

Figure 7–4a. IGBT Turn–Off Test Waveforms of STD Series MGW20N60D (100 ns/div) @ I_C = 20 A, V_{CC} = 360 V, V_G/R_G = 15 V/20 Ω, T_J = 125°C

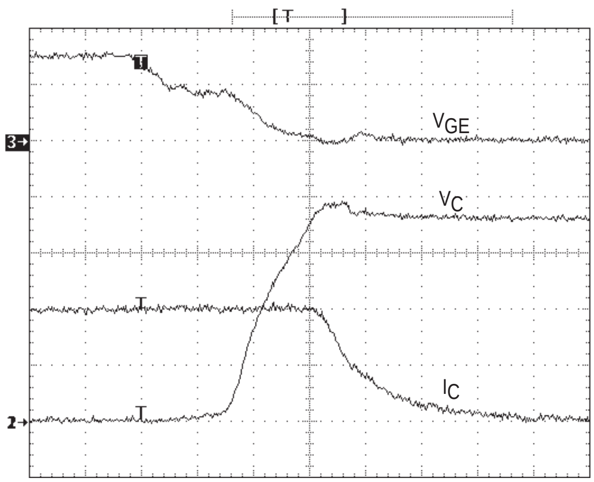

Figure 7–4b. IGBT Turn–Off Test Waveform of E–Series MGW21N60ED (100 ns/div) @ I_C = 20 A, V_{CC} = 360 V, V_G/R_G = 15 V/20 Ω, T_J = 125°C

Turn–on switching losses of IGBTs are largely dependent on reverse recovery behavior of the free–wheel diode in inductive load applications. The turn–on process is complete only after the FWD has recovered and begins to block full DC link voltage. Slower diodes, besides adding recovery current transient to the load, prolong turn–on process as seen from Figures 7–5a & 7–5b. Switching can be quickened by using higher gate input voltage or lower gate resistance, thereby increasing the rate of rise of current in IGBT and corresponding rate of fall of current in the FWD [1]. The speeding up however is limited by the nature of reverse recovery. Snappier recovery requires that turn–on *di/dt* be reduced in order to avoid occurrence of unsafe recovery voltage transients and generation of excessive EMI. Softer FWDs, on other hand, allow faster IGBT turn–on.

Faster and softer recovery of FWD is therefore very important in such applications. Motorola has accomplished this by designing a series of Ultra Fast Soft (UFS) diodes. The improvement in both speed and softness as compared to the STD diode are illustrated in Figures 7–5a & 7–5b. All circuit conditions being identical, the new copack solution containing UFS incurred almost twice as fast switching and dissipated only 0.73 mJ @ 20 A and 125°C. That is a 60% reduction in turn–on losses! More measurement data are provided in Table 1. Further discussions on UFS diode characteristics are carried out in a later section.

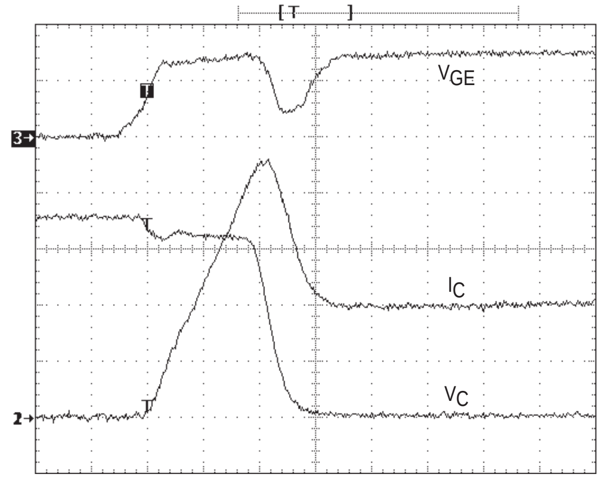

Figure 7–5a. IGBT Turn–On Test Waveforms for STD Series MGW20N60D (100 ns/div) @ I_C = 20 A, V_{CC} = 360 V, V_G/R_G = 15 V/20 Ω, T_J = 125°C

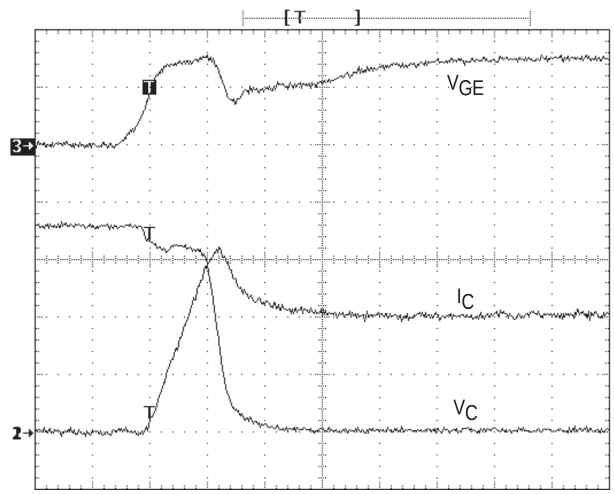

Figure 7–5b. IGBT Turn–On Test Waveforms for E–Series MGW21N60ED (100 ns/div) @ I_C = 20 A, V_{CC} = 360 V, V_G/R_G = 15 V/20 Ω, T_J = 125°C

Short circuit withstand capability of IGBTs is a function of (1) losses generated during the fault period and (2) devices capability to remain unlatched during and at the switching off instant of fault current [2]. Great strides of progress have been made with E–series IGBTs and we have improved short circuit endurance time (tsc) from 4.0 μs to 10 μs at 125°C. As seen from Figure 7–6 the short circuit current of E–series IGBT is considerably lower than that for the STD IGBTs, reducing the loss dissipated. The allowable DC bus voltage is increased for this series of IGBTs as seen from Figure 7–6b.

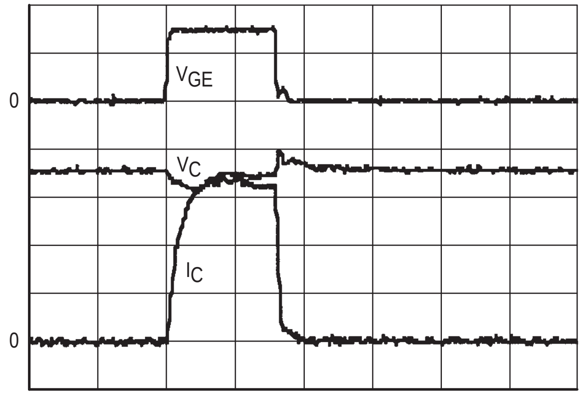

Figure 7–6a. IGBT Short Circuit Test Waveforms @ 125°C for STD Series MGW20N60D (250 ns/div) Scales: I_C – 50 A/div, V_{CC} – 100 V/div, V_G – 10 V/div

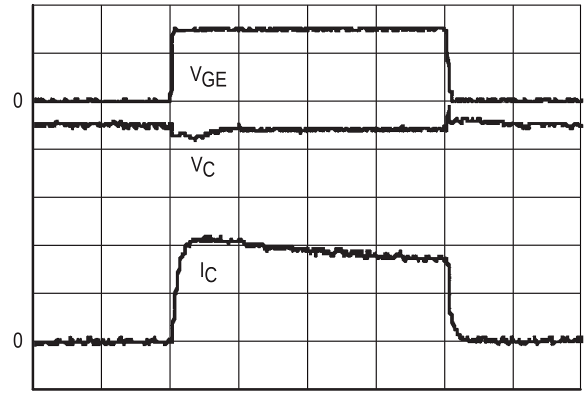

Figure 7–6b. IGBT Short Circuit Test Waveforms @ 125°C for E–Series MGW21N60ED (250 ns/div) Scales: I_C – 50 A/div, V_{CC} – 100 V/div, V_G – 10 V/div

Gate–Emitter back–to–back zener clamp is integrated in the E–series IGBTs as shown in Figure 7–7 to provide ESD protection in industrial environments [3]. This monolithic strategy for gate protection has been successfully used for many years by device manufactures such as Motorola for power IGBTs designed and used in automotive ignition control circuits. The advantages include increased gate ruggedness as well as reduced circuit board part counts which results in fewer assembly steps and higher reliability in customer applications.

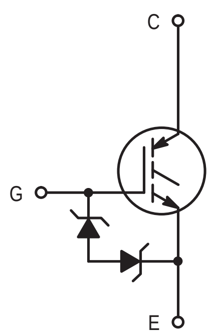

Figure 7–7. E–Series IGBT with Gate Protection

Table 2. Typical G–E Clamp Leakages for MGP21N60E

I_{GSS} @	V_G = 15 V	V_G = 20 V
25°C	2.0 µA	15 µA
125°C	5.0 µA	35 µA
150°C	8.0 µA	50 µA

Implementation of on–chip zener clamps requires little active area, so conduction voltage drop is not sacrificed. An increase in gate–to–emitter leakage of a few tens of microamps is measured, but this is insignificant when compared to leakier circuit components such as opto–couplers. Measured gate–emitter leakage currents at 15 V and 20 V at three temperatures are shown in Table 2 for E–series IGBTs.

NEW UFS SERIES FREE–WHEEL DIODES

Conduction voltage drop of new UFS diodes is compared with the STD diodes in Figure 7–8. Here again the diode VF at 125°C is plotted against the active–area current density. As observed from this plots forward voltage drop of UFS diodes is actually higher than the STD diodes. At 100 A/cm^2 for example it is 1.25 V, which is 400 mV higher. The overall performance of the diode in inverter applications has however greatly improved as savings in switching losses, which are calculated to have more than compensated for the increase in V_F. Appropriate size of diodes are selected to assure that the diode does not become a limiting factor in copack applications. This is further clarified in the section on “frequency response” of these IGBT and diodes.

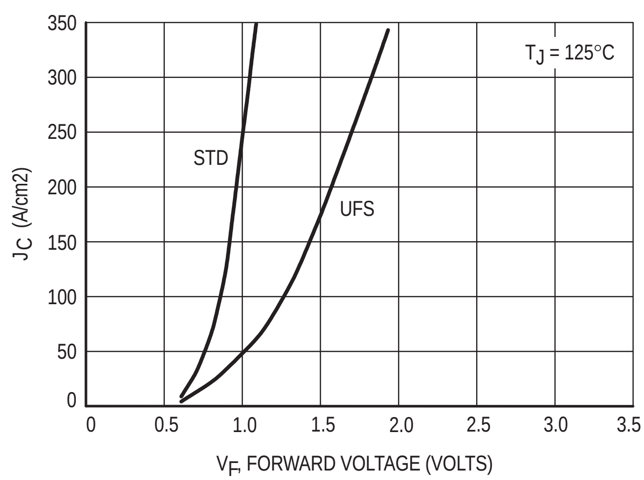

Figure 7–8. FWD V_F versus J_C

Reverse recovery of FWD directly influences turn–on losses of IGBTs in inductive load applications as described earlier in the IGBT section. As a matter of fact, the *ta* portion or first "half" of recovery time *trr*, primarily contributes to IGBT turn–on losses. The *tb* portion contributes to diode reverse recovery losses. Faster diode help reduce both of these switching losses. Figures 7–9a & 7–9b show the reverse recovery current waveforms of STD and UFS series diodes respectively. The difference in the recovery parameters between the two are huge as seen from these traces and from measurement data in Table 3. At test conditions of 200 A/μs, 360 V and 125°C, I_{rm}, t_a, t_b and Q_{rr} for the UFS diode were measured to be 9.5 A, 56 ns, 94 ns and 713 nC respectively as compared to 24.4 A, 132 ns, 94 ns and 2760 nC for the STD diodes! The remarkable reduction in recovery parameters have helped reduce switching losses dramatically. As described earlier, the typical IGBT turn–on losses reduced from 1.85 mJ with the STD FWD to just 0.73 mJ with UFS diode. With typical IGBT turn–off losses of 1.54 mJ, the faster diodes helped reduce overall switching losses from 3.39 mJ to 2.27 mJ, a reduction of 33%. Lowering of reverse recovery losses in diodes is equally impressive, however not as crucial due to their relatively low magnitude.

Softness in reverse recovery could be crucial as snappy recovery behavior may cause intolerable recovery transients and may set off ringing generating EMI noise in the system. Snappy diodes may require usage of snubber circuits which add to the cost of the converter [4]. It is therefore important to have a diode with softer recovery. UFS diodes have been particularly designed to assure fast but soft recovery at full range of current magnitudes and operating junction temperatures as seen again from Figures 7–9a & 7–9b.

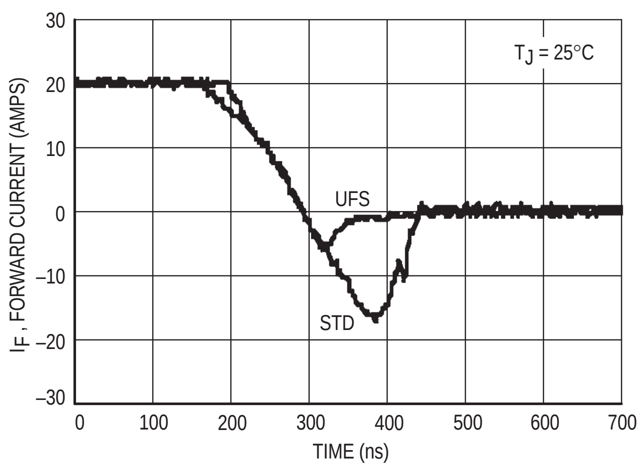

Figure 7–9a. Typical FWD Reverse Recovery Waveforms @ I_F = 20 A, di/dt = 200 A/μs, and V_{CC} = 360 V

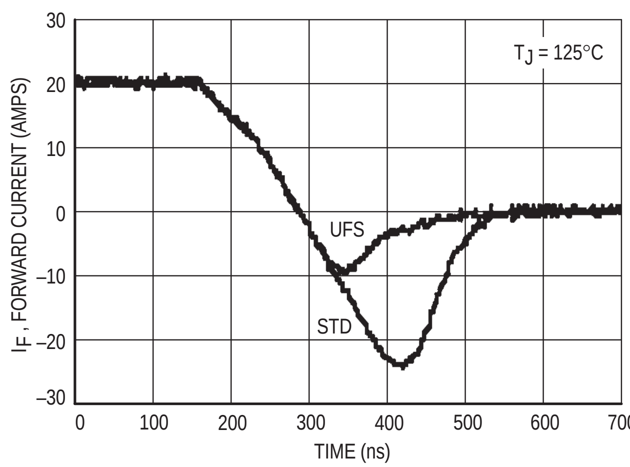

Figure 7–9b. Typical FWD Reverse Recovery Waveforms @ I_F = 20 A, di/dt = 200 A/μs, and V_{CC} = 360 V

Table 3. Typical FWD Reverse Recovery Parameters @ I_F = 20 A, di/dt = 200 A/μs, V_{CC} = 360 V STD MGP20N60 versus UFS MGP21N60E

	STD 25°C	**UFS 25°C**	**STD 125°C**	**UFS 125°C**
I_{RRM} (A)	16.8	6.1	24.4	9.5
t_{rr} (ns)	148	55	226	150
t_a (ns)	92	26	132	56
t_b (ns)	56	29	94	94
Q_{RR} (nC)	1400	168	2760	713
di/dt (A/μs)	203	205	208	201
t_b/t_a	0.61	1.1	0.71	1.6

"Frequency Response"

Figure 7–10 represents the RMS output current versus switching frequency of a full bridge inverter supplying 60 Hz sinusoidal output current to a motor load. The performance of the E–series IGBT with a UFS diode is plotted against that of STD IGBT and diode. The representative devices were 20 A STD and E–series/UFS copacks. Calculations were carried out using measured data for conduction and switching losses as covered earlier in this article. The sink and junction temperatures were kept constant at 90°C and 125°C respectively. Other simulations conditions are described in the figure.

The advantage of this method for performance evaluation is that all relevant device losses and thermal impedances are taken into consideration simultaneously [5]. A single plot represents performance of an IGBT/FWD pair under given set of application conditions and over a broad range of switching frequencies.

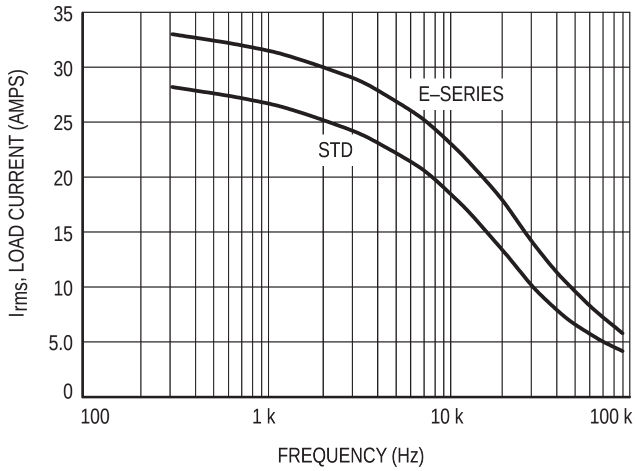

Figure 7–10. Typical RMS Load Current versus Switching Frequency Simulations Conditions: Full Bridge Inverter 60 Hz Sinusoidal Output, T_J = 125°C, T_{sink} = 90°C, PW = 33 W, V_{CC} = 360 V

Note that the diode losses did not play a critical role, and as such, the data in Figure 7–10 compares only the capability of IGBTs. All three significant losses: conduction, turn–on switching and turn–off switching losses were considered. The E–series IGBT and UFS diode solution significantly improves efficiency of the inverter. As demonstrated in this figure the resultant gain in maximum allowable motor RMS current is between 20% to 35% at switching frequencies range from 4.0 KHz to 20 KHz.

CONCLUSION

Motorola's new 600 V E–series IGBTs and UFS free–wheel diodes are designed for efficient and rugged operation in motor control applications. The IGBT technology has made possible simultaneous reductions in IGBT conduction and switching losses while enhancing short circuit capability. Both ultra–fast and soft recovery characteristics have been achieved with the new diode technology. Combined, the pair increases maximum allowable motor RMS current by 20% to 35% and provides user with competitive advantage.

A gate–to–emitter zener clamp is integrated to enhance ESD protection of IGBTs for safe handling in industrial environment.

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Section 8
Comparison of the Performance of Several IGBT Device Technologies in a 1 HP, Adjustable Speed Motor Drive

ABSTRACT

Recent developments in IGBT technologies have focused on the tradeoffs of the device forward voltage drop ($V_{CE(sat)}$) versus switching speed limitations due to device “tail time” in motor drive applications. Tail times are related to the stored charge in the IGBT’s internal BJT and can be reduced at the expense of increasing the $V_{CE(sat)}$ of the device. Several technologies have been developed that attempt to optimize both switching times and forward voltage drop while providing rugged short circuit capability. The following work investigates the performance of several IGBT technologies in an adjustable speed motor drive application.

An off–line, 1 HP motor control test bed was used to test the performance of 600 V, 20 amp IGBT’s in terms of overall efficiency and collector currents. The device performances were compared in terms of temperature rise, power dissipation, collector currents, and switching speed.

IGBT’s IN MOTOR DRIVE APPLICATIONS

IGBT’s are quickly becoming the transistor of choice for motor control applications. The characteristics that make them favorable include the ability to pass greater current than a equivalent die size MOSFET transistors with more favorable drive schemes than bipolar transistors. In addition, IGBT’s in many instances have less conduction loss due to the $V_{CE(sat)}$ when compared to the $R_{DS(on)}$ of MOSFET’s (this is due in part to the IGBT’s loss based on collector current while the MOSFET’s loss is based on the drain current squared). An unfavorable attribute exhibited by IGBT’s is the “tail time” that results from stored charge in the internal PNP transistor. The tail time is sacrificed at the expense of forward voltage drop, $V_{CE(sat)}$ as shown in Figure 8–1. Devices are optimized for efficient operation in applications with regards to conduction and switching losses. The tail time issue also dictates switching speed. Motor controllers tend to operate at switching frequencies from 6 kHz to 15 kHz. This is due in part to the audible range of the human ear. IGBT’s with tail times of less than 300 ns are being realized and these devices work well at 15 kHz. Work is under way to decrease the tail time and V_{CE} drop so that IGBT’s can be operated at even higher frequencies and compete with existing MOSFET’s in motor control and power supply applications.

1 HP VARIABLE SPEED MOTOR DRIVE TEST BED

A new line of IGBT devices has recently been introduced by Motorola Inc. Devices rated at 600 V, 20 amp, are included and targeted for industrial drives of 120 Vrms and/or 230 Vrms. These particular IGBT’s were ruggedized for motor control applications and are specified to withstand 10 µs of short circuit current. Six of these devices were inserted into a bridge configuration in 3 phase, 1 HP, variable speed, motor controller that operated at 9.92 kHz. The test system was then used to evaluate the static and dynamic effects that different generations of IGBT’s had on overall system performance. Figure 8–2 illustrates the test system which uses a volt–Hz, open loop control technique based on an HC16Y1 Motorola microprocessor. This system is a mobile demonstration kit when using a 1/30 HP motor as well as having the ability to drive a heavy duty 1 HP bench set up. Two methods of determining IGBT performance, static and dynamic measurements, were used.

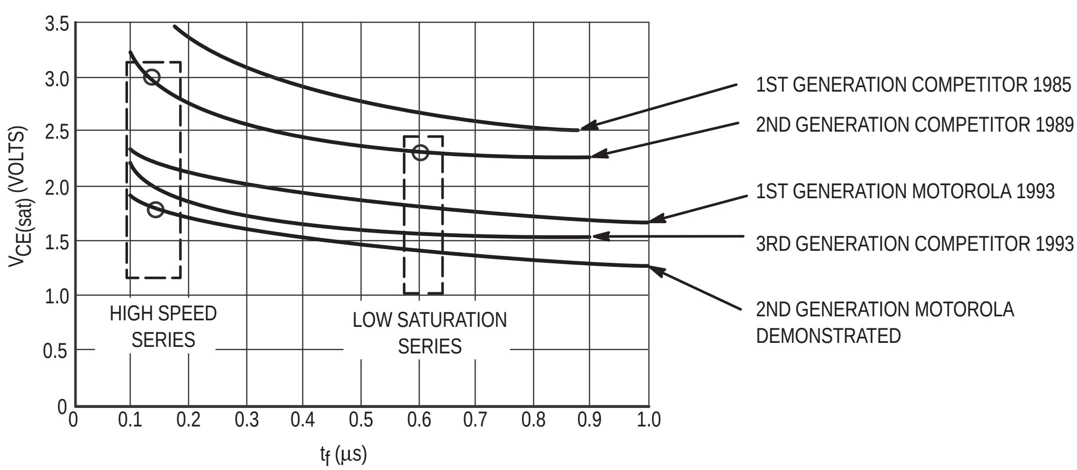

Figure 8–1. IGBT $V_{CE(sat)}$ Relation to Device Fall Time

Test Diagram
Controlled Parameters are Shaded or in *Italics*

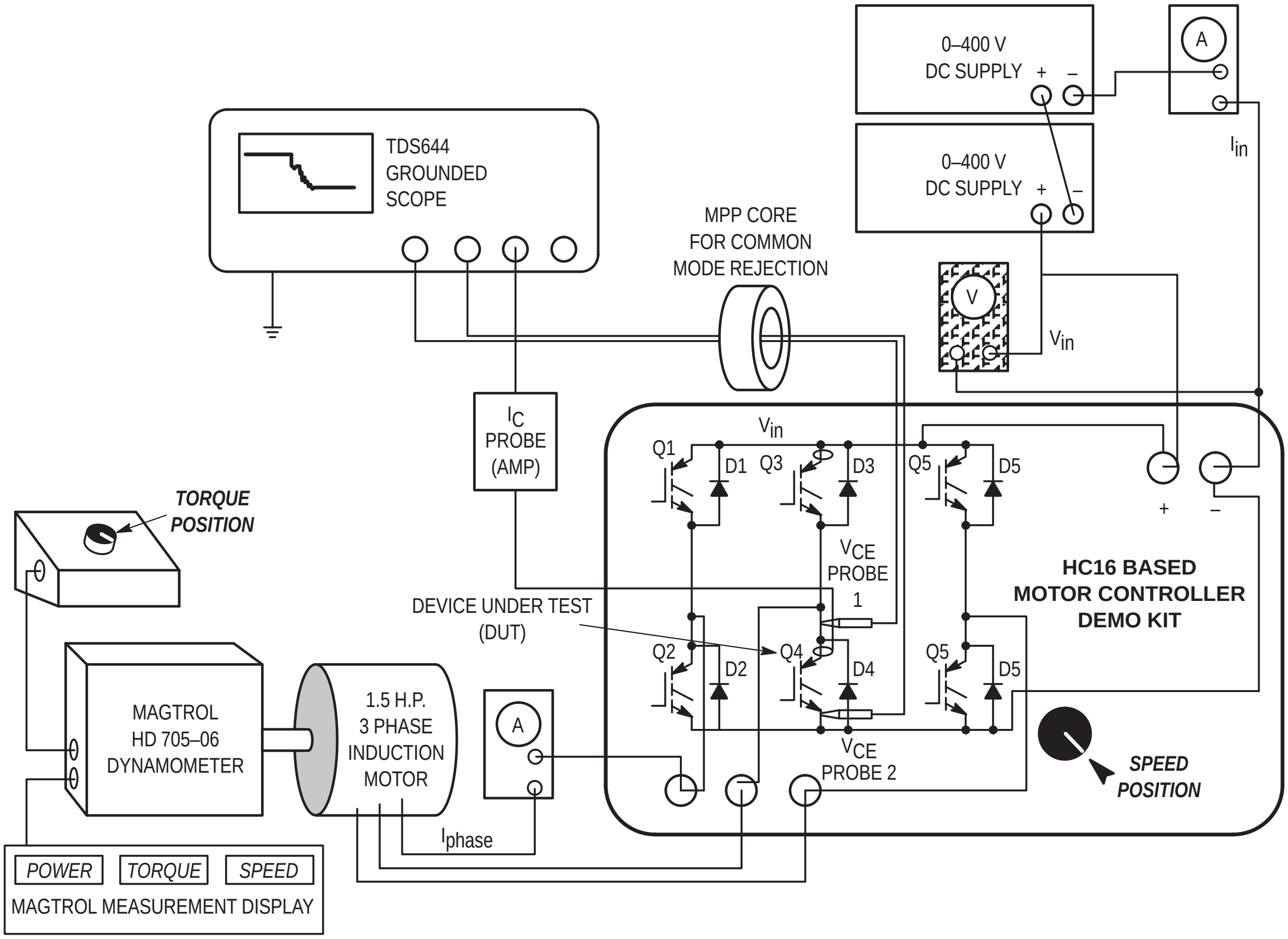

Figure 8–2. 1 HP Variable Speed Motor Drive Test Bed

STATIC MEASUREMENTS

Static measurements provide overall insight into the IGBT's effect on system efficiency. Static measurements of the system "black box" performance were read from meters. The controlled parameters (indicated in Figure 8–2 by shading or by using *italic* print) are the input voltage, and the motor speed, torque, and power (the Magtrol dynamometer measurements). The motor measurements taken from the dynamometer will include the motor losses. Therefore, a current meter is placed in series with one of the motor phases in order to measure output current I_{phase} in an attempt to separate motor losses from those of the drive circuitry. The input variable is input current I_{in}. Input power differences were measured for the various IGBT's being tested and the results are presented in Table 1.

Although the efficiency measurements in Table 1 include the motor losses and some accuracy may be lost by using the dynamometer to measure the output power, one must keep in mind that the controlled test parameters still allow for a fair comparison of the IGBT generations. For instance, the phase currents vary only 0.8% while the efficiencies vary 5.6%. Based on this, the newer generation parts have improved the efficiency of the motor drive. In addition, the heat sink temperature values show that the generation 2 parts are dissipating less heat.

Table 1. Measured System Efficiency of Motorola First and Second Generation IGBT's at 1 HP and 1750 RPM (V_{in} = 300 Vdc)

Measured Parameter	Generation #1	Generation #2
Average Input Power	891 Watts	818 Watts
Average Phase Current *(I_{PHASE})*	3.88 Amps AC	3.85 Amps AC
Average Output Power *(Power)*	752 Watts	753 Watts
Heat Sink Temperature (T_A = 27°C)	39.7°C	37.0°C
Average System Efficiency	84.4%	92.0%

DYNAMIC MEASUREMENTS

To further understand the data, analysis on the dynamic aspects or switching waveforms was performed. Dynamic measurements include the IGBT's collector current and $V_{CE(sat)}$ values captured on a TDS644 oscilloscope. These values will be measured near the peak of the phase current half sine wave shown in Figure 8–4 for each of the six IGBT's rotated into the Q4 spot. Control variables will be 300 Vdc input with 750 watts (approximately 1 HP) output. Then, the average $V_{CE(sat)}$ and tail times will be taken and the test set up repeated for each IGBT technology. In this manner, IGBT performance can be assessed because the devices will be operating in similar fashions. Overall IGBT drop is difficult to measure due to the varying AC waves of the controller. However, by using the differential method proposed in Figure 8–2, $V_{CE(sat)}$ measurements were measured. A temperature probe was inserted on the heat sink near the DUT to measure device operating temperatures for comparison.

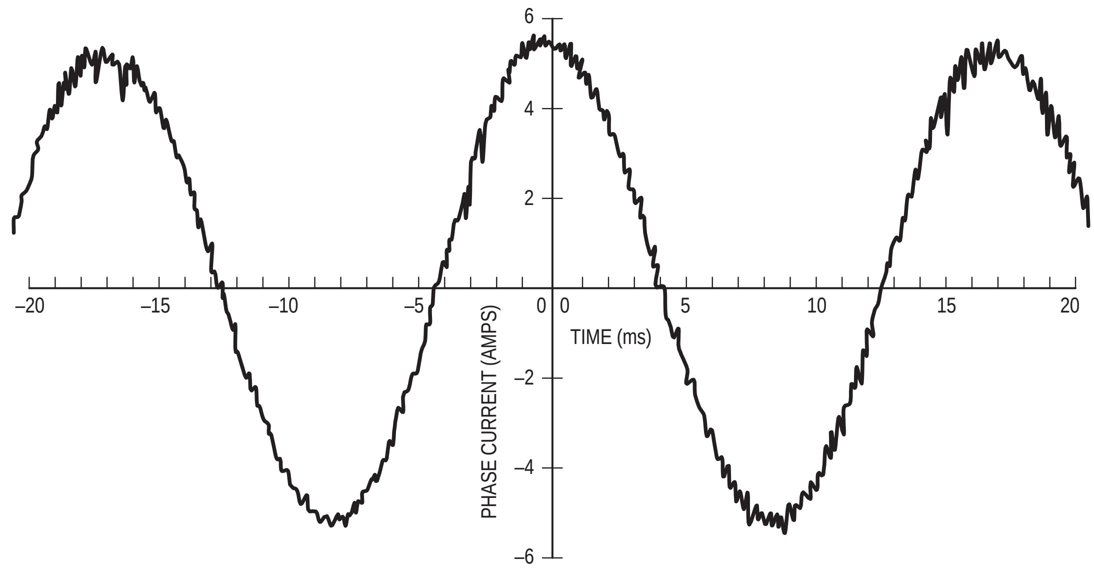

Figure 8–3. Motor Phase Current

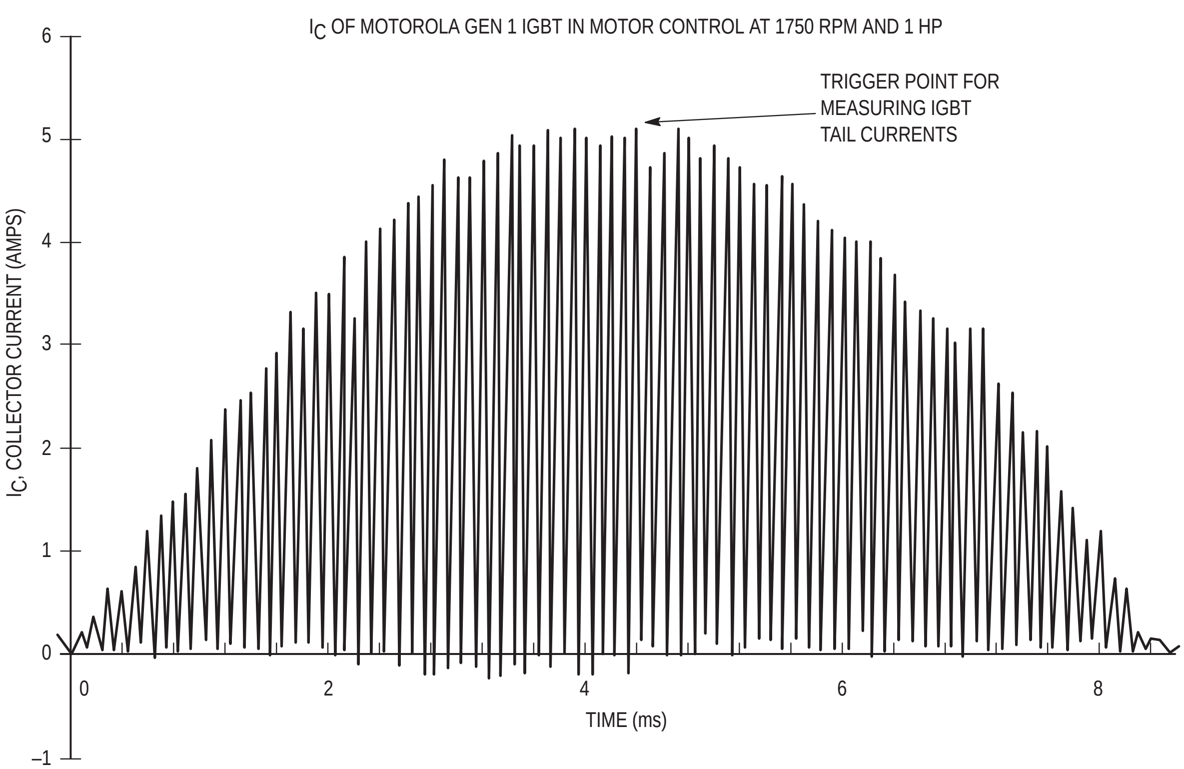

Figure 8–4. IGBT Collector Current

COLLECTOR CURRENT WAVEFORM ANALYSIS

In order to determine the switching performance of the IGBT's, the collector currents were captured on a digital oscilloscope and the results are shown in Figures 8–5 and 8–6. From the typical curves shown it is hard to determine if the generation 2 parts show an improvement. For this reason, the measurements shown in Figures 8–5 and 8–6 were taken for six devices rotated into the Q4 position. The results are shown in Table 2. From the measurements it is apparent that overall, a 5% improvement in the switching speed was realized with the second generation parts.

As mentioned earlier, $V_{CE(sat)}$ usually increases when the tail time is reduced by changing the design of the part. The assessment of the actual $V_{CE(sat)}$ was also an average of values recorded from a switching waveform. However, the large duration of the collector to emitter voltage swing shown in Figure 8–7 will reduce the accuracy realized by using a differential voltage measurement. In addition, the bottom rail of the IGBT bridge also swings in reference to the ground level and isolated measurement techniques are limited. The approach to the final data was to look for a trend in $V_{CE(sat)}$ instead of relying on the accuracy of the experiment. In Table 2 it is apparent that the generation 2 devices exhibited lower $V_{CE(sat)}$ even with the improved tail time. The improvement of 20.2% $V_{CE(sat)}$ most likely had more of an effect on efficiency than did the improved switching speed.

Table 2. Measured Average Tail Times and $V_{CE(sat)}$ Values for Motorola First and Second Generation IGBT's at 1 HP and 1750 RPM (V_{in} = 300 Vdc)

Measured Parameter	Generation #1	Generation #2
Average Collector Current Tail Time	246 ns	234 ns
Average $V_{CE(sat)}$	2.23 Volts	1.78 Volts

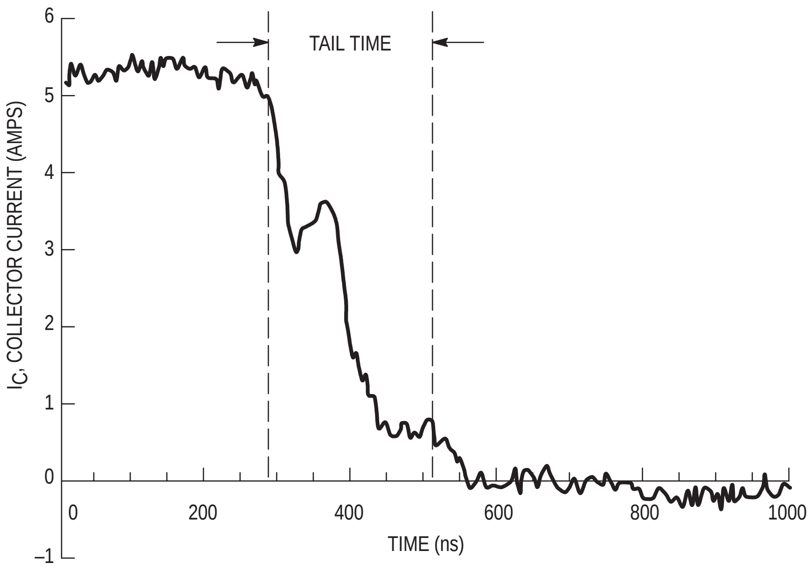

Figure 8–5. Tail Time Measurement of Generation 2 IGBT in a 1 HP Motor Drive at 1750 RPM

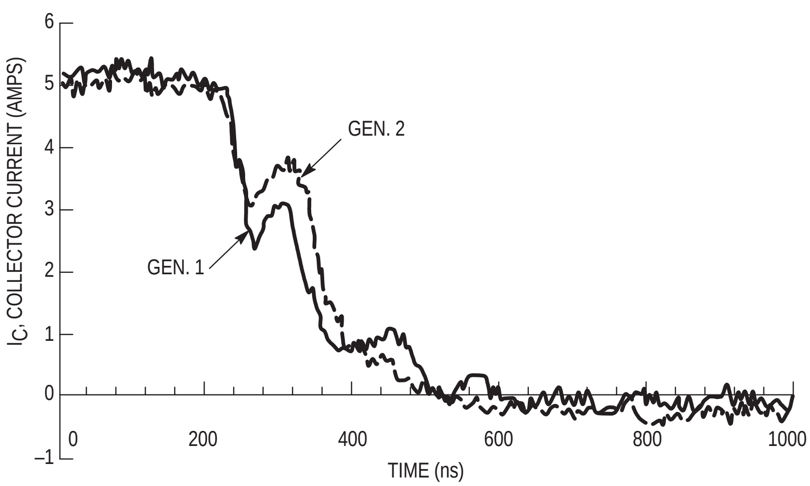

Figure 8–6. Tail Time Comparison of 600V Generation 1 and Generation 2 IGBT's in a 1 HP Motor Drive at 1750 RPM

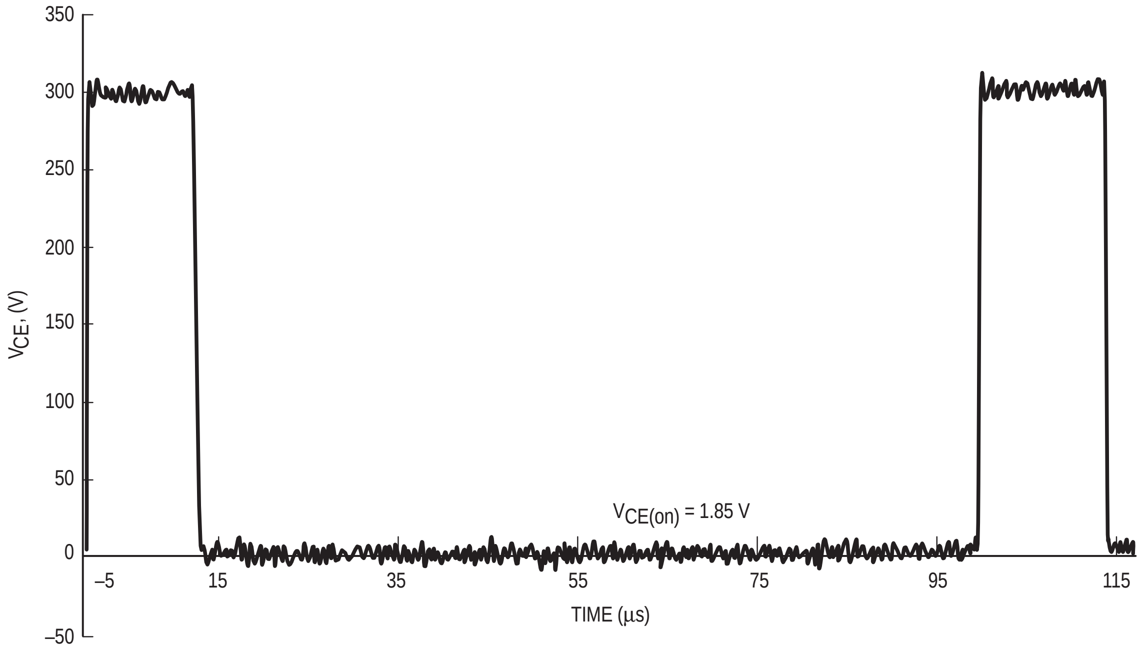

Figure 8–7. Typical V_{CE} Waveform of the Motorola Generation 2 IGBT in a 1 HP Motor Drive at 1750 RPM

SUMMARY

A new series of IGBT's have been developed and tested for a one horse power motor controller. The second generation of parts had a definite performance improvement over the initial design and the result was a 9% improvement in system efficiency and a reduced heat sink temperature. The improved efficiency was a result of a reduced tail time and a reduced $V_{CE(sat)}$. These results will be used to optimize the design of future power transistors to realize even better performance.

Section 9
Power Module Control Design

ABSTRACT

The control and interface circuits for power transistor modules that are used in 50 to 100 kW motor drives are difficult to design because of the 400 to 600 A currents, 400 V operating levels, and fast switching times. Each of the power module control design functions is examined, as well as futuristic semiconductor devices that will simplify the control circuit. These functions include: Logic–to–power module interface, DC–DC gate bias power supply, IGBT gate driver, over current protection, temperature sensing, under voltage shutdown, and fault output interface. The module control functions are usually located on an external printed circuit board. Recent progression in power IGBT modules have improved the ease of interfacing to the power module by locating the control circuit board in the module. These "smart" modules, while easier to use, cost more and place pre–defined limits on circuit flexibility. An alternative modular approach is shown.

INTRODUCTION

Power modules are used primarily in the power stage of motor drives. The power module's control circuits receive logic level commands from the motor's speed or torque computer. After receiving these logic signals the power module's circuitry activates the power devices in a manner that controls the motor's speed, torque, direction, and, in some cases, turns the motor into a generator. The module's control circuits can be divided into several elements as shown in Figure 9–1.

Each of these elements requires special design attention to work reliably with a 400 to 800 A, 600 V power module that may operate at a frequency of 20 kHz. The module's power device technology also affects the design criteria. IGBT (insulated gate bipolar transistor) power devices appear to be the power device of choice for high voltage and high current controls. MCT (MOS controlled thyristors) devices are also available but require special care in their drive circuitry and may exhibit reduced reverse biased safe operating area.

IGBTs and soft fast recovery rectifiers configured in a half H switch are normally used for large three phase motor drives. The IGBT gate driver requirements primarily determine the module control supply voltages. A positive 15 V gate on bias is a defacto industry standard for IGBT power modules. Raising the bias voltage to 20 V would improve the IGBT's forward on voltage, but at the risk of reducing its short circuit ability. The higher gate voltage allows much higher levels of short circuit current to flow, thereby increasing the chances of die failure or latch–up. Reducing the gate voltage to 10 V increases the IGBT's on voltage by about 15% at its rated current level. A reduced gate voltage has more effect when the IGBT's load current is doubled. A 400 ampere to 800 ampere load current increase will usually cause the 10 V gate biased IGBT to pull out of saturation before reaching 800 ampere. Most 400 amperes rated IGBT modules will remain in saturation when conducting 800 amperes with a 15 V gate bias.

Using a negative gate bias to the IGBT insures that the IGBT remains off during the time following the flow of the free wheeling diode's reverse recovery current [1]. A –5 V gate off bias also improves the IGBT's chances of survival during dangerous overloads or abnormal operating conditions by insuring that the gate bias on the non–shorted IGBT remains stable. Raising the IGBT's gate threshold to 8 V, for example, may eliminate the need for a –5 V gate bias.

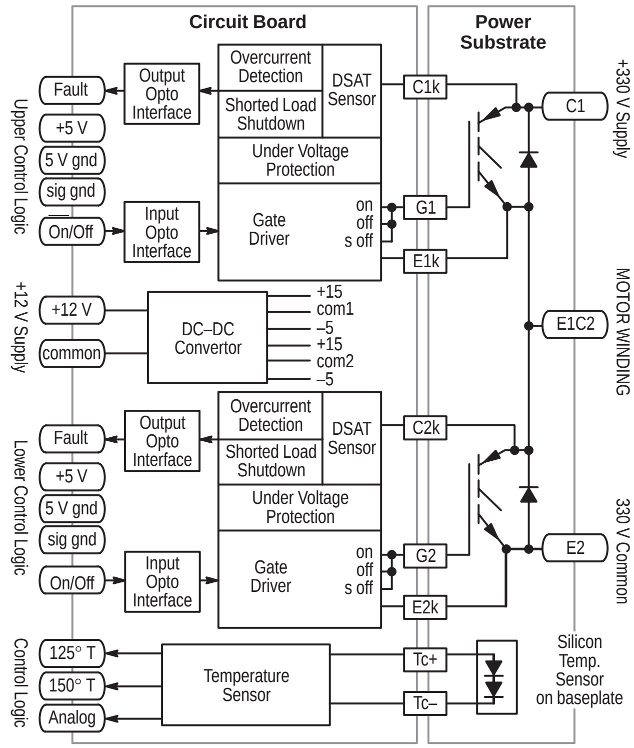

Figure 9–1. The Power Module Control Consists of Several Elements

CONTROL FUNCTIONS

Optocoupler Interface

Optocouplers were chosen because of their cost and performance. Other isolated interface methods that could have been used include pulse transformers, fiber–optics, and piezoelectric couplers [2]. The optocoupler as shown in Figure 9–2 provides high voltage isolation from the logic input to the power output stage. The input signal is a logic 0 for switching the IGBT on and a logic 1 or open for switching the IGBT off. The input logic 0 signal drives a normally biased on transistor switch to an off state, which switches on the optocoupler LED, and the IGBT. The logic input 0 or low allows for a possible open or broken wire from the motor control logic. Open or intermittent connections seem more likely to occur than short circuits in cables or connectors.

The optocoupler's LED current is set to 10 mA by a current source integrated circuit. This 10 mA value permits higher temperature operation. The optocoupler's specification sheet uses 16 mA as a nominal value. At 10 mA the CTR (current transfer ratio) is specified at 15 to 25%. The optocoupler output loading is therefore set for 1.5 mA or 15% of the LED current. One other advantage of using the current source is that the

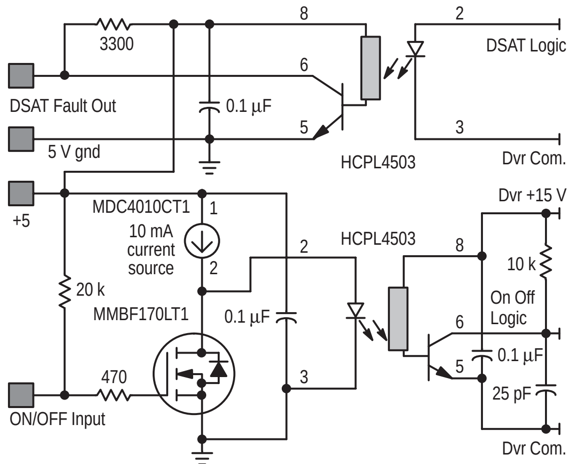

Figure 9–2. Optocoupler Interface Circuit for Input and Output Signals

optocoupler LED current will be held fairly constant over extreme temperature swings and optocoupler LED V_{fon} device to device variations. An alternate method would be to use a 330 ohm 1/8 watt resistor in place of the current source IC.

When the optocoupler LED is in conduction, the optocoupler's output pulls low. A 10 k pull up resistor value sets the optocoupler sink current to 1.5 mA. The output low–to–high time is set internally by the optocoupler and the pull up resistance value as well as the capacitance of whatever is connected to the optocoupler output line. In this design the on–off optocoupler output is connected to about 25 pF of capacitance. The time constant for 10 k and 25 pF is about 1.25 µs for 0 to 99% and 0.25 µs for 0 to 66%. The optocoupler's low–to–high time is specified at about 1µs. This means that the optocoupler's output will have uneven propagation delays, 1 µs high–to–low, 2.25 µs low–to–high. Increasing the optocoupler's LED current will allow a lower value pull up resistor to be used, which will speed up the optocoupler's output low–to–high performance. The problem with lowering the pull up resistance is that the optocoupler is only specified to operate at 70°C at an LED current level of 16 mA and its CTR peaks at about 6 mA. The CTR degrades by 25% with a temperature rise from 25° to 100°C. Therefore, a value of 10 mA appears to be a good compromise between fast switching and high temperature operation.

The fault output design is similar to the input optocoupler circuit. Its output is pulled up with a 3300 ohm resistor to +5 V bus. When a fault occurs the optocoupler LED is switched off, allowing the optocoupler output to pull high to 5 V. Under normal operation the gate driver circuitry will switch on the fault optocoupler LED, which pulls the optocoupler output low, indicating that the gate drive circuitry is operating.

Figure 9–3 shows what an optimized optocoupler for high power motor control applications might look like. This conceptual device minimizes external parts and uses an H bridge amplifier with a current source.

IGBT Gate Driver

The gate driver is the core of the control module. It must function in a stable manner under a wide variety of conditions, such as shorted loads, reduced power supply voltages, and variable pulse width switching requirements. Charging and discharging approximately 100,000 pF of gate capacitance in about 400 ns requires a pre–driver and a power driver stage.

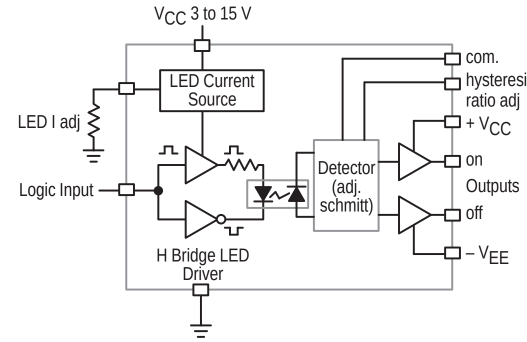

Figure 9–3. Optocoupler Conceptual Design for Input Logic to Gate Drive

There are several gate pre–driver ICs available that accomplish some of these requirements [3]. To obtain stable operation during shorted loads or abnormal control signals (i.e., both top and bottom IGBTs concurrently driven on) the IGBT gate drive impedance should be very low. Unfortunately, the IGBT switching times are usually controlled by a series gate resistor of a few ohms which, in effect, sets the minimal gate driving impedance. This is one reason a negative voltage off bias is beneficial. Noise spikes generated by a shorted load or other abnormal events have to overcome the negative voltage bias plus the IGBT threshold voltage before the non–shorted IGBT can switch on and cause more problems.

Other noise spikes that affect the IGBT's operation are associated with the free wheeling rectifier's reverse recovery time. These noise spikes occur because the rectifier takes about 30 to 100 nanoseconds to totally switch off. During this time, the opposite IGBT is switching on, resulting in a large shoot–through current spike. This spike occurs every time a IGBT is switched on, or at a rate of up to 20 kHz. During normal operation these noise spikes are usually the most troublesome for the gate driver design to accommodate. There is research underway in new high voltage rectifier technologies that may someday alleviate this reverse recovery phenomenon.

One method to minimize noise problems in the gate driver circuit is to keep all critical control lines at a low impedance and to add RC filters to limit the bandwidth of these lines to the required minimum. The printed circuit board layout is also critical to minimize common mode coupling of the IGBT noise spikes back into the driver circuits or even into the microcontroller. All critical control lines should be routed for minimal distances and the input traces of the interface optocouplers should never be physically close to the output traces. If ground planes are used, their grounding points should not intersect control circuits. (The ground plane needs a separate return path to common.)

The gate driver circuit as shown in Figure 9–4 starts with the on–off optocoupler signal connected to a comparator. The comparator reference is set to 2 V. The optocoupler output must therefore pull lower than 2 V before the comparator output toggles high. This gives some noise margin to the optocoupler output and speeds up its 2.25 µs low–to–high time. The comparator output signal, which is either less than 1 V (IGBT off) or at +15 (IGBT on) is resistor coupled to each input of a dual FET pre–driver IC. The resistors are required for the DSAT control logic to function correctly.

The two inverted outputs of the FET driver individually drive a P FET and an N FET driver stage that controls the IGBT gate. When the comparator's output signal toggles high, the pre–driver IC's two outputs go low. One output switches on the

P FET power device which applies +15 V bias to the IGBT gate and the other output switches off the N FET power device, thereby unclamping the IGBT gate. The power FET driver stage uses a P FET 20 A, 30 V, 0.1 ohm device for the turn–on driver and N FET 20 A, 30 V, 0.04 ohm devices for the normal and shorted load turn–off drivers. Both P and N FET drivers are in DPAK packages and offer high current density for their size in this application.

One difficulty with the pre–driver IC is its internal under voltage lockout design: Its outputs are toggled low during an under voltage lockout condition; this switches on the P FET driver which switches on the IGBT with much less than normal gate voltage. To circumvent this built–in problem, zener diodes were used to couple the pre–driver IC outputs over to the power FET drivers. A 6.8 V zener is connected in series with the P FET driver. When the pre–driver IC is operating in its UV lockout mode, which is 5.8 V or less, the P Channel device remains off because the 6.8 V zener is non–conductive. In normal IGBT ON operation the P FET power driver stage is biased on with 8.2 V (15 V level minus the 6.8 V zener = 8.2). An active gate clamp consisting of a NPN small signal transistor switches off the P FET when the pre–driver IC output goes high. A 2.7 ohm series resistor between the IGBT gate and P FET's drain adjusts the IGBT's rise time. When driving resistive output loads the IGBT rise time was noted to be about 200 ns.

The N FET driver output line from the pre–driver IC is connected with a 10 V zener diode to the N FET driver. During normal IGBT OFF operation the N FET driver is biased on with 10 V. The 10 V bias is obtained as follows: The pre–driver IC's OFF output state is 15 V minus the 10 V zener which leaves 5 V positive on the N FET gate, and the N FET source is connected to a minus 5 V bus, thus giving a 10 V gate–to–source bias level. An active gate clamp consisting of a PNP small signal transistor switches off the N FET when its input signal goes low. A 2.7 ohm series resistor between the IGBT gate and normal turn–off N FET adjusts the IGBT fall time. The IGBT's normal fall time was noted to be about 400 ns when driving resistive loads.

A difficult aspect of the gate driver design is controlling the –5 V off bias from the single supply powered pre–driver IC. The 10 V zener previously mentioned provides isolation, thereby allowing the N FET to operate from a minus 5 V bus and be driven from the single 15 V supply powered pre–driver IC. The IGBT is switched off with a minus 5 V bias.

Thermal scan tests of the gate driver circuit components revealed that the power FET drivers and series resistors ran about 15° above ambient. The 2.7 ohm series gate resistors are metal oxide type, which are somewhat flame resistant.

Undervoltage Shutdown

An undervoltage lockout circuit as shown in Figure 9–4 is necessary to insure that the IGBT gate bias is sufficient. An undervoltage sense IC, MC34164, is used to the detect if the 15 V bus went below 12 V. A NPN transistor is biased from the –5 V bus allowing the NPN collector to pull down the MC34164 sense input when the –5 goes below –4 V. The undervoltage lockout, allows time for all the gate control circuits to stabilize before switching of the IGBT can occur. If the DC–DC converter or other power supply type failure occurs, the under voltage lockout will shut off the IGBT. It is important that the undervoltage lockout design incorporates hysteresis that is accurate over temperature.

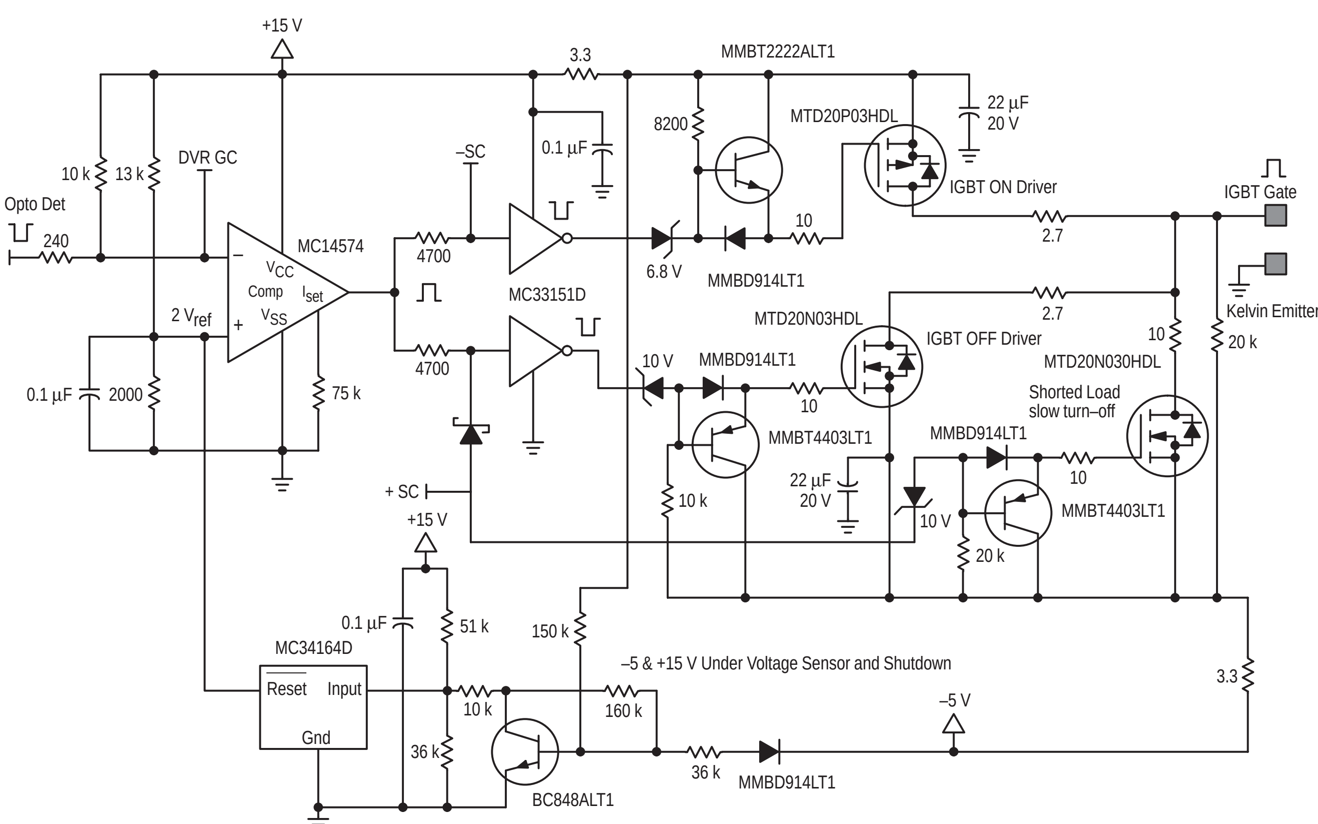

Figure 9–4. Gate Driver Circuit for Either Upper or Lower IGBT Power Devices

One effect of switching off the gate drives is that the power supply load goes down, allowing the +15 or –5 voltage to rise and reset the undervoltage lockout. This sets up an unstable mode of operation. There are two ways to correct this: Shut down the DC–DC converter before its load regulation becomes marginal and allow about 20% of hysteresis in the undervoltage lockout. This will minimize unstable operation during power up–down and low DC–DC converter input voltage conditions.

Current Sensing

A method to detect gross overcurrent levels is desirable since the power module's IGBTs exhibit high transconductance. This means that IGBT devices can conduct two or three times their maximum rated DC current level before entering a near saturation or linear mode of operation. The DSAT (de–saturation) current sensing method was chosen over the sense IGBT method because the motor type of application requires high peak currents. (Current levels are usually directly related to torque.) When a maximum torque command is invoked, the motor's peak current levels may exceed the nominal IGBT current ratings, but the IGBT can usually handle momentary over currents. As long as the IGBT stays in or near its saturation operating mode, no damage should occur if the heat management system is functioning. In effect, the DSAT method allows all the IGBT's current handling capacity to be utilized. Other methods to discern the IGBTs forward current include: Sense IGBTs, current sensing resistors, and Hall effect devices [4].

The DSAT current sensing method relies upon the IGBT's forward ON voltage to increase with its current flow. The IGBT's forward ON voltage gives a fair indication of how much current it is conducting. For example, a typical IGBT 400 A/600 V module's forward ON voltage at 200 A is 1.5 V, at 400 A it is 2.2 V and at 800 A it is over 3 V.

The output of the current sensor is connected to a dual comparator IC. Some filtering and gating are required to clean up the current sense signal. The dual comparator references are set to trip at 2.5 V for an over current indication and 3 to 5 V for a shorted load indication. The over current signal is fed back to the system controller by an optocoupler. The system program then determines what action to take. A shorted load indication is a serious event that requires the power module to protect itself from immediate failure. When a shorted load occurs, the gate drive control should respond in less than 10 microseconds. The gate drive bias is removed in a manner that will limit the IGBT's collector overshoot voltages caused by the 600 to 1000 A current flow and the inductance of the shorted load. Essentially, the gate bias is switched off slowly with a special shorted load turn–off circuit. Once the shorted load event has initiated this mode of operation, other timing circuits affect the gate driver for a time that will allow cooling of the IGBT dies. This time can vary from a few milliseconds to tenths of a second. Obviously, the system controller will also be informed that the gate driver is in a shorted load mode and will have to commence a restart or invoke other predetermined steps.

In this design, two comparators as shown in Figure 9–5 are used to detect overcurrent and shorted load conditions. The IGBT forward on voltage is connected to both comparators indirectly from a resistor limited voltage source and an isolation diode. The resistor voltage source applies up to 15 V and 1.5 mA into the IGBT collector. During normal IGBT operation the collector–to–emitter on voltage will be less than 2.5 V and its on resistance less than .006 ohm. The comparator sense line tracks the IGBT collector–to–emitter on voltage with the isolation diode's forward 0.5 voltage added to the sense line voltage. The IGBT on voltage goes above 2.8 V when an overcurrent condition occurs, and the overcurrent comparator toggles since its reference voltage is 3.3 V. If a shorted load occurs, the IGBT on voltage goes above 6.2 V and the shorted–load comparator also toggles.

The comparator outputs are coupled to a dual one shot flip–flop IC. The overcurrent comparator output drives a CMOS one–shot flip–flop whose pulse width is 15 µs. The overcurrent flip–flop Q output is diode OR'd into the Fault optocoupler FET driver which shunts the optocoupler LED current to common, thereby switching off the Fault optocoupler; this allows its output to pull high for about 15 µs.

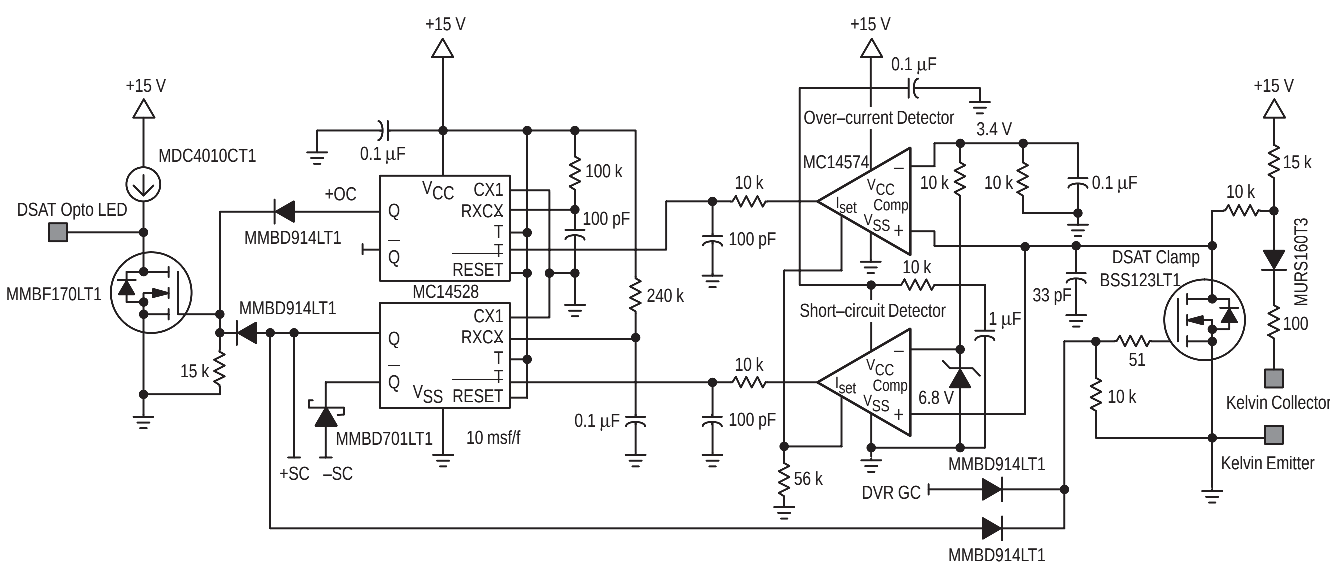

Figure 9–5. DSAT Overcurrent Detection and Shutdown Logic

The shorted load comparator output drives the other one shot flip–flop. The pulse width for this shorted load flip–flop is 10 ms. Both Q and Qbar outputs of this device are used. The Q output (+SC) drives four other elements: The Fault optocoupler FET driver which shunts the optocoupler LED current to common, an N FET that clamps the DSAT sense line to common, the pre–driver IC turn–off input, and the slow turn–off power N FET IGBT gate driver. The Qbar output (–SC) drives the pre–driver IC turn–on input low, which turns off the P FET IGBT gate driver.

When a shorted load happens several actions take place: The P FET turn–on driver FET is switched off, the normal turn–off N FET driver is held off, a power N FET turn–off with 10 ohm IGBT gate resistor is enabled, the DSAT sense line is clamped low, and the fault optocoupler output goes high. The one–shot disables the gate driver for 10 ms, even if the motor control logic signals remain steady. Small RC filters are used on the DSAT sense comparator inputs and the flip–flop inputs to minimize high frequency noise spikes from triggering the comparator or flip–flops. The time delay from a shorted load event to actual gate driver shutdown was noted to be about 4 µs.

The DSAT sense line is clamped low during the off time of the IGBT and during the switching transitions. The DSAT clamp is driven from the on–off optocoupler output. The off–to–on switching edge time relies upon the clamp FET's gate discharge time to delay the unclamping of the DSAT sense line until after the IGBT has switched on. The propagation delay of the comparator–to–predriver IC–to–FET driver chain insures that the DSAT line is clamped low, slightly before the IGBT actually switches off.

Temperature Sensor

Temperature monitoring of the module (Figure 9–6) is important because of the possible 1500 hundred watts power module heat dissipation. The module will fail in a few seconds if its heat management system deteriorates, even if the motor current is at nominal levels. A temperature sensor is used to monitor the baseplate temperature which tracks the IGBT die's junction temperature. Two digital outputs indicate ≥125 and ≥150°C baseplate temperatures. An analog output gives the temperature as a linear voltage. The two digital outputs indicate an abnormally high 125°C temperature condition and an impending failure 150°C condition. The system computer could also track the time from an 125 to 150°C event to determine the severity of heat rise per time of the temperature problem. The analog output allows the computer to calibrate the temperature sensor and then to track the temperature variations over time, which can predict how long the module can continue to operate until dangerous junction temperatures will occur.

Using a series string of silicon diodes for the temperature sensor element offers high sensitivity and lends itself for further integration. The ideal diode string would equal .01953 V per °C, which would correspond to one bit change for an 8 bit A/D converter. A MMAD1108 device, for example, is an 8 diode array in a SO–16 SMT package that could be attached by thermal epoxy near the hot spot or center of the power module. By wiring all eight diodes in series, and adjusting the diode string's forward current, a sensitivity of –.01953 V per °C can be obtained. The diode string's voltage will be about 4.0 V at 25°C, 5.562 V at –55°C and 1.558 V at +150°C. Since most MCU A/D ports run from 0 to 5 V, a level shifter is required. An op amp can level shift plus invert the diode string's voltage, thereby conditioning the sensor's voltage to match the A/D voltage range and giving a positive deviation for a temperature increase. The op amp's output can also be connected to comparators that use reference voltages set to correspond to the analog 125 and 150°C voltage levels. When these levels are reached, the comparator output toggles low, which can switch on simple LED indicators to warn of excessive temperature problems.

The initial breadboard circuit used a MMAD1108 device. Unfortunately, there is not enough room in the module to accommodate the device's large 10mm x 7mm footprint. A SOT–23 dual series diode, MMBD7000LT1, was therefore chosen for its small 2.8mm x 2.8mm footprint, which was epoxied onto the baseplate. The dual diode, however, only gives a sensitivity of about –.00453 V per °C. The prototype temperature sensing circuit, Figure 6, consists of a dual op amp, a dual comparator, and a 5 V regulator. The +12 V power bus feeds the 5 V regulator. A LM2931DT is used to regulate the 5 V supply for this circuit. The LM2931DT is rated for 125°C operation.

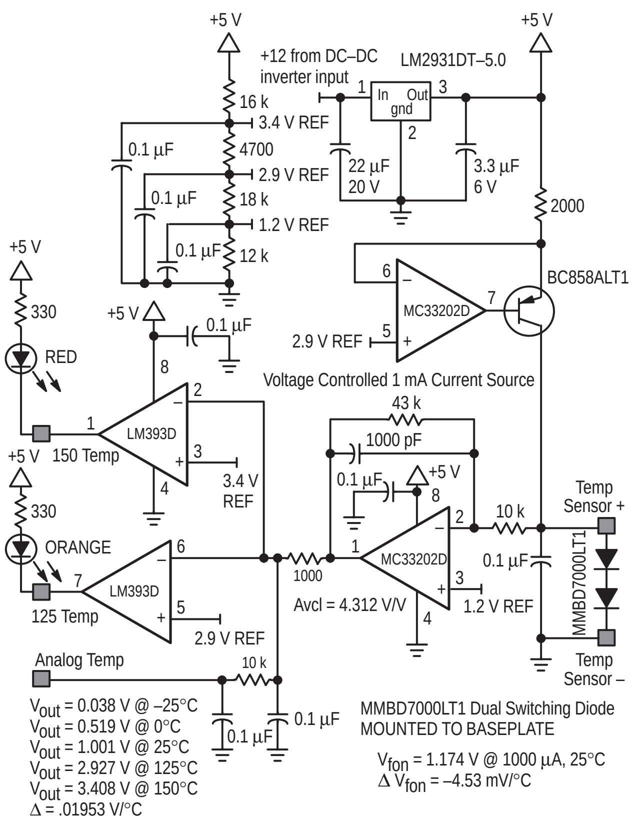

Figure 9–6. Temperature Detector Circuit uses a Dual Diode Sensor

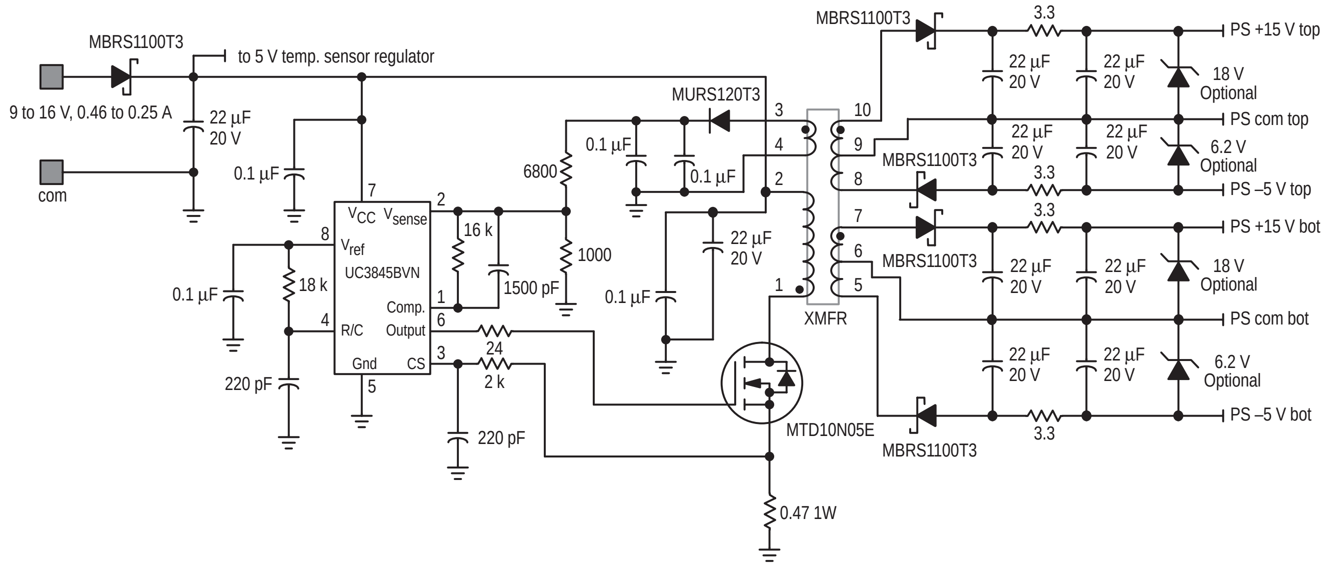

Figure 9–7. DC–DC Power Supply for 1/2 Bridge Control Circuit

A MC33202 dual op amp was chosen because its output can vary from 0.15 to 4.85 V. One op amp is used to provide an 1 mA constant current to the dual series diode. This insures higher accuracy from the dual series diode over a wide temperature range. The dual diode's forward on voltage will vary from about 1.45 V at –40°C to 0.59 V at +150°C. If a simple resistor is used to bias the dual diode, its current level would vary by about 17% over –40 to +150°C, which raises the diode's on voltage at higher temperature and causes an erroneous reduced temperature reading. An 1 mA constant current level was favored over an 100 µA level. The 1 mA level gives a lower impedance input to the second op amp and minimizes noise pickup from the power module's high energy levels. The second op amp is connected as an inverting amplifier with a V_{in}/V_{out} voltage gain of 4.3. A capacitor in the op amp's negative feedback loop limits the bandwidth to under 10 kHz. The amplifier's output drives the minus input lines of a LM393 dual linear IC comparator.

The comparator's positive inputs are tied to voltage references of about 2.9 and 3.4 V, which are the respective 125 and 150°C analog outputs. Each comparator output is an open collecttor type is normally off or pulled to about 3.5 V by an LED and series resistor that is connected between the output and +5 V. When the analog temperature voltage reaches ≥2.9 V, the comparator's output toggles low, switching on the LED. As the temperature voltage increases to ≥3.5 V, the second comparator output goes low and switches on its LED. Both comparator output lines are brought out as logic signals.

DC–DC Converter

The IGBT gate bias voltage and control signals require a high level of isolation from the control circuit and low voltage power source. The isolation is necessary for both safety and operational requirements. Generally, an isolation barrier of 2500 V will meet most regulatory standards. For stable operation the DC–DC converter as shown in Figure 9–7 should exhibit minimal input–to–output capacitance and perform reliably when subjected to voltage transients that approach 15,000 V per microsecond descriptions. The insulation between the windings provide the isolation and should be rated to withstand high voltage transients and elevated temperatures. The crucial operating requirements for the control power supply include:

- Input Voltage: 8 to 20 V (application specific)
- Output Voltage: 2x +15 and –5 V
- Output Power : 1 to 3 watts (ckt. off = 1W, ckt. on = 3W)
- Max. T_A: 125°C
- V_{isio}: 2500 V
- dv/dt: 15 kV/µs
- Size: Less than 2 cm cubic volume
- Regulation: Line and load 5%
- Efficiency: >80%

Other methods that could be used to supply isolated gate driver power include a "bootstrap" from the high side IGBT collector or a photo–voltaic device using a light source and solar cells. The "bootstrap" method was rejected mainly because the high voltage must be applied to activate the control circuit. This does not allow enough time for the gate driver circuits to stabilize and basic diagnostics to be performed before the high voltage is switched on. In a 100,000 watt control system the logic and interface circuits should always be first on and last off to insure reliable and safe operation. (Some systems actually lock out the high voltage until the control logic and power interface is stable.) The photo–voltaic might be practical if the gate driver power requirements could be significantly reduced. A solar cell is about 12% efficient; therefore, to supply about 2 watts to each gate driver would require employing a 16 watt light source.

A DC–DC converter based upon the flyback topology was chosen because it requires few components, while allowing for multiple positive and negative secondary windings. Voltage regulation can be accomplished from a separate transformer voltage feedback winding or from a optocoupler. Testing revealed that the transformer feedback winding method gives good line regulation and poor–to–fair load regulation. If the gate control circuits always draw a constant current, the load regulation requirement is diminished. An optocoupler voltage feedback approach is more expensive but will give better load regulation.

The DC–DC converter input voltage is usually derived from the same voltage source that feeds the system's microcontroller or digital logic voltage regulator. It is advantageous to use an input voltage to the DC–DC converter that is equal to or slightly higher than the gate voltage requirements or +15 V. Using an 15 to 20 V input instead of the 9 to 12 V input will improve the DC–DC converter's efficiency.

Some protection in the DC–DC converter's input line is necessary to help insure that this critical power source is stable during abnormal conditions. A series rectifier in the +12 V supply line protects against reverse voltages, and, with the addition of a large filter capacitance, smoothes out +12 V bus voltage transitions. The series rectifier prevents the capacitor from discharging back into the 12 V supply, thereby keeping the DC–DC converter operating during irregular power on–off–on sequences. A UC3845 current mode control IC was chosen for its high performance current mode capabilities. The standard 8 pin case 626 dual in–line package (DIP) was chosen over the SO–8 SMT package because of the 626's lower operating temperature. The DIP's $R_{\theta JA}$ is 100°C/W while the SO–8 is rated at 178°C/W. The UC3845 typically dissipates 0.15 watts, which gives a junction temperature rise of 15° for the 626 and 27° for the SO–8 packages. A 10 ampere 50 V power N FET is used to drive the transformer primary. One aspect of using the UC3845B is its internal 8.7 V shutdown mode. This limits the input voltage to about 9 V. The internal 8.7 V shutdown switches off the DC–DC converter before its regulation becomes marginal.

Testing showed that the DC–DC converter would engage at about 8.7 V and drop out at 8.2 V. The average current draw is .3 A at 12.0 V input with both channels driven. The current draw of either top or bottom +15 V rails is about .07 A each. The –5 V rails ran about .05 A each. The power in/out efficiency is about 70%. The total power consumed by the gate driver board is about 3 watts. The power consumption is affected most by the optocoupler LED requirements, IGBT gate capacitance, and IGBT switching frequency

Temperature testing of the prototype DC–DC converter components indicated that the transformer, power FET, source current sensing resistor, and UC3845 ran about 15°C above ambient. Momentarily shorting the +15 or –5 outputs did not cause the circuit to fail; the UC3845 went into a narrow duty cycle mode.

An optimal DC–DC converter for the module control circuits would be one that is assembled and tested as a separate unit. This will increase the final test yield of the control circuit board.

INTERNAL VS. EXTERNAL CONTROL PCB

There are definite advantages to locating the control circuits as close as possible to the IGBT power devices: Increased response times, thermal sensing, and short lead lengths. From a semiconductor manufacturing viewpoint, it is difficult to combine a multi–chip wire and die bond assembly with a printed circuit board attachment. However, for the power module user, interfacing from a microcomputer control system to high energy power modules can be simplified with the interface control circuits inside or attached directly to the module.

There are some module user disadvantages to consider when incorporating control circuits inside the power module. The module manufacturing costs will be higher than a standard module and external control PCB. This is partly due to the fact that completed modules that fail final testing are not repairable. Another disadvantage is that some applications may operate beyond the control circuit's design parameters [5]. The internal circuit values cannot be adjusted to perfectly match the application.

The concept illustrated in Figure 9–8 is another method to moderately simplify the user interface to the power module. The idea would be to construct a standard power module in a fashion that would accept a plug in PCB or interface module. The interface module would then be designed to match the power module's parametrics and allow some user adjustments to match the specific application. The interface module's physical layout could be designed to allow a complementary mechanical match to the power module. A mechanical latch would snap in place when the interface module is plugged into the power module.

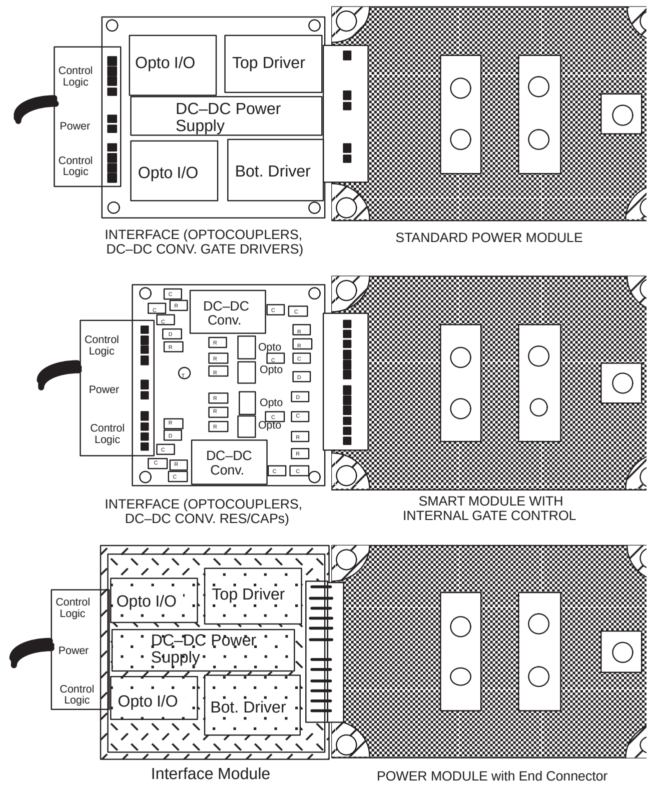

Figure 9–8. Power Module Circuit Attachment Options. Note how the smart module still requires an interface circuit board.

CONCLUSION

The control circuitry could be improved upon by a gate driver IC, which would integrate the current sensing amplifiers and logic, undervoltage detection, +15 and –5 V gate drive operation, temperature detection, and a coded fault output signal.

Optocoupler coupler devices need to be designed specifically for internal power module operation. They should include a built–in logic level input, a push–pull or totem pole output, and matched positive and negative switching times of under 1 microsecond. An optocoupler with an open collector exhibits a high off state output impedance, which makes the output line more sensitive to induced or capacitance coupled noise, generated by the high Di/Dt and Dv/Dt values from the power IGBT stages.

The temperature sensor function could be integrated into one stand–alone IC with either internal or external diode strings or integrated into the gate driver IC.

The cost penalty of embedding a complex printed circuit board in the power module is difficult to justify in high volume production. If the control circuits unconditionally need to be in the power module, the control circuit devices should be further integrated and directly attached to the power substrate. This eliminates the internal printed circuit board and its associated drawbacks. Including some type of user programmable functions such as current limit trip–points and shutdown time selection would allow the user to match the module to each application.

Adding a fast and precision isolated current sensor into the module's phase output line would eliminate the need for expensive external motor current sensors.

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[4] R. Chokhawala, J. Catt, L. Kiraly, "A Discussion on IGBT Short Circuit Behavior and Fault Protection Schemes", International Rectifier, TPAP–3, 1993

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Section 10
Cost Effective Power Package Handles Up to 3 HP Motor Drives

VersaPower™

Born out of the challenge to provide a cost effective power package solution for fractional to 3 hp motor drives, Motorola's new VersaPower™ package promises to go several steps further, providing electronic power designers a low cost platform core, capable of offering a wide range of standard and custom silicon power topologies across a series of consistent, standardized sizes.

Nobody yet knows the "best" way to make a 1 hp electronic motor drive. While the expectations of the users is that a 1 hp drive should cost perhaps a third of a 3 hp drive, the manufacturer is faced with the reality that most of the expense, such as the microprocessor and control electronics, display and keypad, internal power supply, housing, etc., remain virtually the same. This often puts the drive manufacturer in the position of accepting relativity poor profit margins at this low end.

There is an enormous amount of pressure on the drive designer to "fix this". One area that has been closely scrutinized is the power silicon. While the higher power drives have long been the domain of power modules the 1 hp drive manufacturers have customarily focused on the discrete approach, commonly employing herds of TO–220 and axial leaded parts to fabricate the 3–phase inverter and input rectifier circuits.

Economies of scale and volume have endowed discrete parts with a price advantage when directly compared, silicon for silicon, with power modules. However, direct price comparisons often ignore or disregard the thermal, electrical, mechanical and assembly advantages of the module approach.

There are a number of challenges confronting the drive designer who chooses to go the discrete route:

- In 460 VAC drives it can prove to be difficult or even impossible to meet UL spacing requirements when using unpotted discretes.
- Since the next larger die often requires a significantly different discrete package there is usually little room for growth of the drive without substantial redesign.
- The majority of discrete parts are non–isolated, imposing additional heatsink isolation burdens.
- The discrete drive designer must pay close attention to thermal control. Bolting multiple non–isolated parts to a common heatsink can prove to be mechanically difficult and costly in both hardware and assembly time. In general, discrete parts require mechanical support, modules provide them.

Recently there has been considerable excitement in the "roll your own" approach of putting large surface mount discretes on various insulated aluminum or copper "clad" materials. This is a workable solution, but it should be recognized that this adds an additional level of manufacturing burden upon the drive maker, in effect, putting the drive company into the power module business.

At Motorola it was felt that there was no reason for our drive customers to be carrying this burden. We believed that we could develop a simple and easy to use power package which could compete directly, in final value for value, with the discrete approach and still provide ample expansion up the power curve. This paper is about the resulting package which we call VersaPower.

Package Design

The new Motorola VersaPower™ module is a low profile, low part count, low to medium current, flexible power module. It consists of a thermally conductive and electrically isolated base plate, a thermo–plastic housing with molded in leads and a protective cover. It has dual in–line leads for easy mounting to a PCB (Printed Circuit Board) with a uniform pin to pin pitch of 0.250″ (6.35 mm).

The key element of the construction of the VersaPower™ module is the flexibility of using an IMS baseplate. This substrate provides the same flexibility of design as a single side PCB but with much improved thermal transfer. IMS constructed modules have been in use for over 10 years and are a proven technology.

The structure of the IMS is a stack–up of a metal base plate with an insulating dielectric layer laminated on one side and a copper foil on top of that. The base plate for the IMS can be aluminum, copper, steel or a composite such as Copper/Invar/Copper. The dielectric layer is created by two or more layers of an electrically insulating and thermally conductive loaded polymer. The copper foil side, consisting of up to 4 ounce copper, is etched to form the circuit.

The most common base plate material and the one used in the VersaPower™ module, is aluminum. The standard base plate thickness are 0.040, 0.060, 0.080 and 0.125 inches. The VersaPower modules use 0.080 aluminum for good heat sinking capability and adequate stiffness to maintain base plate flatness for assured heat transfer to a heatsink.

The dielectric layer provides the high voltage isolation between the copper traces of the circuit and the base plate. The polymer layer of the IMS is supplied in thicknesses between 0.003 and 0.006 inches depending on the isolation voltage required. Although the polymer layer is heavily loaded for good thermal transfer the polymer layer causes the greatest thermal resistance. Therefore a thin layer is desirable. The VersaPower™ module isolation layer is between 0.003 and 0.004 inches and is guaranteed to meet a minimum 2500 volt isolation requirement.

The copper foil layer of the IMS contributes the flexibility of the VersaPower™ module. It can be etched into many different circuit patterns. The semiconductor chips can be mounted directly to the copper foil or where more heat spreading or thermal capacity is needed the silicon can be mounted on a heatspreader. The copper layer is produced in common PCB thicknesses such as 1 to 4 ounces depending on the current handling capacity needed for the module. Because the IMS has much greater thermal transfer capacity than a standard fiber glass PCB the same size copper trace on the VersaPower module will carry current with greater efficiency than on an FR4 board.

The leads are molded into the housing to provide ease of assembly and to keep the piece part count to a minimum. Except for the number, the leads are the same for all VersaPower™ packages, maintaining the same height and spacing on all modules in the family.

The plastic housing size may change without the additional cost of tooling a new leadframe. Provision was made to trim the leadframe to different lengths depending on the number of pins needed for the package. Leads are plated with a solderable metal and do not need to be solder dipped prior to assembly.

The housing has molded stand–offs to maintain a consistent height when soldering to a PCB. The standoff are designed to accept self tapping screws so the module may be solidly attached to the PCB prior to soldering if desired.

The final design is both conducive to high volume assembly and flexible towards changes in internal topography. The first release is a family of 5 IGBT/Diode 6–packs covering 1 to 3 hp, 230 and 460 VAC induction motor drives in a 16 pin package. 20 and 24 pin packages are being introduced. Figures 10–1 through 10–4 illustrates some configurations to come.

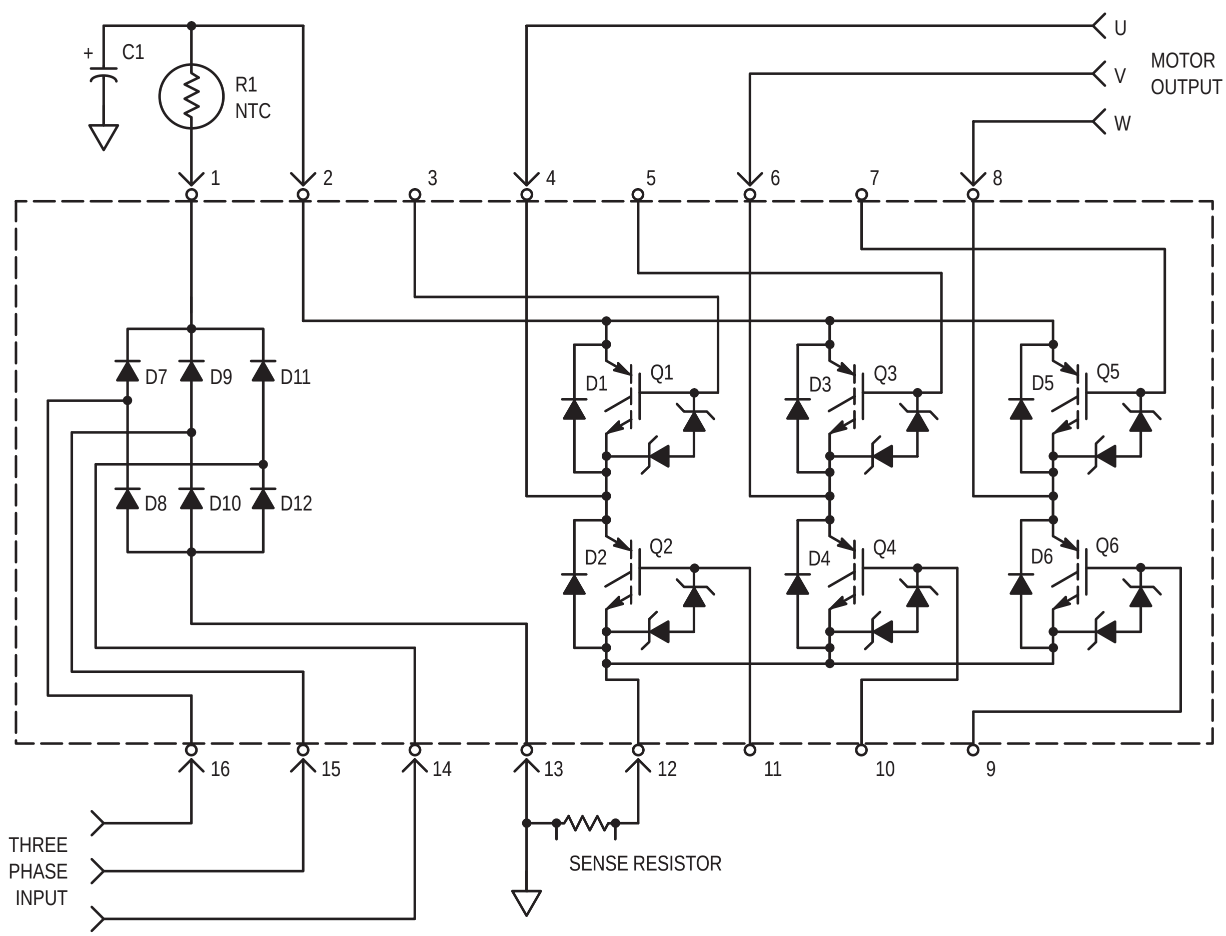

Figure 10–1. 16 Pin VersaPower™ Three Phase Input and 6–Pack

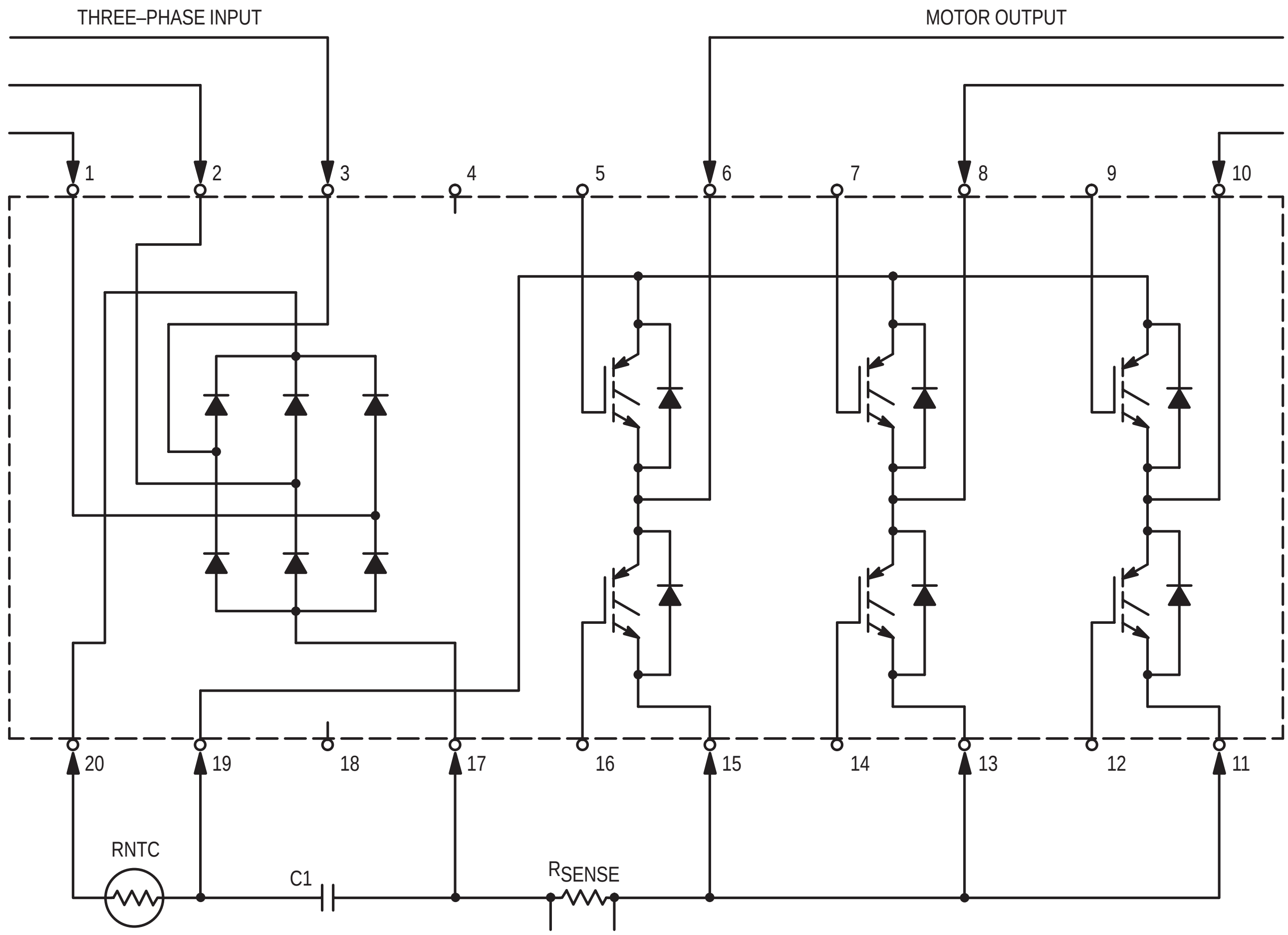

Figure 10–2. 20 Pin VersaPower™ with a 3 Phase Input Bridge and 6–Pack Output

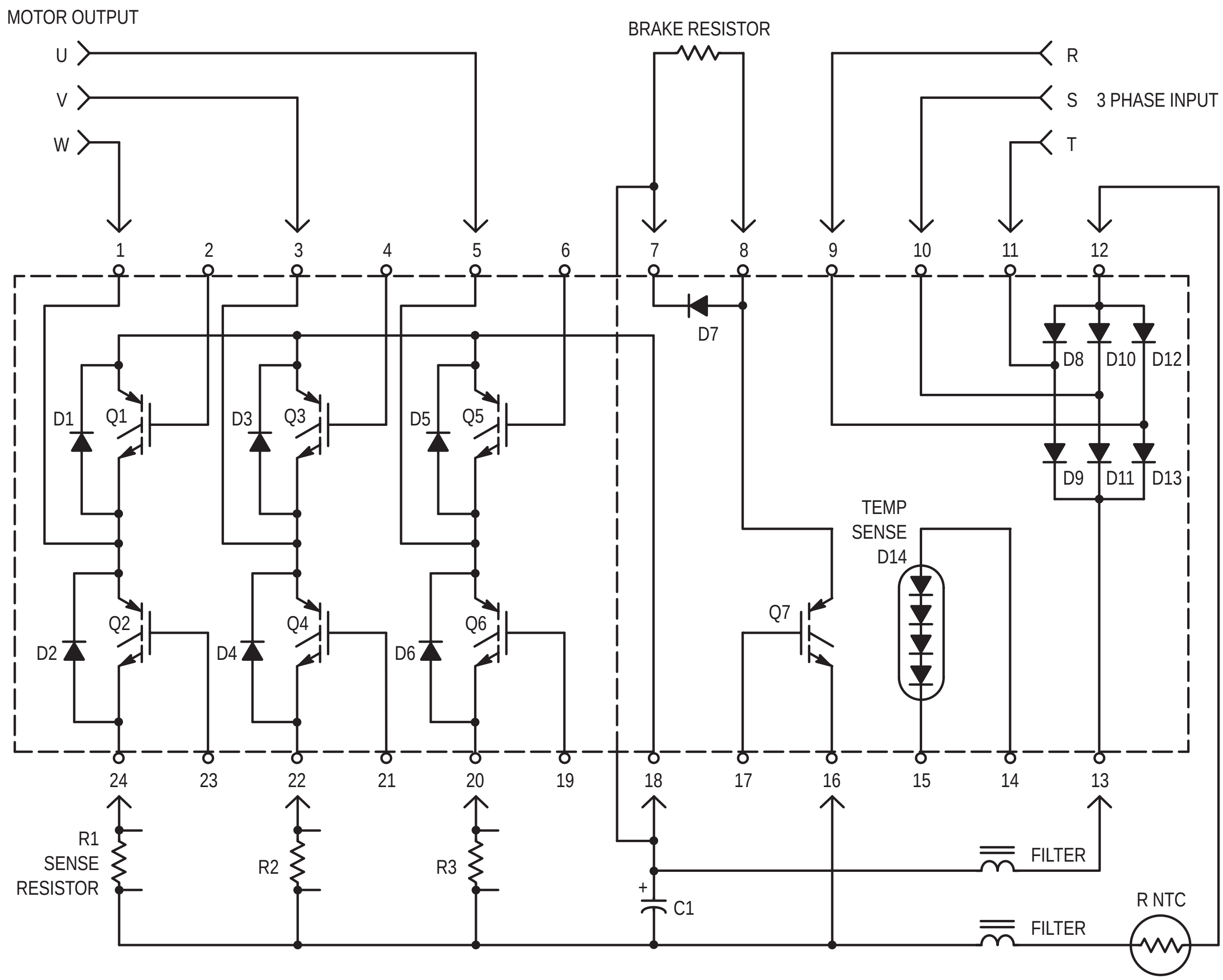

Figure 10–3. 24 Pin VersaPower™ IPS with Brake & Temp Sense

CONCLUSION

The original premise was to provide a low end module for motor drives which could match or better the system costs of the discrete approach while providing room for future growth. The resulting VersaPower™ module meets that goal while showing additional promise as a standard platform for non–motor power applications.

Figure 10–4. 16, 20 and 24 Pin VersaPower™ Packages

Temperature Sense for Less

Many power circuits, particularly inverters used for motor control, require temperature sensing of the power devices for reliability. This information can be used to shut down the system in the event of overheating. Also, some applications require special operation at very low temperatures. A variety of methods have been used for temperature sensing, including special integrated circuits, thermocouples and thermistors. Most power products require external temperature sensing, on the case or on the heat sink. Motorola has developed a reliable, low–cost solution for sensing the internal temperature of our hybrid power modules.

The basic premise is simple: the voltage across a diode biased at a fixed current has a nearly constant temperature coefficient. Voltage references are available with temperature coefficients approaching zero. A differential amplifier can be arranged to measure the difference between the reference and the voltage across a diode, which should result in a linear temperature indicator. A schematic is shown in Figure 10–5. The diode is placed on the same substrate as the power circuit, while the voltage reference and amplifier are located on the control PCB, external to the module.

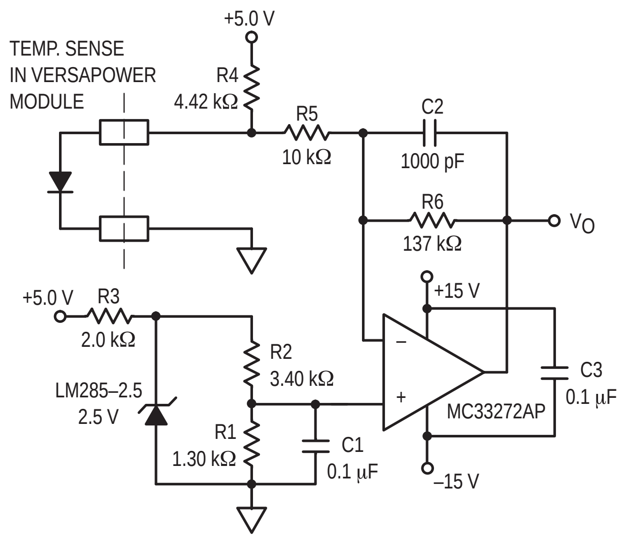

Figure 10–5. Temperature Sense Circuit

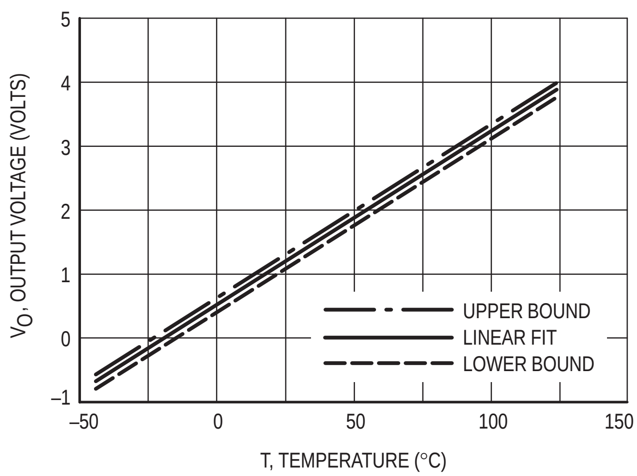

Figure 10–6. Linear Fit for Temperature Sense

Experimentation has shown excellent linearity of the output voltage V_O with respect to temperature T. Results, a linear fit, and error bounds are shown in Figure 10–6. A 99.5% confidence interval indicates a prediction error of ±5°C over a range from –40°C to +125°C, generally adequate for setting trip points. In addition, improved accuracy may be gained by calibrating the circuit at one or two temperatures. One observation increases accuracy to ±3°C, while two observations increases accuracy to ±0.75°C. This can be a software calibration, updating a line fit or look–up table. Most applications do not require such high accuracy, so the general fit can be used directly.

Cost is greatly reduced using this system. The actual temperature sensor is a low–cost device internal to the hybrid power module. In many cases, the op amp is “free,” an extra op amp in either a dual or quad op amp I_C being used for other functions in the system. The voltage reference could be used for other functions, such as A/D referencing or power supply control. No additional steps are required in assembling the system to mount a sensor to the module or heat sink.

Getting the Amps Out

The VersaPower™ package has been designed to interface directly to printed circuit boards. This works particularly well in applications up to and including 3 hp. One advantage of using this power module, rather than discretes, is that only slight modifications of the PCB layout are necessary to extend the range up to 5 hp. At increased current levels, particular attention must be paid to appropriate trace design on the PCB. This article shows some techniques for designing up to 25 A traces while meeting minimum spacing requirements.

To avoid arcing or breakdown between traces, as well as to meet certain regulatory approvals, conductors at different voltage levels must follow minimum spacing rules, determined by the voltage differential expected. The tables below show spacing for motor drives that derive their DC bus from rectified 230 VAC or 460 VAC three–phase power lines. Separate columns indicate different spacing for potted PCB or standard FR–4 PCB.

Any PCB designed to use the VersaPower™ must also obey these design rules, placing a constraint on the arrangement of wide conductors. To achieve the flexibility of using a single layout for high and low voltage modules requires the use of 460 VAC spacing for all boards.

The picture below shows several different widths and shapes for 25 A traces. The 680 VDC spacing rules from the accompanying table were followed. Some solutions for maintaining spacing include removing a semicircular portion of the power trace near a high–voltage pin, narrowing the trace near the pins, or even routing a slot in the board to increase “over–the–board” distance. The particular board shown in the picture uses 3 oz. copper foils on both sides of the board-effectively two thick traces in parallel. For a 25°C rise at 25 A, 0.320″ wide traces are necessary. Many of the traces in this design also extend well past the pin of the power module, creating a small heat sink for the trace.

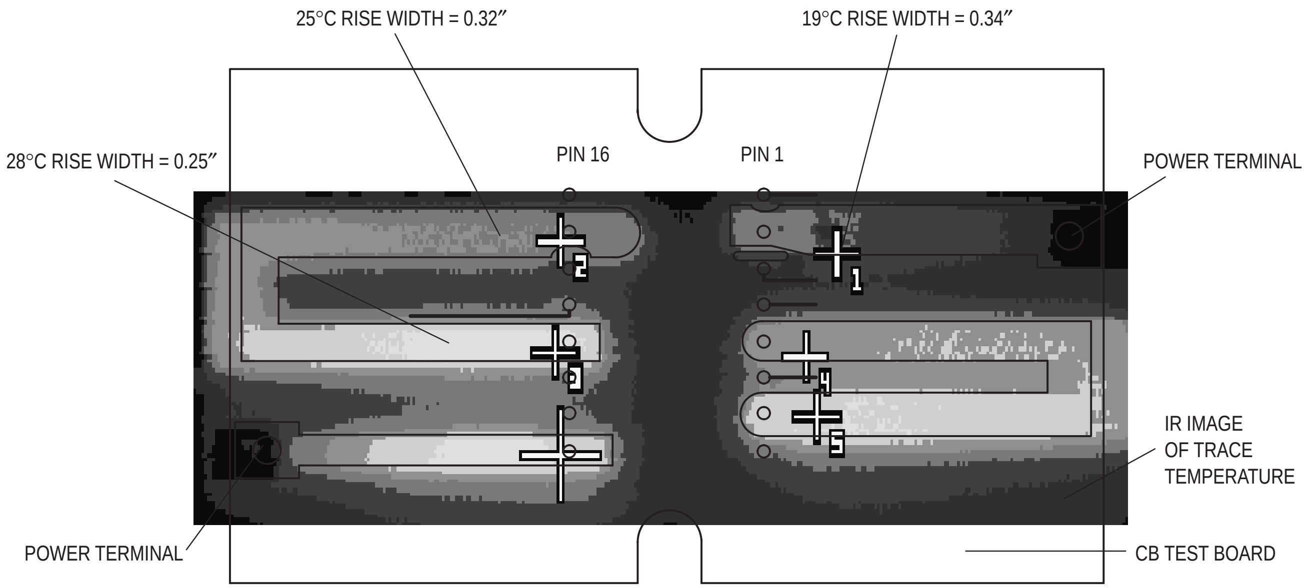

Figure 10–7. Two Sided, 3 oz. Copper at 25 A VersaPower™ Package Pin Footprint

Table 1. 230 VAC Spacing Design Rules

Spacing (in.)	Nominal Voltage	Potted P.C. Board Creepage [1] (in.)	P.C. Board Creepage [2] (in.)
Bus to Bus, Brake to Bus	340 VDC	0.035	0.070
Input to Output	280 VAC	0.025	0.050
Line to Line	240 VAC	0.025	0.040
Bus or Brake to Line or Ground	170 VDC	0.015	0.020
Line to Ground	140 VAC	0.010	0.015

Table 2. 460 VAC Spacing Design Rules

Spacing (in.)	Nominal Voltage	Potted P.C. Board Creepage [1] (in.)	P.C. Board Creepage [2] (in.)
Bus to Bus, Brake to Bus	680 VDC	0.080	0.135
Input to Output	560 VAC	0.060	0.115
Line to Line	480 VAC	0.050	0.095
Bus or Brake to Line or Ground	340 VDC	0.035	0.070
Line to Ground	280 VAC	0.025	0.050

NOTES:
IEC664A Table 4, PCBs, Pollution Degree 1
UL840 Table 6.2, Pollution Degree 1
IEC664A Table 4, PCBs, Pollution Degree 2
UL840 Table 6.2, Pollution Degree 2

The various shapes show what is achievable using standard PCB techniques. Clearly, a current rating of 25 A is at the upper limits of production boards. This shows, though, that 5 hp drives are feasible using VersaPower™ and appropriate PCBs. Lower power drives can similarly benefit from the same techniques; wide traces, heat sinking tabs, narrowing where necessary for voltage clearance, and so forth.

Table 3, taken from NEC Table 430–150, shows typical phase current ratings for continuous operation. Taking PCB layout to extremes allows the design of up to 10 hp 460 VAC drives using a VersaPower™ module. Moderate application of these ideas still can achieve up to 3 hp 230 VAC or 5 hp 460 VAC drives with headroom for overload conditions.

Table 3. Typical Phase Current Ratings for Continuous Motor Operation

HP	200 VAC (A)	230 VAC (A)	460 VAC (A)
3/4	3.7	3.2	1.6
1	4.8	4.2	2.1
1–1/2	6.9	6.0	3.0
2	7.8	6.8	3.4
3	11.0	9.6	4.8
5	17.5	15.2	7.6

The VersaPower™ package simplifies design of low–cost, low–power motor drives. In addition, with close attention to PCB layout, somewhat higher power levels are achievable. This represents a clear advantage over discretes and enables the rapid design of advanced power circuits.

Section 11
IGBTs Integrate Protection for Distributorless Ignition Systems

INTRODUCTION

A specially designed IGBT provides the desired characteristics for the next generations of distributorless ignition systems for automobiles.

To meet tighter emission standards, auto designers are now pursuing a distributorless approach to ignition for many future vehicles. In engine control systems like the one shown in Figure 11–1, the ignition driver interrupts the current to a coil that fires two plugs simultaneously or a separate coil that is used for each spark–plug. One single power device was used in breakerless ignition systems, but distributorless, or direct fire, systems use one for every cylinder, or at least one for every two cylinders!

A number of improved semiconductor processes have been developed since bipolar Darlington transistors were first used for ignition systems. These include power MOSFETs, IGBTs and even smart power ICs that combine power devices with bipolar and/or CMOS circuits to provide sophisticated control capability. Although ignition system designers would like to integrate all of the desired functions of the ignition power switch into one semiconductor device for improved reliability, reduced size and number of components, the cost of a component made with today's more complex smart power processes can be prohibitively high. Furthermore, the performance and reliability may not meet automotive requirements. An alternative is to use the most area efficient silicon power switch with the additional protection that can be obtained from a standard semiconductor process and a separate control IC to obtain the "smarts."

In the ignition voltage range, approximately 400 V, IGBTs are proving to be more cost effective than bipolar power transistors. Furthermore, several active and passive devices can be obtained from a standard power IGBT process that allow simple circuits that provide protection for the basic power device. The circuits that can be integrated are very simple but only require a small increase in the area to the basic power IGBT and the addition of only one masking layer to the process. Therefore, the cost impact of these circuits is only a small fraction of the total cost of the power switching device. However, the functions that can be obtained provide significant improvement in ruggedness, reliability, protection and ignition system cost reduction.

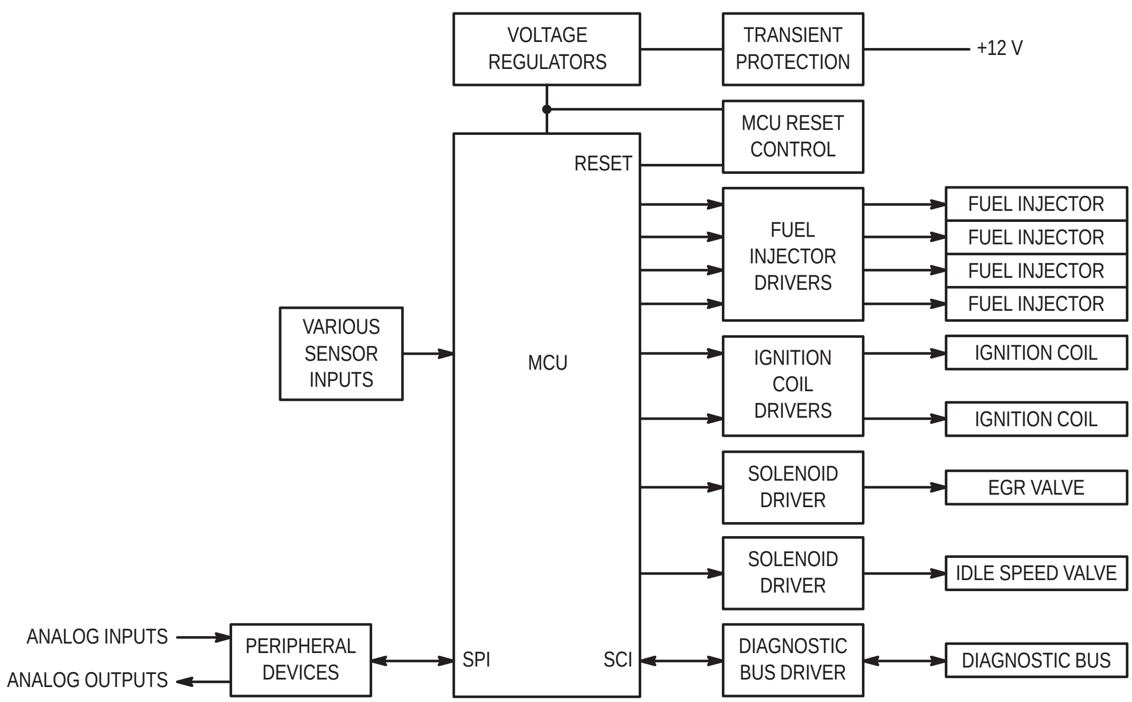

Figure 11–1. MCU–Controlled Direct Fire Ignition System

The small signal devices that are available in the standard power IGBT process have been utilized to achieve lower cost, protected power devices [1, 2]. A summary of these devices is shown in Table 1. These structures take advantage of the diffusions that are available in a standard double diffused vertical MOS process used to fabricate IGBTs. One processing step, an extra photoresist mask, has been added to obtain the polysilicon diodes.

Table 1. Device Performance Characteristics

Structure	Device	Description	Breakdown Voltage
Vertical	N–Ch	IGBT	500 Volts
–	Diode	Polysilicon	7–8 Volts
–	Diode	Back–Back Poly	7–8 Volts
–	Zener	Diffused	7–8 Volts
–	Resistor	Metal	–
–	Resistor	High To Poly	–
–	Resistor	Low To Poly	–

The differentiating factor between the SMARTDISCRETES™ process (Motorola's term for this approach) and an IC process is the lack of isolation between circuit elements — except for the oxide isolated diodes. This allows the process to be much simpler and lower cost than a power IC or smart power process, but also limits the circuits that can be obtained.

PUT A CLAMP ON IT

Figure 11–2 shows a high voltage ignition coil driver with an integrally clamped IGBT that has been specifically designed for automotive applications. The clamped IGBT utilizes polysilicon diode technology to offer a robust new alternative for ignition coil drive. The IGBT is more area–efficient than a power MOSFET or bipolar power transistor in the voltage range required for automotive ignition systems. As shown in Figure 11–3, the saturation voltage of a die that fits in a TO–220 package is approximately 1.4 V with 10 A and 4 V applied to the gate. The integrated logic level unit can be driven directly by a microcontrol unit (MCU) and turned on with as little as 3 V. Improved processing allows a high latch current (>60 A, pulsed) to be achieved even at temperatures of 175°C. A number of other features have been incorporated in the design that are important to automotive ignition applications.

The thin gate oxide layer in logic level devices can be easily damaged by ESD that can occur during the user's assembly process or in the application. The gate–emitter is also the lowest breakdown voltage for the IGBT and also the most likely candidate for damage due to electrical overstress (EOS) in an application that can experience transients that greatly exceed the normal supply voltage.

The ignition IGBT incorporates polysilicon diode gate–to–emitter ESD protection. These back–to–back diodes begin to avalanche at ±13 V. Figure 11–4 illustrates their response over temperature. A typical logic level device of this size would fail at about 1 kV. The ESD–protected ignition IGBT is rated to survive a minimum of 3.5 kV in the human body model.

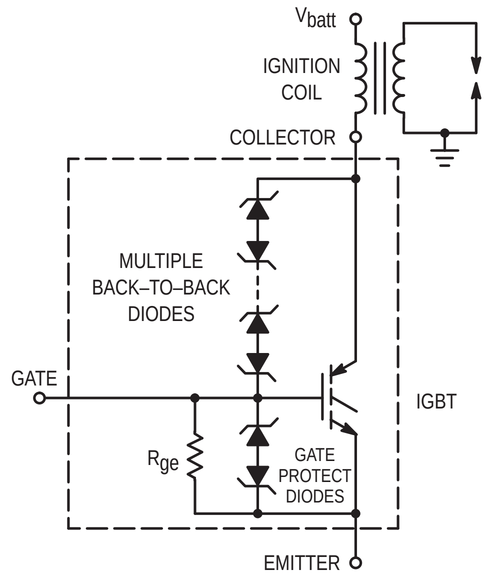

Figure 11–2. IGBT with Integral Collector–Gate and Gate–Emitter Clamps in an Ignition Circuit

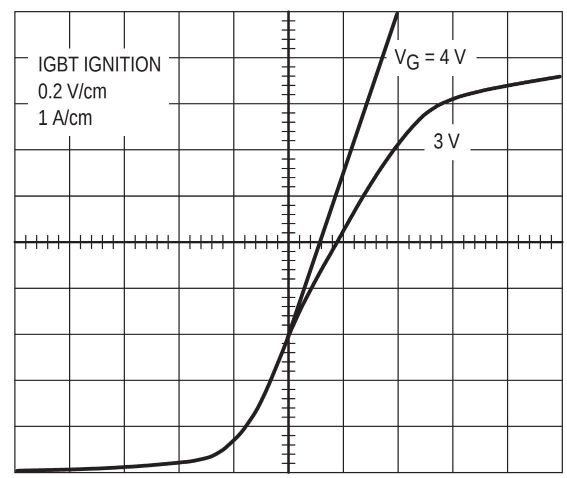

Figure 11–3. IGBT Saturation Voltage

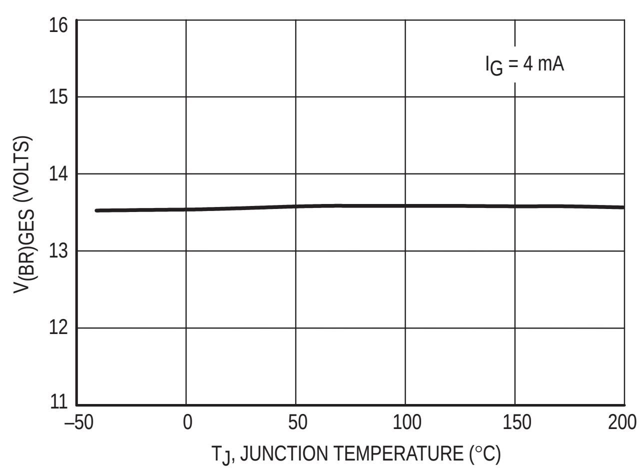

Figure 11–4. Polysilicon Diodes Response Over Automotive Temperature Range

The back–to–back diode structure used to protect the gate–to–emitter oxide is also used to achieve an active collector–to–gate clamp. To achieve higher voltage capability, a string of back–to–back polysilicon diodes is used. The back–to–back configuration provides a temperature compensated clamp because the forward drop of one diode decreases with temperature while the reverse drop of the other diode increases with temperature. The resulting clamped voltage is not sensitive to epi resistivity, epi thickness or temperature. All of these parameters cause the voltage to vary in standard IGBT designs. For example, the voltage changes on a given unclamped device from 0.95 to 1.12 times the 25°C value over the temperature range of –40 to 150°C.

A string of back–to–back polysilicon diodes from collector–to–gate of the ignition IGBT offers two attributes to the automotive system designer: almost no variation of device breakdown over temperature and excellent energy dissipation capability. The string of back–to–back polysilicon diodes has been integrated into the IGBT structure that provides a high voltage clamp that can be precisely controlled with a typical variation of only 10 V over an automotive temperature range of –40 to 175°C.

The avalanche voltage of the drain–to–gate clamp is designed to be less than the breakdown voltage of the IGBT. When the drain–to–source voltage exceeds the avalanche voltage of the collector–to–gate zener, the power device turns on and conducts virtually all of the current allowing the collector–to–gate elements to be very small. The small variation of a nominal 350 V and 400 V clamp over temperature is shown in Figure 11–5. Figure 11–6 displays clamp voltage as a function of diode current. Diode current may be controlled by the system designer by adding external series gate resistance. Recommended values are in the 300 to 1000 Ω range.

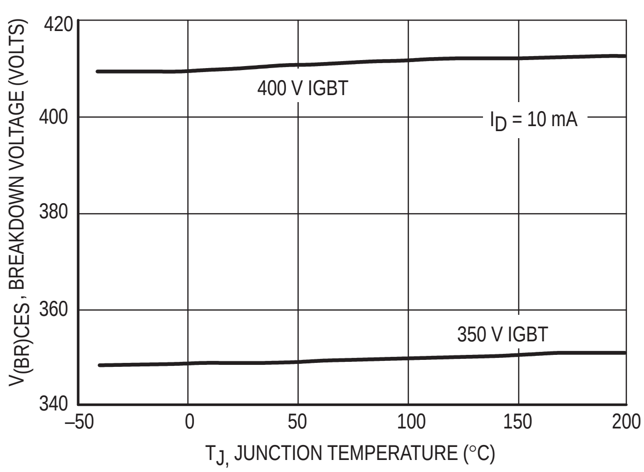

Figure 11–5. Clamped IGBT Voltage Variation Over Temperature

Excellent energy robustness of the ignition IGBT is a result of operating the device in the forward mode rather than an avalanche mode while clamping. The typical single pulse unclamped inductive switching (UIS) performance of the ignition IGBT is 950 mJ and a minimum rating of 550 mJ at a starting T_J of 25°C is guaranteed. This is well above the 170 mJ typically observed at 10 A with ignition coils during an open secondary fault condition. Figure 11–7 illustrates the typical single pulse UIS performance of the ignition IGBT over temperature.

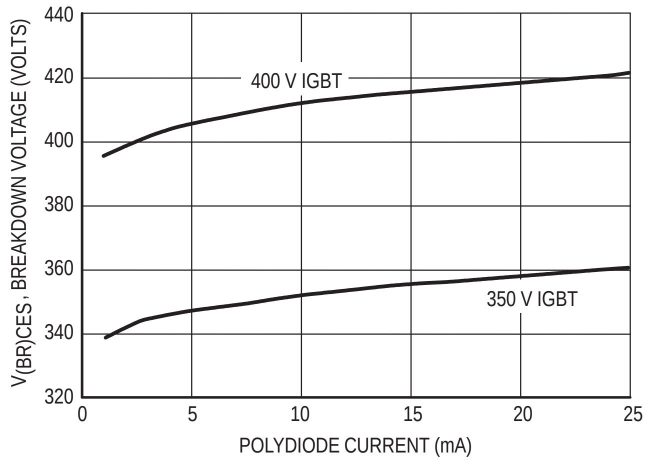

Figure 11–6. Clamped IGBT Voltage Variation With Current

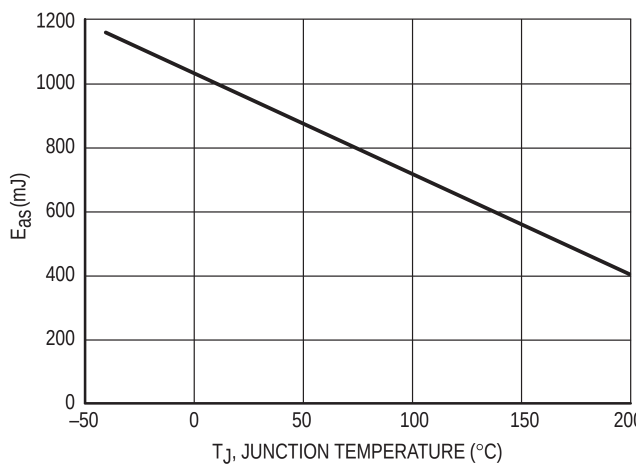

Figure 11–7. Energy Rating versus Temperature

The ignition IGBT also features a 40 V typical emitter–to–collector breakdown. This junction is capable of blocking and surviving a double reverse battery fault condition. The reverse collector current is rated at 12 A for pulse widths less than 100 μs, enabling the device to easily clamp open secondary negative transients.

PACKAGING

Another change occurring in automotive electronics is the transition to surface mount technology. The ignition IGBT is offered in a surface mount package, the D^2PAK, as well as the industry standard TO–220. The area–efficient IGBT structure allows the die to fit inside the smaller TO–220 package and minimizes the heat sink space, or printed circuit board space for the surface mount version, required inside a control unit module. Two levels of clamp voltage are available: 350 V and 400 V. Clamp voltage variations are achieved by adding or subtracting polysilicon diodes. This means the devices in Table 2 share identical characteristics except clamping voltage and package–related thermal properties.

Table 2. Energy Rating versus Temperature

Clamp ($V_{(BR)CES}$	Package	
	TO–220	D^2PAK
350 V	MGP20N35CL	MGB20N35CL
400 V	MGP20N40CL	MGB20N40CL
P_D (Watts)	150	150
$V_{CE(on)}$	<1.8 V	<1.8 V

Parameter extractions have been performed on the IGBT by Alliance Technology and used in a model developed by Alan Hefner of NIST (National Institute of Standards and Testing). Besides excellent simulation of DC performance, resistive and inductive switching characteristics, a complete in–vehicle ignition simulation has been demonstrated on Analogy's Saber simulator [3]. A distributorless ignition system with dual sparkplugs being fired by the ignition IGBT was used for the vehicle simulation. The tests included normal operation and operating extremes of low supply voltage and open secondary. The simulation was based on the interaction of behavioral models of the battery, starter motor, crankshaft speed, ignition coil, spark plug, spark plug wires and the IGBT.

This ignition device is just one of a few of the possible combinations of the components that can be obtained from a standard power IGBT process. The polysilicon diodes have also been used to provide a linear temperature sensor and the cellular structure of the IGBT allows a number of cells to be isolated and used for lossless current sensing. The circuit designs that are possible are also very simple, so the design time required for new products is minimal. This is an added advantage for custom devices that must be developed with severe program timing constraints. The ease in obtaining design changes combined with a developed IGBT model and simulation tools provide the capability to verify proper performance even under worst case operating conditions and to significantly reduce design cycle time.

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[1] Steve P. Robb, Judith L. Sutor and Lewis E. Terry, "SMARTDISCRETES™–a New Trend in Power Transistors," Proceedings of the ECS Symposium on Smart Power and High Voltage Devices, Spring 1989 Meeting.

[2] Steve P. Robb, Judith L. Sutor and Lewis E. Terry, "SMARTDISCRETES™, New Products for Automotive Applications," IEEE Workshop on Automotive Power Electronics, August, 1989.

[3] J. Mike Donnelly and Kim Gauen, "New IGBTs and Simulation Models Simplify Automotive Ignition System Design," IEEE PESC, Seattle, WA, June 21–24, 1993.

Section 12
Reduce Compact Fluorescent Cost with Motorola's PowerLux™ IGBT

INTRODUCTION

Compact Fluorescent Lamps (CFL) are becoming more and more popular in the consumer market because they bring a significant energy savings when compared to the incandescent bulbs they are intended to replace. As a consequence, the today's focus is to cut the costs and miniaturize the electronic circuits associated with these low pressure lamps, which makes them more affordable to the consumer.

Although there are many solutions for driving fluorescent lamps, almost all the electronic ballast's for CFLs use the half bridge topology described in this paper.

CIRCUIT ANALYSIS

The CFL application can be split in two main types of products:

a – The disposable one: the attached electronic circuit is thrown away when the lamp wears out.

b – The replaceable one: a new lamp is plugged into a socket (which contains the electronic circuit), making the expected life many times longer.

The benefits and consequences of each solution is as follows:

1 – Disposable CFLs are cheaper to manufacture, but as the lamp and circuit are both replaced, turn out to be more expensive in the long term. The expected life time is 8000 hours for European models and about 10000 hours for those built for North America.

2 – Replaceable CFLs require a more rugged electronic circuit, to survive the expected longer life time and the hazards that may occur when re–lamping the module. They are more expensive to build, but can be more cost effective in the long term. The expected life time should be at least 32000 hours to make these lamps competitive when compared to the disposable alternative.

Table 1. Comparison of Topologies

	BVCES	PEAK CURRENT	COMPLEXITY	COST	DIMMING	CONCEPT
FLYBACK	1200 V	400 mA	HIGH	MEDIUM	FEASIBLE	PARALLEL RESONNANT
PUSH–PULL	1600 V	400 mA	MEDIUM	MEDIUM	DIFFICULT	PARALLEL RESONNANT, CURRENT FED
HALF BRIDGE	700 V	350 mA	LOW	LOW	EASY	SERIES RESONNANT, VOLTAGE FED

NOTES: * All Values Assume Disposable CFL Module, P_{out} = 20 W, V_{line} = 230 V.
* Costs are Defined as Global for a Fully Assembled CFL.
* FLYBACK = Single Power Switch.
* PUSH–PULL and HALF BRIDGE = Dual Power Switches.

In both cases (disposable or replaceable), the ballast circuit can be designed with one of the topologies given in Table 1, keeping in mind that the single switch FLYBACK is not necessarily cheaper than a two switch alternative.

The circuit we'll describe throughout this paper is based on the HALF BRIDGE topology, operating from the 230 V line.

The basic circuits given in Figures 12–1 and 12–2 show the two alternatives: self oscillant or driven by a specific controller.

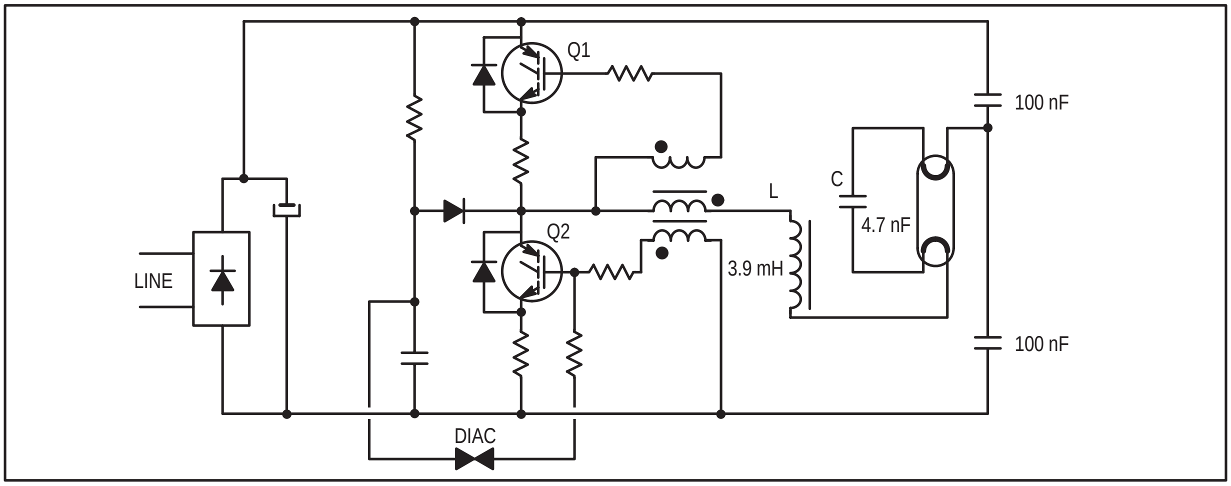


Figure 12–1. Basic Self Oscillant CFL

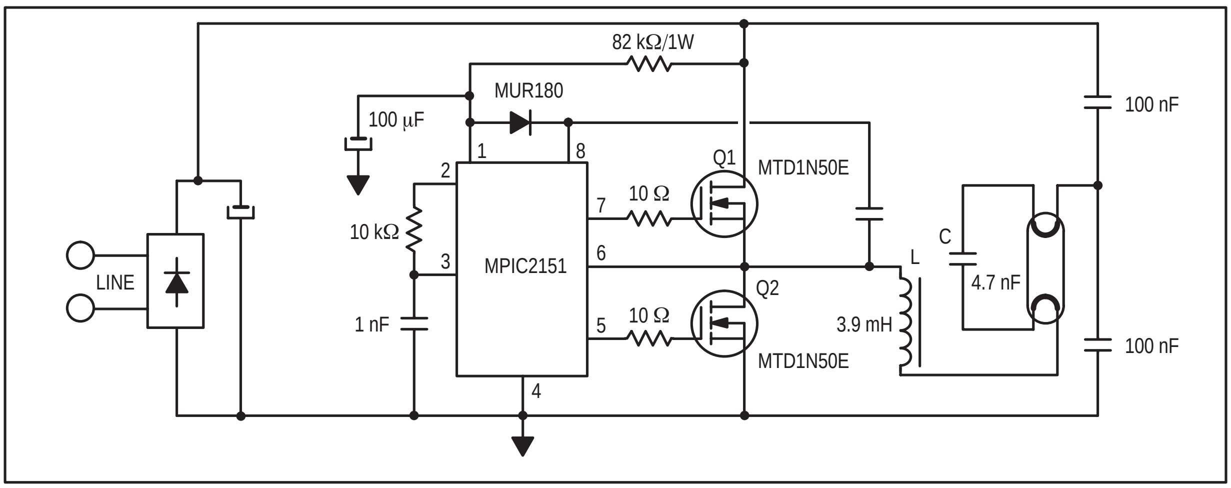


Figure 12–2. Basic Driven CFL

The resonant frequency of a serial RLC network is given by equation (1):

$$fo = \frac{1}{2 * \pi * \sqrt{(L * C)}} \qquad (1)$$

Out of resonance, the impedance is given by equation (2):

$$Z = \sqrt{(R^2 + (L\omega - 1/C\omega)^2)} \qquad (2)$$

When the frequency equals resonance, the impedance drops to a minimum:

$$Z = R \qquad (3)$$

The quality factor of the RLC network is given by the equation (4):

$$Q = (L * \omega)/R \qquad (4)$$

At resonance, the voltage across the capacitor is at its maximum as given by (5):

$$V_C = V_{CC} * Q \qquad (5)$$

From the AC stand point, a half bridge circuit is built around two power switches and is loaded by a series RLC network. It operates in three modes:

Phase 1: Pre–heating the filaments to improve start efficiency and extend the tube's life time. The operating frequency forced by the converter moves to point A on the curve given in Figure 12–3. The current is high enough to rapidly heat–up the filaments.

Phase 2: Striking the fluorescent lamp. The frequency is pushed close, but preferably not equal, to the RLC resonance (point B). The current increases, the voltage across capacitor C_1 is at a maximum, as given by equation 5, and the lamp strikes.

Phase 3: Continuous operation – The operating frequency is far from the RLC_1 resonance (point C) and the current flowing through the lamp is mainly dependent upon the value of inductor L (leaving aside, for the moment, the other parameters), hence upon the frequency of the chopped voltage provided by the two switches.

One must keep in mind that capacitor C_1 is being shorted by the low impedance of the fluorescent tube, the series RLC_1 circuit is heavily damped and no significant Q coefficient can be generated in the network.

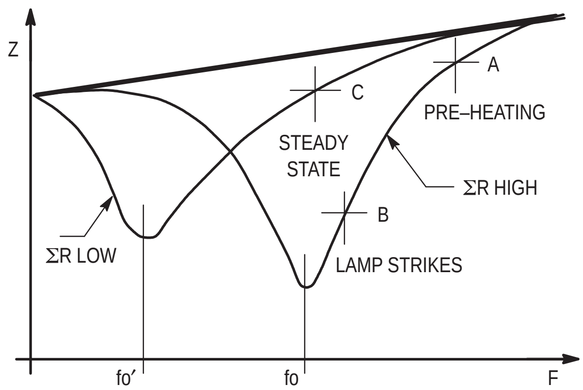
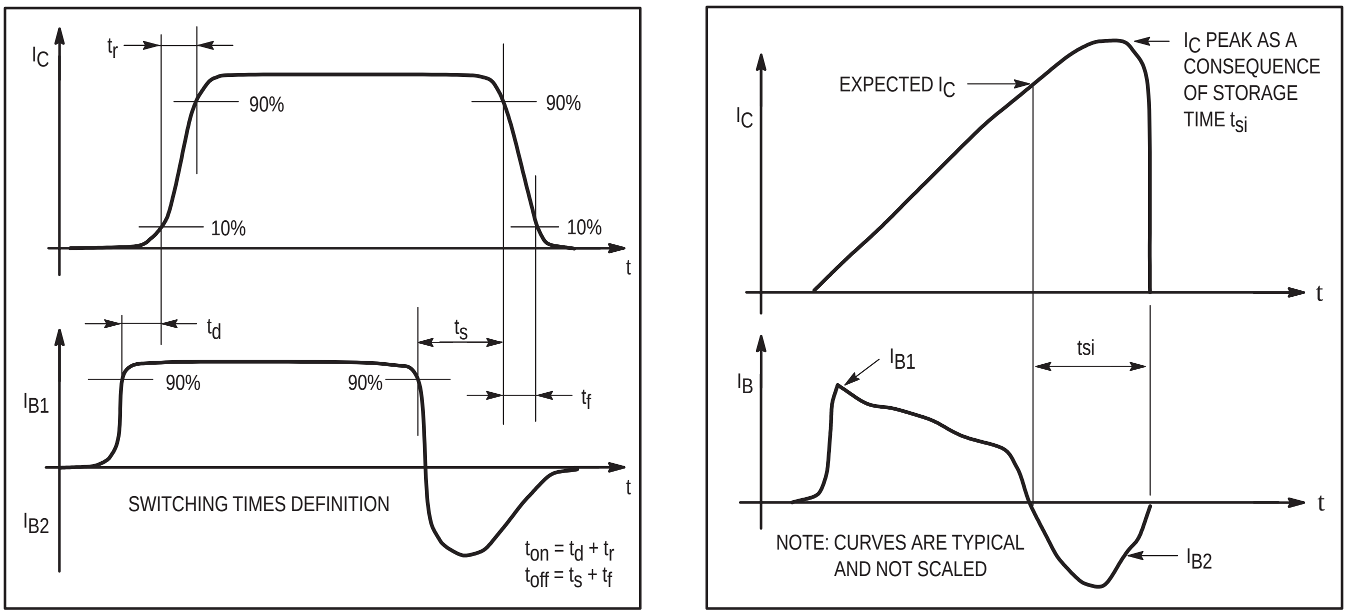


Figure 12–3. RLC Series Resonant Network Behavior

If we use bipolar power semiconductors to build the output stage of the converter, we must take into account the switching characteristics of these devices because they highly influence the performance of the electronic ballast. As one can imagine, a bipolar transistor based self oscillant topology is most sensitive to the AC parameters:

– The frequency **– F –** is dependent on the storage time **– t_{si} –** as depicted in Figure 12–4.

– The current fall time **– t_{fi} –** and the storage time **– t_{si} –** are highly sensitive to the reverse bias applied across the Base/Emitter.



For a standard bipolar transistor, the storage time is dependent on the gain (β) of the transistor associated with the operating point I_C and the drive conditions I_{B1} and I_{B2}. The H2BIP device is free from this relationship, for a given I_C range, and provides a far better design than older bipolar technology.

Typical I_C and I_B current waveform in a self oscillant half bridge circuit.

Figure 12–4. Switching Characteristics of a Bipolar Power Transistor

With regard to a MOSFET, storage time can be disregarded since, like the fall time, it's mainly dependent upon the impedance connected across Gate/Source at turn off. At first glance, the MOSFET would be preferred for these types of electronic ballast, but it presents two major drawbacks:

– The Rdson is a function of the Breakdown voltage capability: the higher the BVDSS, the higher the Rdson for a given chip size.

– The Rdson has a positive temperature coefficient and its absolute value will double over the usual +25°C to +125°C temperature range, yielding high on state losses into the silicon.

Table 2 gives a summary of the comparison between BIPOLAR and MOSFET power devices. One must point out that, for low line voltage (eg. 120 V), the MOSFETs can be the preferred choice because they bring more advantages than drawbacks compared to other semiconductors technologies.

Table 2. Bipolar to MOSFET Simplified Comparison for 500 V Breakdown Voltage

	V_{ON}	GAIN	tsi	tfi	RELATIVE CHIP SIZE
BIPOLAR	V_{CEsat} < 1 V	$\beta = f(I_C)$ $\beta = f(T_J)$	1.8 µs <—> 2 µs* 1.5 µs <—> 5 µs**	120 ns <—> 400 ns	1.0
MOSFET	R_{DSon}*ID = f(T_J)	g_{fs} = CONSTANT	200 ns^x	40 ns <—> 80 ns	1.2

NOTES: * Bipolar H2BIP Technology with Built–in Free Wheeling Diode
** Standard Bipolar Devices
x Dependent Upon the G/S Impedance

On the other hand, since the Rds_{on}, hence the ON losses, is a function of the die size, the designer must cope with the cost/performance ratio to make the final design cost effective.

To overcome the compromise associated with either the bipolar transistor or the MOSFET, we have developed a new concept, at the silicon design level, yielding an IGBT fast enough to be suitable for the 40 kHz operating frequency commonly used in the CFL electronic ballast's.

PowerLux™ IGBT

Main characteristics

The IGBT technology is widely used for high current/high voltage applications, such as motor controls and automobile engine ignition circuits. It has proven to be rugged and reliable, but is prone to high switching losses when operated above a few kilohertz, due to the large tail current that appears at turn off.

Figure 12–5 gives the basic equivalent schematic of a standard IGBT, the die cross section is shown in Figure 12–6.

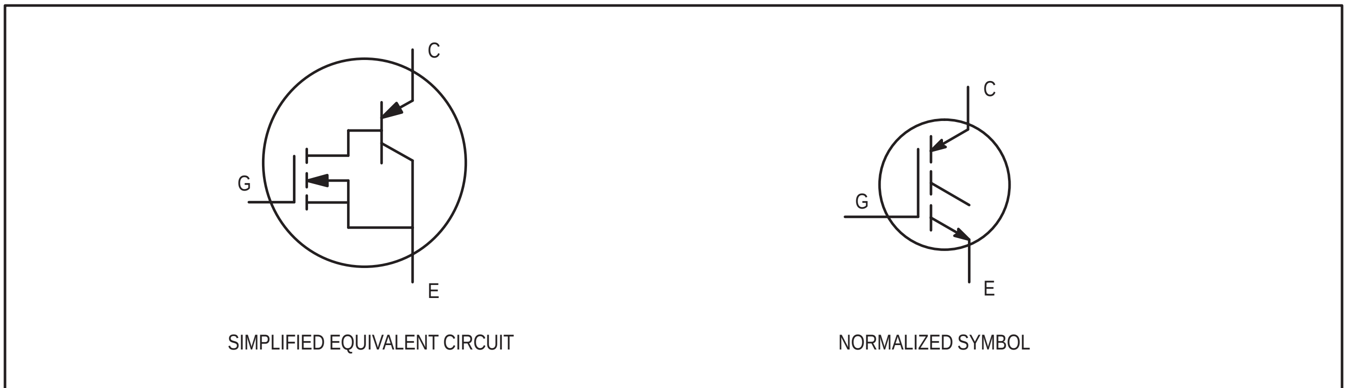


Figure 12–5. Basic standard IGBT equivalent circuit

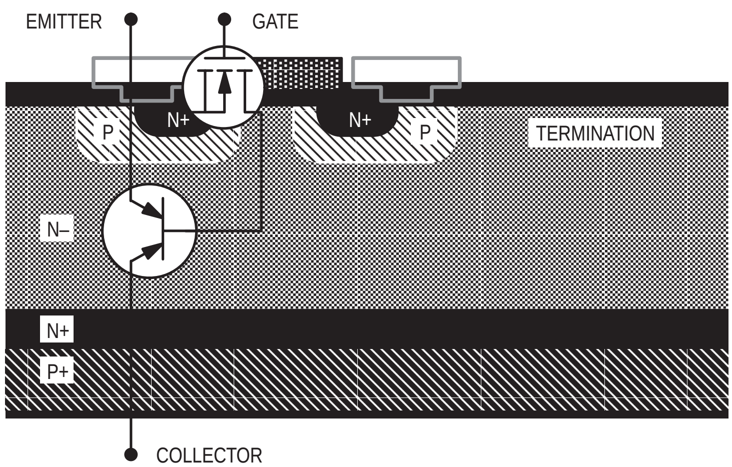


Figure 12–6. Typical Standard IGBT Die Cross Section

The basic equivalent circuit shows that the IGBT is a MOS gated device which controls the base current flowing into a junction transistor which does not have an integrated free wheeling diode.

This concept has two advantages:

1 – The input is identical to a MOSFET: high impedance, voltage driven.

2 – The output is equivalent to a BIPOLAR: Von is identical to Vcesat and, unlike the MOSFET, does not increase, for a given current I_D, over the operating temperature range.

On the other hand, since there is no path to remove the extra charge stored in the Base/Emitter of the output stage when the device switches off, the drain current will exhibit a long fall time known as a tail current effect. As a matter of fact, during switch off, the MOS turns off much faster than the bipolar junction and the charges are trapped in the Base structure. This is the main drawback that limits today's standard IGBT to applications running in the 20 kHz range.

However, the technology is robust and, thanks to its MOS input, far easier to control than a Bipolar transistor. These advantages make the IGBT the best choice to build high current drivers as stated above.

IGBT Main Electrical Characterisitics

Like any other semiconductor, the IGBT's electrical Characterisitics are limited by normalized DC and AC parameters that are defined in the designer's data sheet. Although all these parameters are important, the critical ones, from an electronic ballast stand point, are linked to the expected behavior of the device when it's operated in the application:

1 – Operating frequency stability
2 – Turn – OFF losses
3 – ON state losses
4 – Voltage capability

The first two fields are dependent upon the switching performance, the third one being a function of the transconductance and associated ON voltage, the fourth being dictated by the breakdown voltage of the device.

The IGBT has two main drawbacks:

1 – Latching effect: the device latches when the I_D current exceeds a given value.
2 – Current tail.

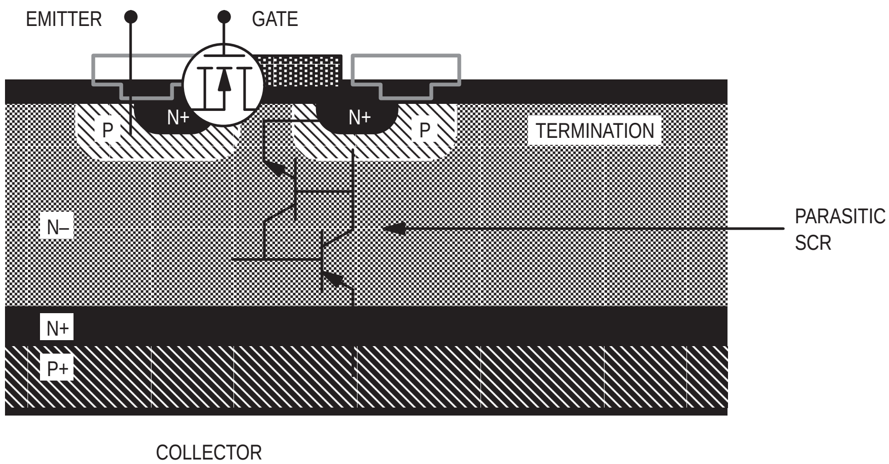


Figure 12–7. Parasitic Thyristor into the IGBT Structure

The tail current is of prime importance for the electronic ballast because it generates most of the switching losses. As a matter of fact, since these applications operate, in steady state, in the 30 kHz to 50 kHz range, this type of circuit cannot accommodate semiconductors with a poor switching performance: very fast current fall times are mandatory as described Figure 12–8.

The tail current and therefore, the switching loss is the most important parameter because it determines the suitability of the IGBT for operating at 40 kHz.

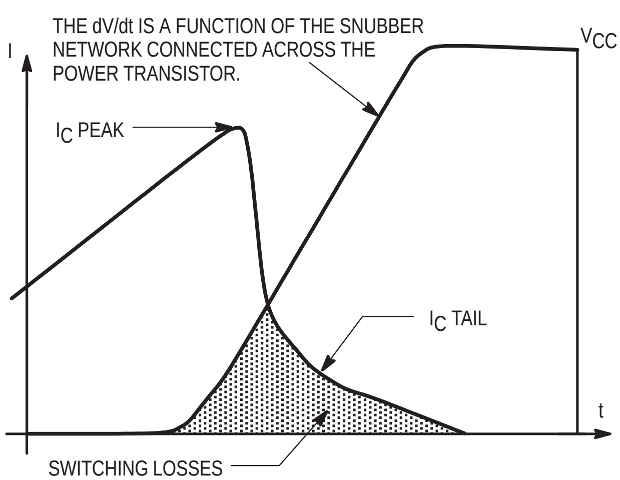


Figure 12–8. Switching Losses

As shown by the typical circuit diagrams given in Figures 12–1 and 12–2, one must provide a path to re–circulate the inductive current at the turn off of either switch. When the output stage is built with Bipolar devices, an extra free wheeling diode is connected across the Collector Emitter. The H2BIP* technology was developed three years ago to integrate this function into the power die. Of course, one can avoid the diode, using the Base Collector junction to accomplish the function, but this is not recommended for two reasons:

1 – If the voltage dropped across the Base/Emitter external network is larger than the BV_{EBO}, then the junction is avalanched on each pulse and the expected life time can be downgraded if the energy is higher than the maximum rating of the transistor.
2 – Forcing a forward current into the Base/Collector junction yields poor control of the switching performance (unless the transistor is operated in a very hard saturation mode, but this may lead to high losses in the drive network), which, in turn, downgrades the RBSOA characteristics of the device (a characteristic that allows the transistor to sustain the fault operating conditions).

The MOSFET alternative brings the advantage of the body diode that performs the free wheeling function.

Until now, the IGBT did not have an intrinsic diode. The PowerLux™ devices have being designed with a monolithic diode, making the device suitable for a CFL electronic ballast applications. The main characteristics of that diode are shown in Figure 12–9.

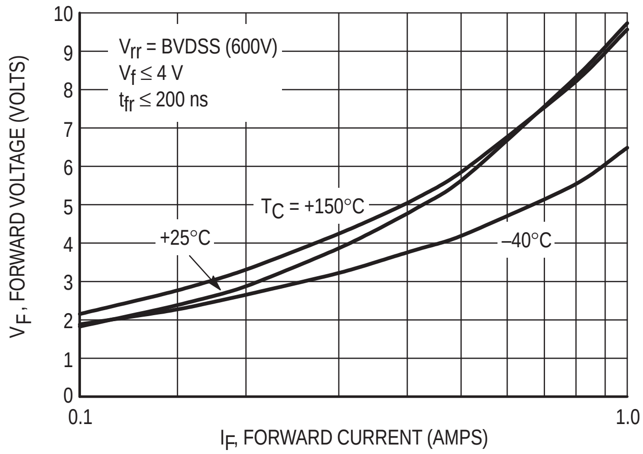


Figure 12–9. PowerLux™ IGBT Diode Characteristics

PowerLux™ IGBT Electrical Performance

The fast IGBT, specifically designed for the compact Fluorescent Lamp applications, brings an integrated collector/emitter diode and has switching capabilities that make the device suitable for operating frequencies up to 40–50 kHz. This new part belongs to the PowerLux™ family, the basic equivalent circuit being given in Figure 12–10.

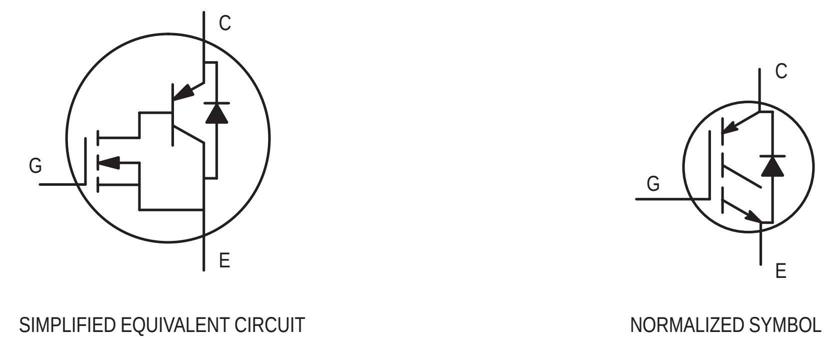


Figure 12–10. Simplified IGBT Equivalent Circuit

BREAKDOWN VOLTAGE BV_{DSS}

Since the device is intended to be used on the 230 V mains, with no or limited voltage regulation, the BV_{DSS} has been targeted at 600 V minimum. Since that parameter has a positive temperature coefficient, as shown by the curve given Figure 12–11, the BV_{DSS} is free of thermal run away.

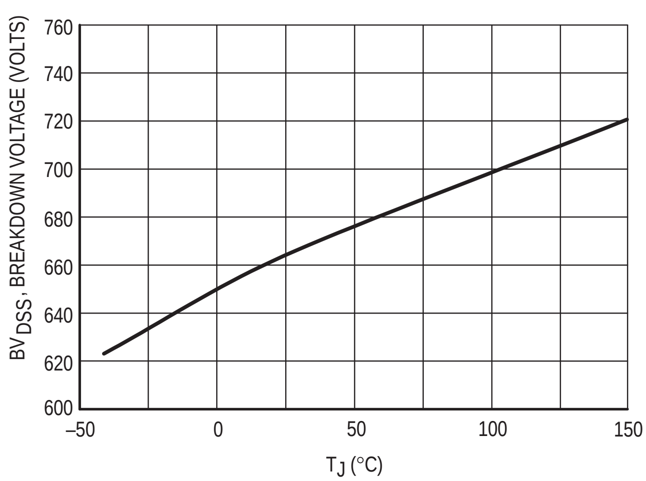


Figure 12–11. BVDSS = f(Tj)

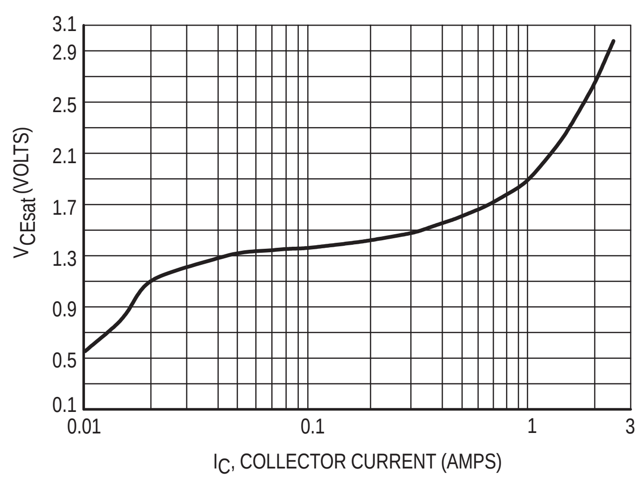


Figure 12–12. $V_{ON} = f(I_D)$ @ Vgs = 10 V, T_C = +25°C

ON STATE VOLTAGE V_{ON}

This parameter plays a significant role since, associated with the collector current I_C, it generates the ON state losses which, together with the switching losses, determine the junction temperature for a given junction to ambient thermal resistance and ambient temperature.

Keeping in mind the CFL as the target application, the IGBT has been designed to get a $V_{ON} \leq 1.80$ V at I_C = 400 mA. The curve given Figure 12–12 shows the typical value V_{ON} as a function of the collector current.

As depicted in Figure 12–13, the V_{ON} has a negative thermal coefficient and there is no risk of thermal run away when the device is operated within its maximum ratings.

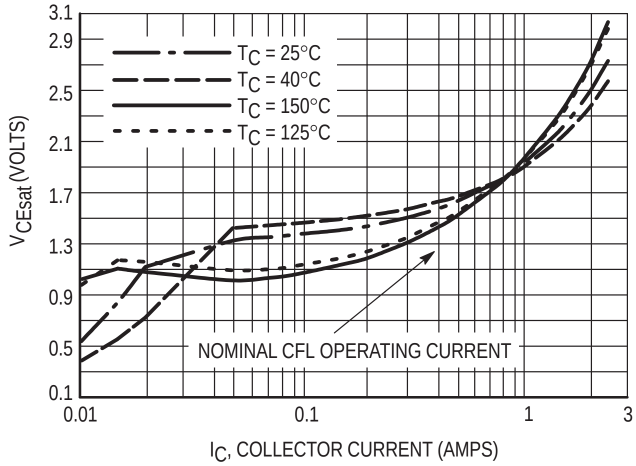


Figure 12–13. $V_{ON} = f(T_J)$, Vgs = 15 V

THRESHOLD VOLTAGE Vgs_{th}.

The threshold voltage is defined as the Gate/Source voltage that yields a 1 mA collector current. For an electronic ballast application, one must consider two main types of circuits:

1 – Self oscillant: the drive voltage, derived from either a second transformer or from the output inductor, is almost sinusoidal and the Vgs_{th} spread may influence both the turn–on and turn–off, hence the operating frequency. Like the MOSFET, this behavior is highly dependent upon the circuit used to drive the devices.

2 – IC Driven: The Vgs is supplied by a specific driver, like the MPIC2151, with a square waveform. The Vgs_{th} variation has no influence on the timing as long as it's well below the 10 V to 18 V supplied by the integrated driver. On the other hand, the minimum Vgs_{th} must be higher than the maximum logic zero level voltage sourced by the driver, otherwise the IGBT could be operated in continuous conduction mode.

Additionally, the IGBT must be made insensitive to the electrical noise coming from the very fast dI/dt and dV/dt generated in the circuit. Taking into account these specifications, the PowerLux™ IGBT has been designed with a typical Vgs_{th} of 4.0 V, the spread being ±1.00 V.

GATE SOURCE BREAKDOWN VOLTAGE BV_{GSS}

The device is protected by two back to back zener diodes, integrated into the chip and connected across Gate–Source. This clamps the Gate voltage to typically ±21 V, making the device ESD resistant (Human Body Model). However, it's recommended to use the standard procedures when handling these MOS gated devices to avoid the damage associated with high ESD voltages.

SWITCHING LOSSES E_{off}

Since one cannot fully define the behavior of the IGBT with a collector current fall time **– tfi –** only, the devices are characterized by a switch off energy **– E_{off} –** parameter which takes into account the complete tail current. The PowerLux™ IGBT has an $E_{off} \leq 5\mu J$ at Tj = +25°C, with a positive temperature coefficient as depicted in Figure 12–14.

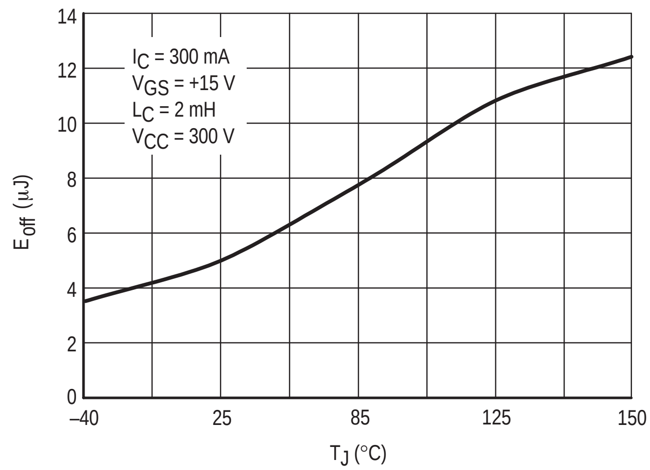


Figure 12–14. Switching Losses $-E_{off}-$ as a Function of Temperature

FREE WHEELING DIODE

The built–in diode has been designed to match the CFL's requirements:

$Vf \leq 4.00$ V @ If = 400 mA, Tj = +25°C

$tfr \leq 200$ ns @ If = 400 mA, Tj = +25°C

Since the current flows into the diode for a limited duty cycle (typically 15%), the relatively high Vf does not generate more than a few milliwatts of loss into the silicon as given by equation [7]:

$$P_{diode} = If_{rms} * Vf * DC \tag{7}$$

$$P_{diode} = 0.090*4*0.15$$

$$P_{diode} = 54 \text{ mW (maximum)}$$

PowerLux™ IGBT APPLICATION

Typical CFL circuit

With a current capability of 500 mA in steady state, up to 2 A in pulse mode, the MMG05N60E is well suited for the full power range of CFL applications. As a matter of fact, since the power into a fluorescent tube is a function of its length, hence the Von across the two electrode ends, the current flowing into the transistors is almost constant over the 7 W to 23 W range. The main difference is the strike voltage (the longer the fluorescent tube, the higher this parameter) which, in turn, needs a higher current during the start–up. Although the breakdown capability of the power device is not related to the strike voltage required by the lamp, the silicon must be able to sustain the inrush current during both the filament pre–heating and the strike sequence. The demoboard designed in the Application Lab takes care of these constraints, using the integrated MPIC2151P driver to control a couple of IGBT in the popular half bridge topology as described Figure 12–15.

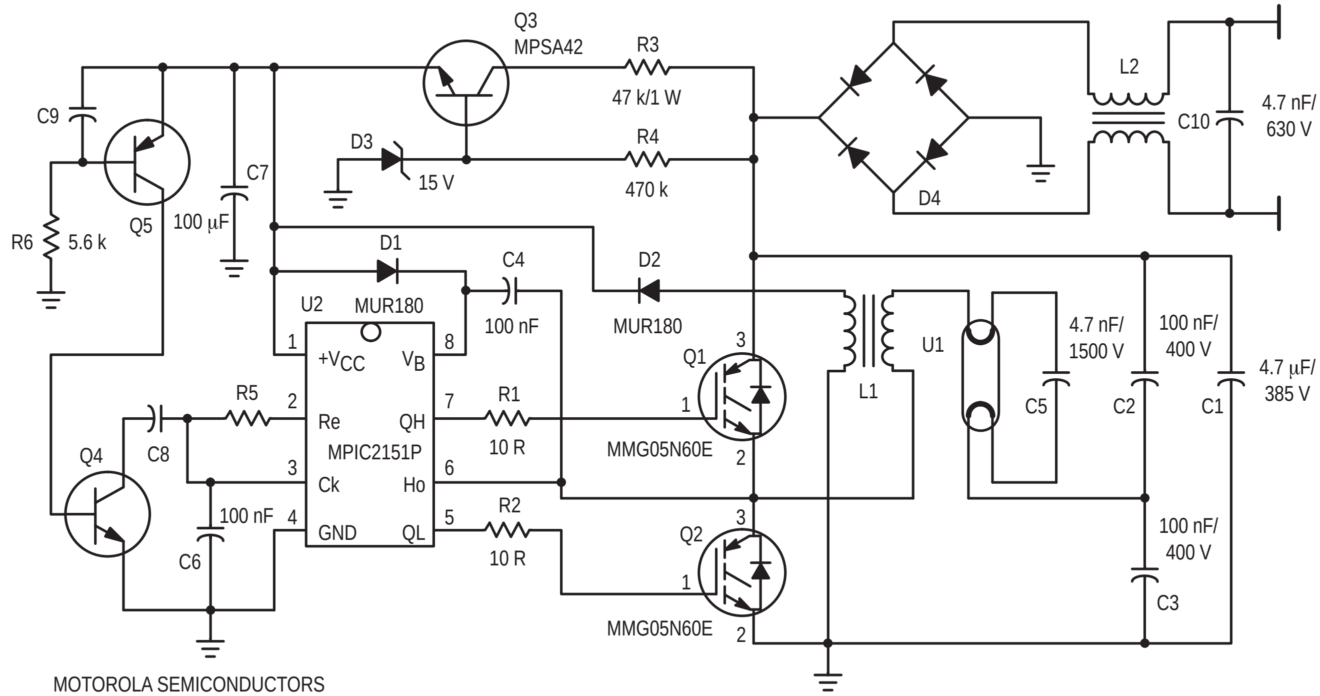


Figure 12–15. Demoboard Schematic Diagram

Start–Up

In order to increase the life time of the lamp, the filaments are pre–heated prior to applying the strike voltage across the electrodes. This is achieved by starting the circuit at a high frequency, connecting capacitor C2 across the timing network after a delay coming from R5/C7. The curves given in Figure 12–16 show the behavior of the RLC series resonant network built with the components shown in Figure 12–15, assuming the cold resistance of the filaments being 10 Ω each, with a thermal time constant of 500 ms.

Since this CFL is of the disposable type, there is no need for safety circuits as one should include in the linear tube used in the industrial application.

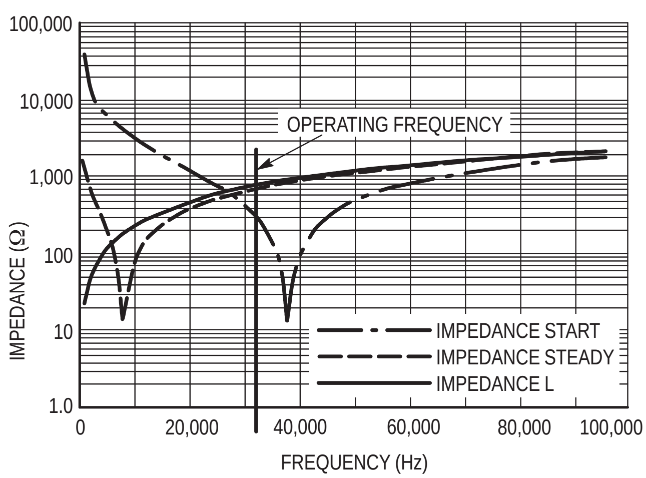


Figure 12–16. RLC Series Resonnant Circuit Typical Behavior

Impedance START = impedance of the start–up network built with the output inductor L and resonant capacitor C.

Impedance steady = steady state impedance of the output inductor associated with the passive side of the half bridge.

Impedance L = impedance of the pure output inductor.

Steady State

Once the lamp is ON, the current is limited by inductor L, according to equation (8):

$$I = (Vcc–Von)/L\omega \qquad (8)$$

with: Vcc = DC bus supply voltage

Von = ON state voltage across the fluorescent tube

Since both Vcc and Von are constant (for a given power and line voltage), and the operating frequency is bounded by low and high limits, the range of potential inductance values is very restricted, and L can be calculated straightforward by combining equation (9) with re–arranged equation (8):

$$P = Von*Irms \qquad (9)$$

$$L = [Von*(Vcc–Von)]/(P*2*\pi*F) \qquad (10)$$

For an 11 W lamp powered from a 230 V nominal line, operated at 35 kHz, the inductor is:

$$L = [50*(310–50)]/(11*2*\pi*35^{+3})$$

$$L = 3.09\ mH$$

As we can observe on the curve given in Figure 12–16, the circuit operates far from the resonance generated by L and C5/C6 in parallel. It's the designer's responsibility to select the operating point either close or far from a second resonant pole, keeping in mind the following points:

a – When operated far from resonance, the circuit is less sensitive to the tolerances of either component, but the switching losses are maximum since the power devices are switched off at peak collector current.

b – When running in a quasi resonant mode, the current is sinusoidal and switched off during the negative going slope of the sine wave. Consequently, the switching losses are minimum, but the circuit becomes more sensitive to the electrical tolerances of the passive and active components.

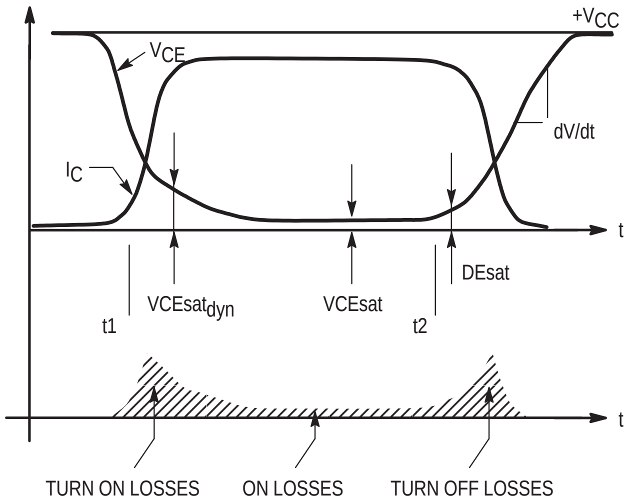


Figure 12–17. Switching Time and Loss Definitions

The switching losses generated by the IGBT are calculated with equation (11) and added to the ON state losses, with those coming from the integrated free wheeling diode, to derive the maximum junction to ambient thermal resistance as stated by equation (18) (see Figure 12–17 for the definitions of the related parameters).

$$S_{WL} = E_{off} * F \tag{11}$$

with: F = operating frequency

Eoff: energy dissipated during switch off

$$E_{off} = Vce*Ic \tag{12}$$

The E_{off} parameter is provided by the IGBT designer's data sheet. It is fully characterized for preferred operating conditions and a set of curves gives the typical behavior as a function of the collector current and the junction temperature.

$$P_{ON} = \int_{t1}^{t2} V_{ON} * I_C * dt \tag{13}$$

Since there is no dynamic Vcesat associated with an inductive load, equation (13) can be simplified as:

$$P_{on} = 1/2*Von*Ic_{peak}*DC \tag{14}$$

On the other hand, one cannot abruptly cancel the current into the inductor so the integrated free wheeling diode provides a path to re–circulate this current. The forward drop of the diode is the most important parameter because it generates most of the diode losses as given by equation (14):

$$P_D = Vf*If*F \tag{15}$$

Like the Pon losses, equation (15) can be simplified to:

$$P_D = 1/2*Vf*Ifpeak*DC \tag{16}$$

Thermal Analysis

The junction temperature of a semiconductor, operated under steady state conditions, is given by equation (17):

$$Tj = Tamb + \Sigma P*Rth_{j–a} \tag{17}$$

The maximum junction temperature for a silicon device, assembled into a plastic package, is +175°C, but in order to improve the long term reliability, it's highly recommended not to continuously operate the device above +150°C. Also, if the silicon temperature is forced to that value, the pins of small packages like the SOT223 or the TO92, will be nearly at the same temperature as the junction and the solder attach to the printed circuit board will be rapidly downgraded. Consequently, it's far better to operate the power devices around +120°C junction temperature to avoid the risk of long term overall reliability. Assuming the maximum ambient temperature being +90°C, we can calculate the maximum junction thermal resistance by re–arranging equation (17) as stated below:

$$Rth_{j–a} = (Tjmax – Tamb)/\Sigma \tag{18}$$

$$Rth_{j–a} = (120–90)/0.30$$

$$Rth_{j–a} = 100°C/W$$

Since the SOT223 junction to ambient thermal resistance is 156°C/W, it's obvious that it cannot be operated without a minimum heatsink to reduce the Rthj–a to 100°/W. This is easily achieved by using extra copper area on the pcb to mount the IGBT. The curve given Figure 12–18 gives the thermal resistance as a function of the foot print area. A single copper rectangle (or square) of 10x6 mm (using standard 35 µm thickness) is enough to get the expected $Rth_{j–a}$ as calculated above.

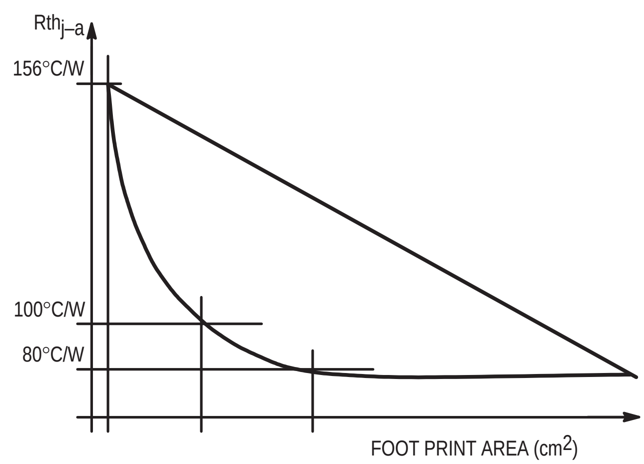


Figure 12–18. Junction to Ambient Thermal Resistanceof a SOT223 Package

Note: the curve is given for information only: accurate data are available from the Motorola surface mount device technical booklet.

Engineering Test Results

The engineering tests, performed in our Toulouse Applications Laboratory, are summarized by the oscillograms given Figures 12–19 and 12–20. The critical point is, beside the V_{on}, the collector current fall time: as depicted in Figure 12–20 the current tail is negligible and the PowerLux™ IGBT can safely operate up to 50 kHz in the 5 W to 23 W power range.

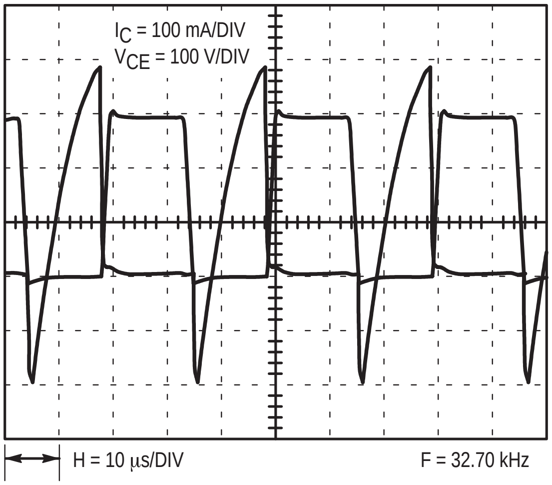


Figure 12–19. Steady State Operation (V_{line} = 230 V)

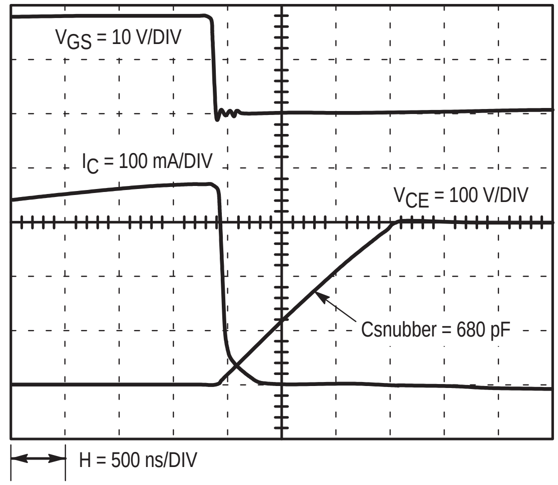


Figure 12–20. Switching Losses in the Steady State

In the steady state operation, the case temperature of the TO92–1W device increases by +26°C, yielding the ability to operate the IGBT up to +100°C ambient. Since, unlike the bipolar device, there are no risks associated with the degradation of the hfe with the temperature, the PowerLux™ IGBT is free from thermal runaway as a result of desaturation. On the other hand, thanks to a latch up trip current level above 5 A, the IGBT is safe from such mechanism, even under start–up conditions.

Low Cost Version

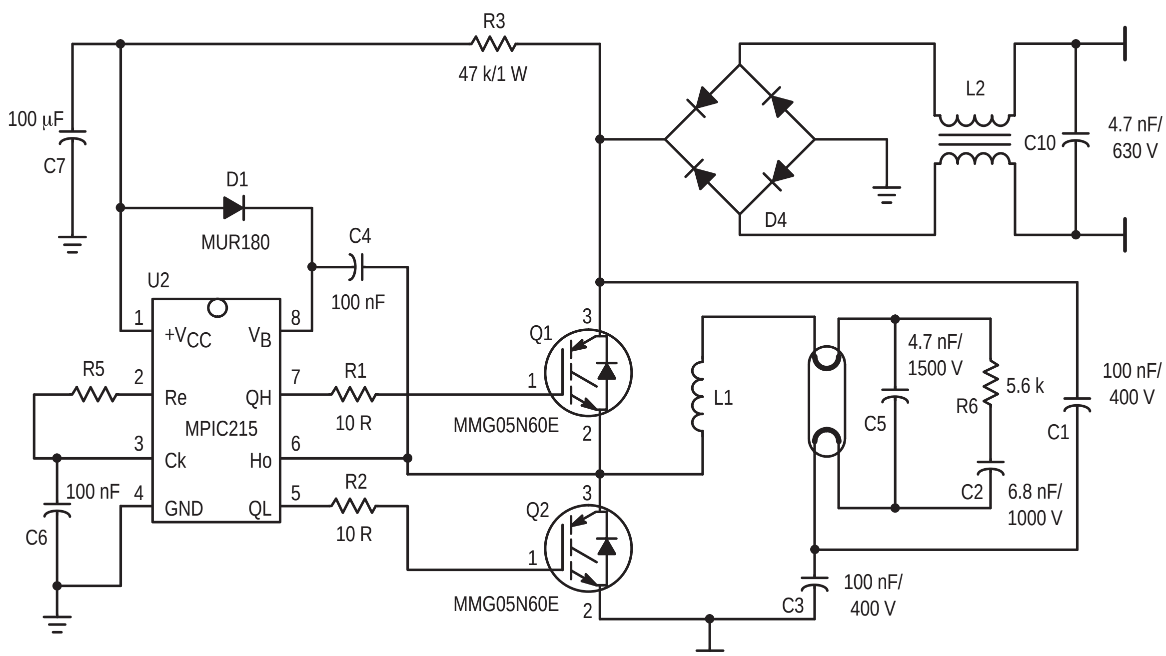
The schematic given Figure 12–15 can be simplified to reduce overall cost of the CFL as depicted Figure 12–21:

a – Replace the pre–heating active network with a PTC and an extra high voltage capacitor in the resonant pole. The PTC can also be connected directly across C5 to dump the circuit until the PTC reaches its high temperature value.

The drawback is a loss of control and the heat generated by the PTC. As a matter of fact, to get the expected resistance, the PTC must operate at +130°C under steady state conditions.

b – Remove the active VDD supply, using a power resistor R3. Like the PTC, the drawback is mainly the heat coming from a component which dissipates around 1 W.

c – Use one capacitor only to close the loop on the passive side of the half bridge. At that point, one must pay extra attention to the imbalance of the magnetic circuit together with the RFI generated by the module.



MOTOROLA SEMICONDUCTORS
PowerLux™ IGBT DEMO BOARD
LOW COST MODEL
ISSUE: 1.00

Figure 12–21. Simplified Low Cost CFL Application

The cost can be further reduced by using a self oscillant circuit as depicted Figure 12–22. Transformer T1 provides the positive feedback to drive the IGBT, the associated components R,D,C being used to improve the dynamic performance of the power device. The drive can also be derived from the output inductor, but such analysis is beyond the scope of this paper.

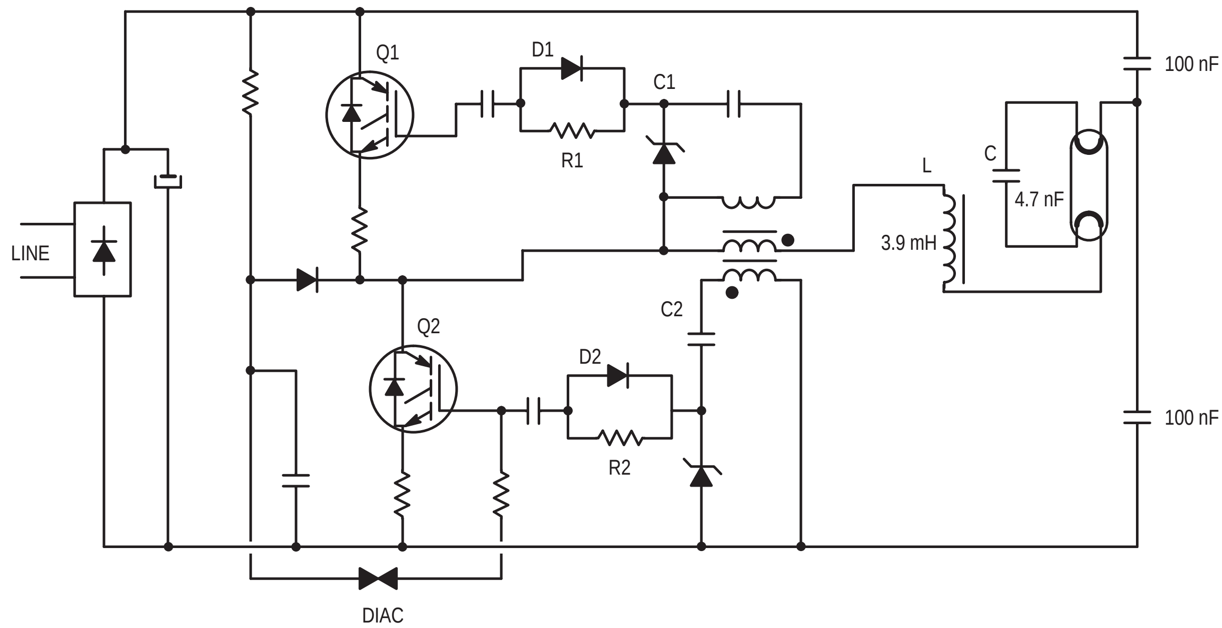


Figure 12–22. Self Oscillant, Low Cost CFL Basic Circuit

One must point out that, although this is the lowest cost solution, it is not easy to design, and it has been already proven that a driven circuit (with a dedicated driver), is usually faster to design and, consequently, the best solution for a short time to market. Also, a driven circuit can be easily modified to control lamps of different output power.

Typical PFC Circuit

Nowadays, European Regulations specify that any piece of electronic equipment connected to the line must have a cosΦ of 0.94 minimum with a THD of 25% maximum for the third harmonic. However, the full implementation of that regulation for input power below or equal to 30 W, hence for the CFL, has been postponed to 1998 and, at the time of printing, no decision has been taken.

In any case, since the PFC will eventually be mandatory, a typical application circuit is given in Figure 12–23.

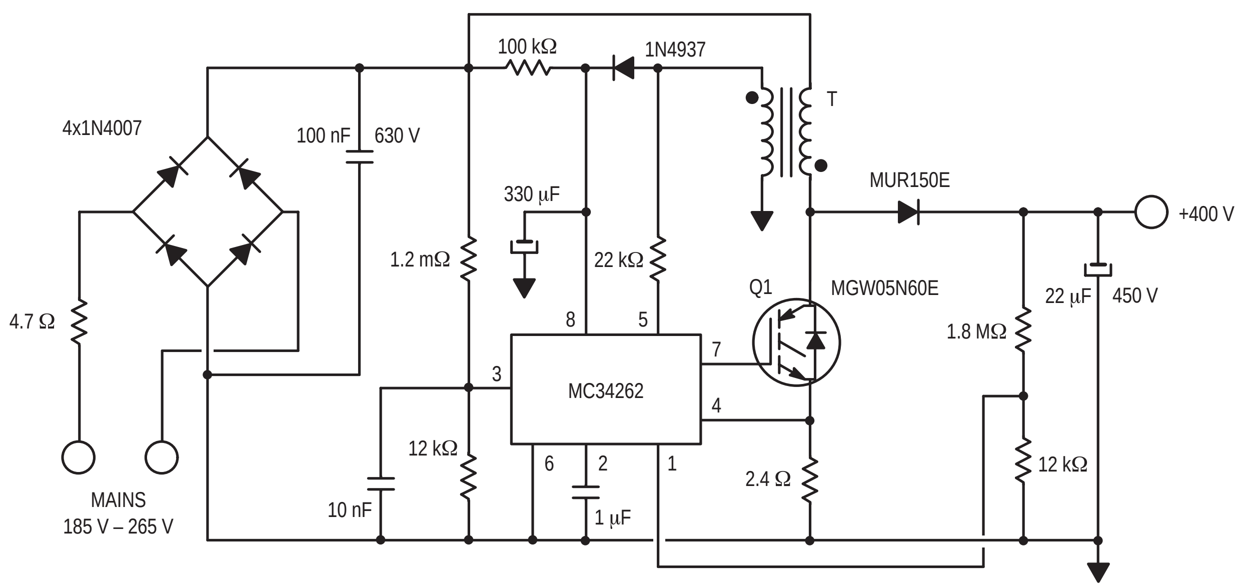


Figure 12–23. Basic Low Cost Power Factor Correction Circuit

Since the PFC boost circuit can easily operate in the 40 kHz range, with a peak current below 500 mA, the MGW05N60E PowerLux™ IGBT can be used to fulfill that particular function, bringing another net cost saving to the CFL and other low power, off–line applications.

Device Comparison: BIPOLAR – MOSFET – IGBT

Selecting a power semiconductor to design an electronic ballast is not straightforward because each of the available technologies has advantages and drawbacks. The choice is the result of the end product specifications and the compromises the design engineer can make for a given application.

Table 3 below is intended to aid the designer in selecting the power device for either a Compact Fluorescent Lamp or a Linear Industrial Tube ballast.

Table 3. Power Semiconductor Technologies Comparison

DEVICES	Vsat	BVCEO	FBSOA	RBSOA	Storage time tsi	Fall time tfi
BIPOLAR standard	LOW	HIGH (1600 V max)	2^{nd} BV limited	Vbe bias dependent	High, wide spread	Medium
BIPOLAR H2BIP	LOW	HIGH (1800 V max)	2^{nd} BV limited	Vbe bias dependent	Low, narrow spread	Fast
MOSFET	=Rdson*ID	Medium (600 V max)	Square =BVDSS	Square =BVDSS	negligible	very fast
IGBT PowerLux™	Medium	Medium (600 V max)	2^{nd} BV limited	Gate bias dependent	negligible	fast

DEVICES	Die size (relative)	Smallest package	Operating Tj °C max	DRIVE	Relative Cost	Dimming sub function
BIPOLAR standard	1.00	DPAK	+175°C	IB1 – IB2 Complex	Medium	Complex
BIPOLAR H2BIP	1.15	DPAK	+175°C	IB1 – IB2 easy	Medium	Medium
MOSFET	1.30	DPAK	+175°C	Voltage Vgs very easy	High	Easy
IGBT PowerLux	0.40	TO92–1W SOT223	+175°C	Voltage Vgs very easy	Low	Easy

CONCLUSION

The PowerLux™ IGBT meets all of the electrical requirements for a Compact Fluorescent Lamp application. Thanks to its chip size which can be packaged in either a SOT223 or a more conventional TO92. This brings a significant cost savings, compared to other semiconductor technologies, without downgrading the global performance of the circuit.

Because it is a MOS gated device, it can be driven by standard MOS drivers, allowing the design of high end modules with built–in functions like dimming or remote control, functions not easily achievable with a bipolar transistor.

The next step is the development of a more powerful device to fit the 55 W and 120 W applications.

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Section 13
Noise Management in Motor Drives

INTRODUCTION

During motor drive design and development, a lot of time is normally spent dealing with high noise levels that are present in these systems. A number of techniques are presented here that make the nuts and bolts of noise management easier, and therefore take a lot of re–design and debugging out of motor drive design. Many of these techniques trade some component cost for noise robustness. The benefits are reduced development cost, faster time to market, and a higher likelihood of trouble free operation in the field.

CIRCUIT TECHNIQUES

Circuit design can have a profound influence upon both the amount of noise produced and upon the susceptibility of motor drive circuits to the noisy environments in which they operate. The following discussion looks at N–Channel output stages, complimentary output stages, and controllers.

N–Channel Output Stages:

For off–line motor drives that use N–Channel IGBT's, an illustration of noise robust circuit design is provided by comparing Figures 13–1 and 13–2. Figure 13–1 shows a minimal circuit topology for one Phase output. Figure 13–2 adds the components that it takes to make this topology noise robust.

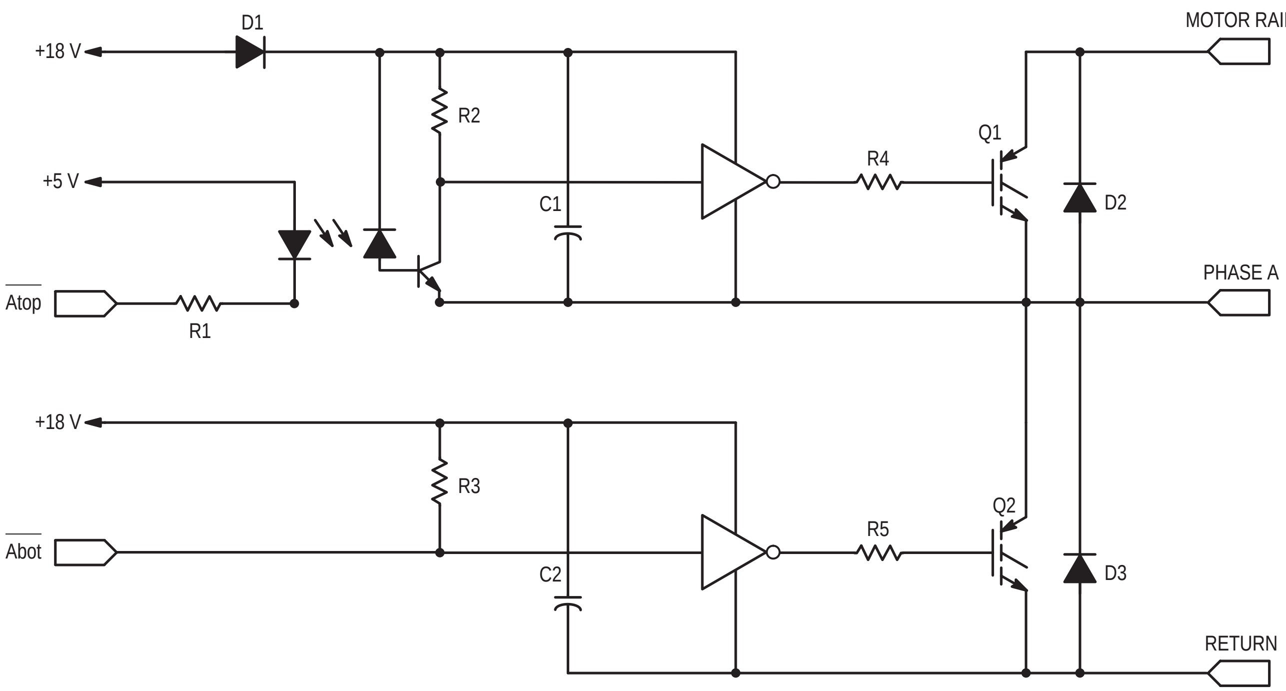


Figure 13–1. Minimal N–Channel IGBT Power Stage

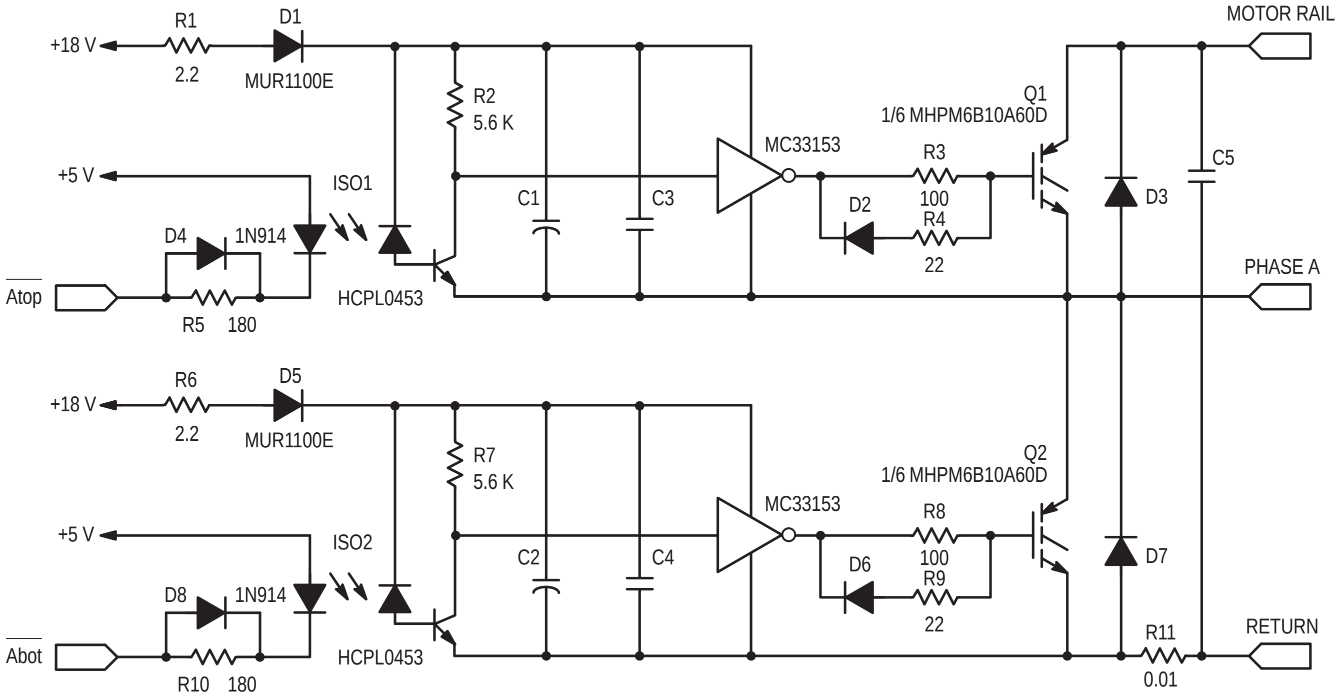


Figure 13–2. Robust N–Channel IGBT Power Stage

Perhaps the single biggest circuit design influence is the use of opto couplers. Opto's are widely used in upper half–bridge IGBT gate drives for level shifting. When used in the lower half–bridge gate drives as well, noise robustness is significantly improved.

Consider the robust design in Figure 13–2. Both Top and Bottom inputs are opto coupled to inverting gate drivers. This arrangement provides level shifting and also isolates the inputs from the high voltage power stage. The isolation provided by this circuit topology significantly improves noise immunity for two reasons. First, the opto's are very effective at keeping conducted noise away from microcontrollers. The noise isolation that they provide adds a degree of robustness that can make controller layout and debugging much simpler. Second, the use of opto's in the lower half bridge facilitates gate drive grounding, since the isolation allows each gate drive to be returned directly to the emitter of its corresponding IGBT. This is a significant issue with regard to power stage design, since ground noise effects on the gate drives is one of the more difficult issues.

To further illustrate this point, consider the schematic in Figure 13–3, where the lower half gate drives are not opto coupled. In this figure, all of the gate driver returns are first tied together, and then contact the power ground at only one point. The effects of this layout constraint are illustrated by showing parasitic ground inductance between phases as inductor Lp. When a switching transient occurs, the voltage drop across Lp shows up between the gate drivers and their respective IGBT's emitters. The result is unwanted gate–emitter voltage spikes that can cause turn–on or turn–off at inappropriate times. In contrast, use of opto couplers permits driver returns to be connected directly to their respective emitters, and eliminates the effects of phase to phase parasitic inductance.

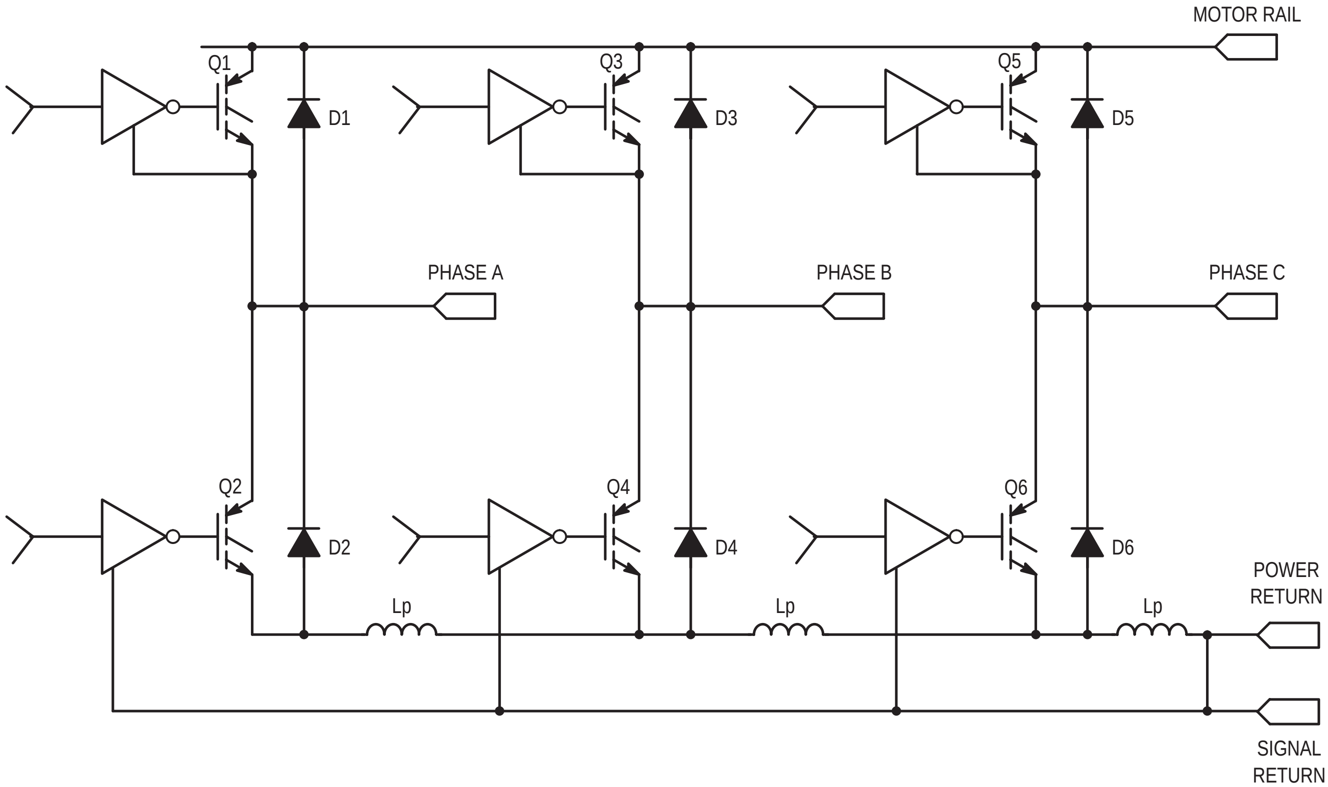


Figure 13–3. Ground Inductance

To put a rough order of magnitude on this issue, let's assume that 10 amps is switched in 25 nsec, and that Lp = 25 nH. The resulting voltage transient across Lp is then 25E–9(10/25E–9) = 10 volts. Since these transients occur between the gate driver outputs and IGBT gates, ten volt spikes can easily cause transitions to the wrong state. For drives that are less than 3 horsepower, careful layout can yield acceptable results. However, using opto couplers both top and bottom provides a much more noise robust design.

To help with gate transients, the MHPM6B10A60D IGBT's that are shown in Figure 13–2 have a 6 volt gate threshold, as opposed to the standard 3.5 volt threshold for MOS gated power devices. The higher threshold provides an additional 2.5 volts of noise margin with respect voltage spikes that will turn an IGBT on when it is supposed to be off. The MC33153 gate drivers that are also in this circuit have an under voltage lockout that is designed for the 6 volt threshold.

Referring again to Figure 13–2, diodes D4 and D8 reduce input impedance to the opto's when the inputs are high. The lower impedance provides higher noise immunity by insuring that the opto's remain off when they are supposed to be off, given an environment that includes high dv/dt. Resistors R1 and R6 protect the 18 volt gate drive supply from di/dt induced voltage transients. Without these resistors it is very difficult to get an all N–Channel power stage to work properly. They, in effect, act as shock absorbers, isolating the gate driver's bias voltage from L(di/dt) voltage spikes that are produced by switching the power devices. Although unnecessary for rectification, diode D5 serves the same function on the lower gate drive. C3 and C4 are ceramic capacitors that provide an improved high frequency return path for the gate drive during switching transients. A short high frequency return current path for the power devices is provided with C5. Polypropylene film capacitors, such as the WIMA MKP10 series, work well for this purpose.

Between the driver output and IGBT gates, two resistors and a diode are used instead of a single gate drive resistor. The additional components allow the IGBT's to turn on slower than they are turned off. Careful choice of turn–on time is important, since peak reverse recovery di/dt of the opposing transistor's freewheeling diode is dependent upon turn–on time. Since the most troublesome noise in a typical power stage is generated during reverse recovery, the two resistor topology and careful choice of values is an important part of the design.

Complimentary Output Stages:

Complimentary P–Channel / N–Channel MOSFET output stages are generally somewhat simpler than all N–Channel output stages, since voltages and power levels are lower. A typical circuit is illustrated in Figure 13–4. It shows a complimentary output stage that is capable of operating at 5 amps and 48 volts. The design challenges in this type of circuit arise from the reverse recovery characteristics of the power MOSFETs' Drain–Source diodes . Unlike IGBT's with discrete diodes that are designed for softness, power MOSFET drain–source diodes tend to be snappy during reverse recovery. Figure 13–5 illustrates this point. It shows a typical power MOSFET's drain–source diode recovery characteristics. After reaching a negative peak at turn–off, the diode's current returns very rapidly to zero. This behavior can produce di/dt's on the order of 1 amp per nsec.

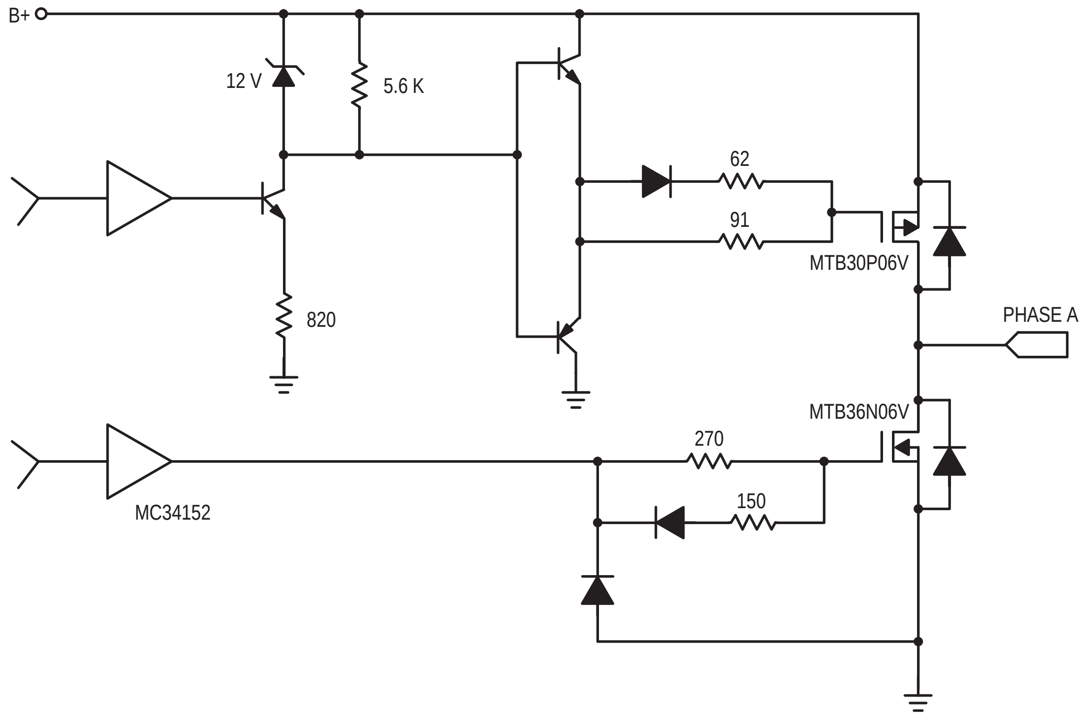


Figure 13–4. Complimentary Power Stage

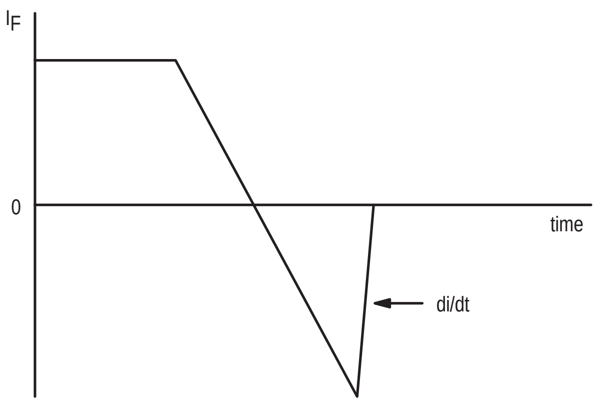


Figure 13–5. Drain–Source Diode Snap

At this rate, even 10 nH of parasitic inductance can produce troubling transients. Fortunately, diode snap can be slowed down somewhat with appropriate choice of gate drive resistors. Doing that requires different values for turn–on and turn–off. Figure 13–4 shows how, with two resistors and a diode for the gate of each MOSFET. In addition to using two values, the switching times that they target is very important. The values shown in Figure 13–4 produce rise and fall times of approximately 200 nsec. With 200 nsec switching times, the resulting gate drive impedances are high enough to permit a small amount of dv/dt induced shoot through current to flow, which considerably softens diode snap.

The way that this works is as follows. In addition to the reverse recovery current that you would normally expect, there is another current generated by switching transitions that can be called dv/dt induced shoot through current. When one transistor in the bridge turns on, its opposing transistor's drain is pulled rapidly to the opposite rail. dV/dt impressed at the drain causes a current to flow through the gate to drain capacitance and show up at the gate as input current. This current returns to the source potential through the gate drive's off–state impedance. It forward biases the gate by drive impedance times dV/dt current. If this voltage exceeds the off transistor's turn–on threshold, then dv/dt induced shoot through current is produced.

Although shoot through current is something that one normally strives to minimize, in this case a small amount is a good tradeoff for the resulting reductions in di/dt. During reverse recovery, dv/dt induced shoot through current adds to the diode's current waveform in a way that significantly reduces negative peak to zero di/dt. Correct choice of gate drive resistors can easily reduce peak di/dt by a factor of 3.

Brushless DC Motor Controllers:

Brushless DC motor controllers that use Hall Sensors pose noise immunity challenges related to the sensor inputs. The sensors are in an inherently noisy environment, since they are located in the motor close to PWM noise that is present in the windings. Given this situation, some motors do a much better job than others of presenting clean signals to the controller. For the general case, it is necessary to build some noise immunity into the way a Brushless controller receives Hall sensor inputs. An example of how this can be done is shown in Figure 13–6.

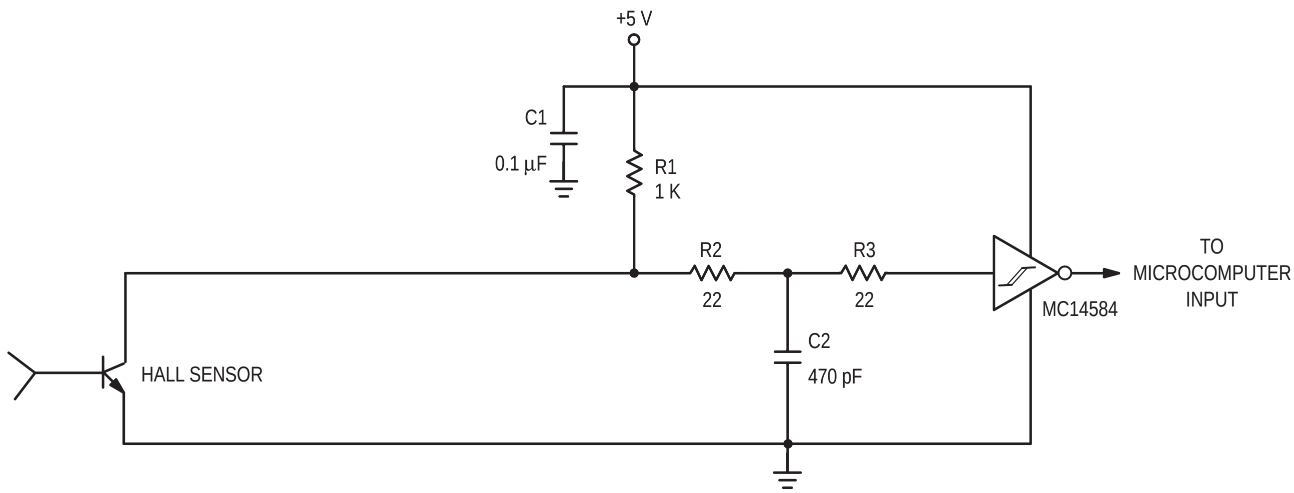


Figure 13–6. Hall Sensor Input

In this illustration, two techniques are used for isolating noise transmitted by Hall sensors. The first is a 100 nsec filter that is comprised of R2, C2, and R3. Since Hall sensor rise times are typically on the order of 500 nsec, the 100 nsec time constant does not significantly affect timing of the Hall signals, yet it is very effective at suppressing spikes that occur on Hall sensor lines. Once the signal is filtered, it is also a good idea to run it through a relatively slow 14000 series Schmidt trigger. The Schmidt trigger improves noise immunity by virtue of its hysteresis, and because 14000 series CMOS parts are inherently slower than most modern microcomputers. This is a case where it is very helpful not to use devices that are any faster than they need to be.

In addition to circuitry, the way that microcomputer code is written also has an important influence on noise robustness. Since the sequence of commutation is known, it is relatively easy to detect an out of sequence Hall sensor input. Generally speaking, when this occurs it is desirable to turn all the power transistors off until a valid Hall code is received. In other words, it is better to let the motor coast in the presence of an incorrect Hall input than to commutate to the wrong state.

LAYOUT

In a motor drive, layout is a critical part of the total design. Often, getting a system to work properly is actually more a matter of layout than circuit design. The following discussion covers some general layout principals, power stage layouts, and controller layouts.

General Principles:

There are several general layout principles that are important to motor drive design. They can be described as five rules:

Rule 1: Minimize Loop Areas. This is a general principle that applies to both power stages and noise sensitive inputs. Loops are antennas. At noise sensitive inputs, the area enclosed by an incoming signal path and its return is proportional to the amount of noise picked up by the input. At power stage outputs, the amount of noise that is radiated is also proportional to loop area.

Rule 2: Cancel fields by running equal currents that flow in opposite directions as close as possible to each other. If two equal currents flow in opposite directions, the resulting electromagnetic fields will cancel as the two currents are brought infinitely close together. In printed circuit board layout, this situation can be approximated by running signals and their returns along the same path but on different layers. Field cancelation is not perfect due to the finite physical separation, but is sufficient to warrant serious attention in motor drive layouts. Looked at from a different perspective, this is another way of looking at Rule 1, ie., minimize loop areas.

Rule 3: On traces that carry high speed signals avoid 90 degree angles, including “T” connections. If you think of high speed signals in terms of wavefronts moving down a trace, the reason for avoiding 90 degree angles is straightforward. To a high speed wavefront, a 90 degree angle is a discontinuity that produces unwanted reflections. From a practical point of view, 90 degree turns on a single trace are easy to avoid by using two 45 degree angles or a curve. Where two traces come together to form a “T” connection, adding some material to cut across the right angles accomplishes the same thing.

Rule 4: Connect signal circuit grounds to power grounds at only one point. The reason for this constraint is that transient voltage drops along power grounds can be substantial, due to high values of di/dt flowing through finite inductance. If signal processing circuit returns are connected to power ground a multiple points, then these transients will show up as return voltage differences at different points in the signal processing circuitry. Since signal processing circuity seldom has the noise immunity to handle power ground transients, it is generally necessary to tie signal ground to power ground at only one point.

Rule 5: Use ground planes selectively. Although ground planes are highly beneficial when used with digital circuitry, in power control systems they are better used selectively. A single ground plane in a motor drive would violate Rule 4 by mixing power and signal grounds at multiple points. In addition, ground planes tend to make large antenna’s for radiating noise. In motor drives, a good approach is to use ground planes for digital circuitry, and use ground traces in the power stages and for analog circuitry.

Power Stages:

There are two overriding objectives with regard to power stage layout. First, it is necessary to control noise at the gate drives so power devices are not turned on when they are supposed to be off or vice versa. Second, it is highly desirable to minimize radiated noise with layout, where tight loops and field cancellation can reduce the cost of filters and enclosures.

Looking first at gate drive, noise management is greatly facilitated by using the source or emitter connection for each power device as a miniature ground plane for that device's gate drive. This is particularly important for high side N–Channel gate drives, where the gate drivers have high dv/dt displacements with respect to power ground. If the power device's source or emitter connection is used like a ground plane, parasitic capacitive coupling back to power ground is minimized, thereby increasing the dv/dt immunity of the gate drive.

Consider the circuit that is shown in Figure 13–7. Further let's assume that the phase output swings 300 volts in 100 nsec, and that the parasitic capacitance to power ground, Cp, is only 1 pF. Then a simple i = C(dv/dt) calculation suggests that 3 mA of charging current will flow through Cp. This 3 mA into 5.6 K ohms of node impedance is much more than enough to cause false transitions. These numbers illustrate a very high sensitivity to parasitic coupling, which makes layout of this part of the circuit very important.

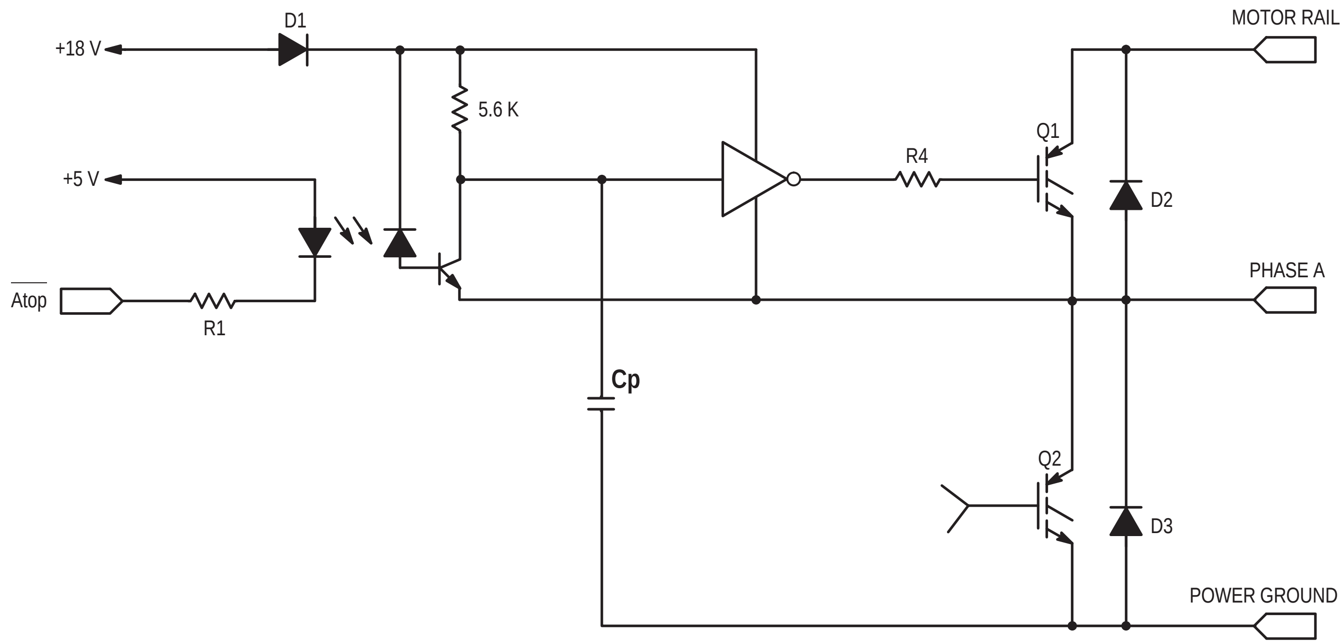


Figure 13–7. Parasitic Capacitance

In addition to viewing source or emitter connections as miniature ground planes, it is also important to keep any signals referenced to ground at least 1/8th inch away from high side gate driver inputs. Given this constraint, it is easy to see why use of use of a single ground plane in power stages is not usually good design practice.

Gate drive noise immunity is also facilitated by minimizing the loop area that contains the gate drive decoupling cap, gate driver, gate, and source or emitter of the power device. One way to do this is to route the gate drive signal either directly above or beneath its return. If the return is relatively wide (1/10th inch or greater) it forms the miniature ground plane that was previously discussed. The resulting minimum loop area minimizes capacitive coupling as well as antenna effects that inject noise at the input of the gate driver. In addition, relatively high peak gate drive currents get some field cancellation, which reduces radiated noise.

The other major source of gate drive noise that causes false transitions is non–zero voltage drops in power grounds. Using opto couplers and routing each gate drive return directly to the emitter of its corresponding power device is the cleanest way to provide noise immunity. For fractional horsepower drives where opto couplers are not practical, taking care to minimize the inductance between power device emitters or sources is a viable alternative.

In terms of reducing the amount of noise that is produced by power stages, minimizing loop areas is a key consideration. The most important is the loop that includes the upper half–bridge IGBT drain, lower half–bridge IGBT source, and high frequency bus decoupling cap. The idea here is to try to keep the high di/dt that is produced during diode reverse recovery in as small an area as possible. This is a part of the circuit where running traces that have equal but opposite currents directly over each other is a priority. Since the currents into and out of the decoupling cap are equal and opposite, running these two traces directly over each other provides field cancellation and minimum loop areas where they are needed most.

Figure 13–8 illustrates the difference between a loop that has been routed correctly and one that has not. In this figure, the solid circles represent pads, the schematic symbols show the components that are connected to the pads, and two routing layers are shown with cross–hatching that goes in opposite directions. Note that by routing the two traces one over the other that the critical loop area is minimized.

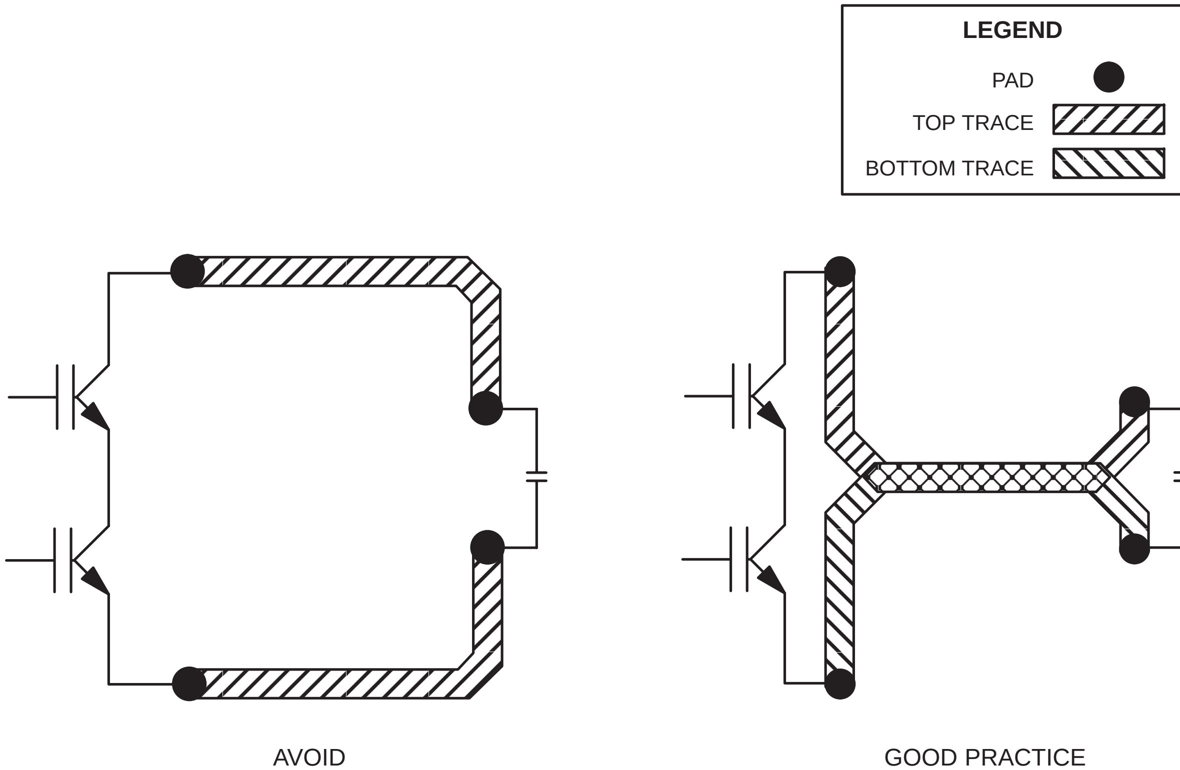


Figure 13–8. Minimizing Loop Areas

For similar reasons it is desirable to run power and return traces one directly on top of the other. In addition, if a current sampling resistor is used in the return, using a surface mount resistor is preferable due to its lower inductance. It also can be placed directly over the power trace, providing uninterrupted field cancellation from placing power and return traces over each other. Again for field cancellation, it is also desirable to run phase outputs parallel and as close as possible to each other.

The power stage is the place where avoiding right angles is most important. Single traces are easy, two forty five degree angles or a curve easily accomplish a 90 degree turn. It is just as important to avoid 90 degree angles in T connections. Figure 13–9 illustrates correct versus incorrect routing for both cases.

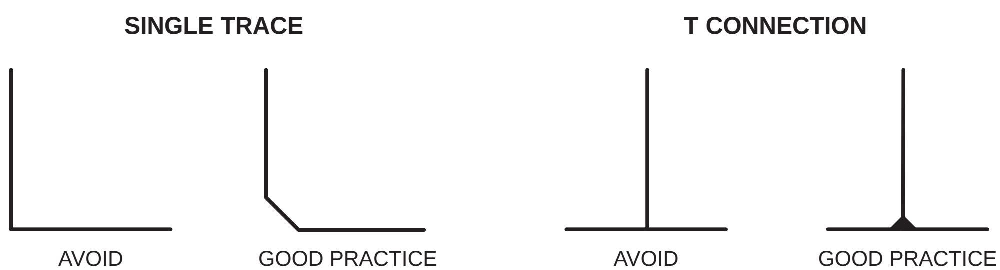


Figure 13–9. 90 Degree Angles

Controllers:

The primary layout issue with controllers is ground partitioning. A good place to start is with the architecture that is shown in Figure 13–10. This architecture has several key attributes. Analog ground and power ground are both separate and distinct from digital ground, and both contact digital ground at only one point. For analog ground it is preferable to make the one point as close as possible to the analog to digital converter's ground reference (VREFL). For power ground the connection should be as close as possible to the microcomputer's power supply return (VSS). Note also that the path from VREFL to VSS is isolated from the rest of digital ground until it approaches VSS.

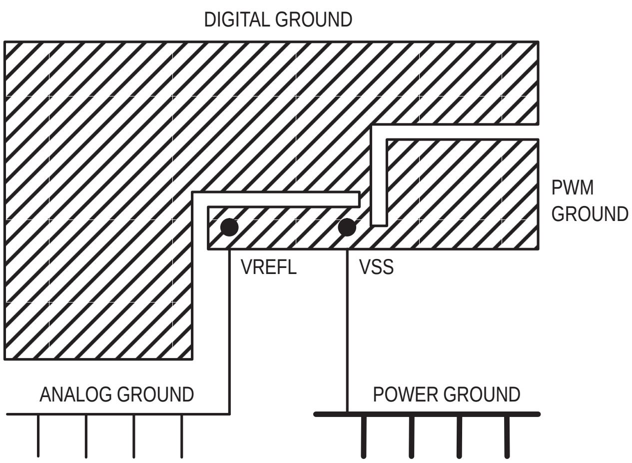


Figure 13–10. Ground Architecture

PWM ground is also isolated as a separate ground plane section until it approaches VSS. This is most important in systems that use opto couplers, since the current that flows through the PWM ground return will be higher than other digital return currents. If a two layer board is used, traces replace the ground planes that are shown in Figure 13–10. The partitioning, however, remains the same.

In addition to grounding, controllers benefit from attention to avoiding 90 degree angles, since there are generally a lot of high speed signals on the digital portion of the board. Routing with 45 degree angles or curves minimizes unwanted reflections, which increases noise immunity.

CONCLUSION

For the most part, the functional architecture of motor drives is much more straightforward than some of the techniques that are required to get them to work. The non–straightforward aspects arise from high levels of both di/dt and dv/dt that produce a lot of noise management design issues. These are systems in which a fraction of a picofarad of stray capacitance in the wrong place, a ground connection that is not carefully routed, or the absence of a functionally not so obvious component will all cause improper operation.

The most important design issues are careful attention to grounding, minimizing critical loop areas, use of series bootstrap resistors, careful attention to power transistor transition times, and filtering sensor inputs. Additional benefits are gained by avoiding 90 degree angles in board layout and cancelling fields by routing equal and opposite current flows as close as possible to each other. As expected, consideration given to these issues up front pays off when it comes to getting a design to work right the first time.

Section 14
Mounting Considerations For Power Semiconductors

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160°C to 135°C.[1] Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.[2] Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic–packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 14–1 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet–metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

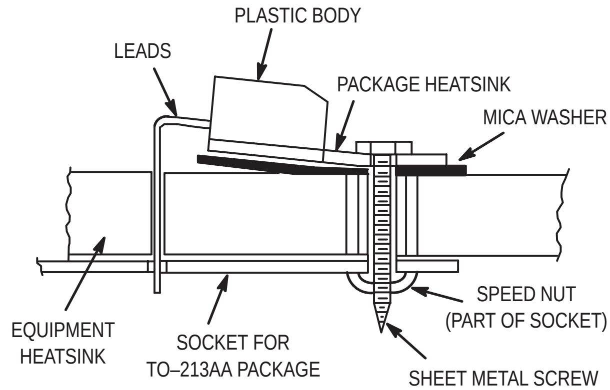


Figure 14–1. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Flange Mount
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high–power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 14–2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

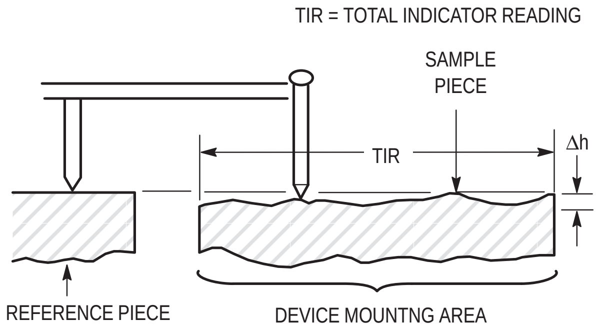


Figure 14–2. Surface Flatness Measurement

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO–204 (TO–3) package with a typical 32–microinch finish, showed that heatsink finishes between 16 and 64 μ–in caused less than ± 2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high–power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromateacid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint’s high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock–marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil™, a dry graphite compound, is shown in the data of Figure 14–3. Grafoil™ is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON–DUX™. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers.

Table 1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal–to–Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In–Lb	Dry	Lubed	Dry	Lubed	Type	See Note
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–213AA (TO–66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO–126	Thermopad™ 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO–220AB	Thermowatt™	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 14–3 and 14–4 for additional data on TO–3 and TO–220 packages.
2. Screw not insulated. See Figure 15–9.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Packages, such as the Motorola Full Pak and HPM modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, are shown in Figure 14–3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 14–3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm™ is a filled polyimide material which is used for isolation (variation of Kapton™). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

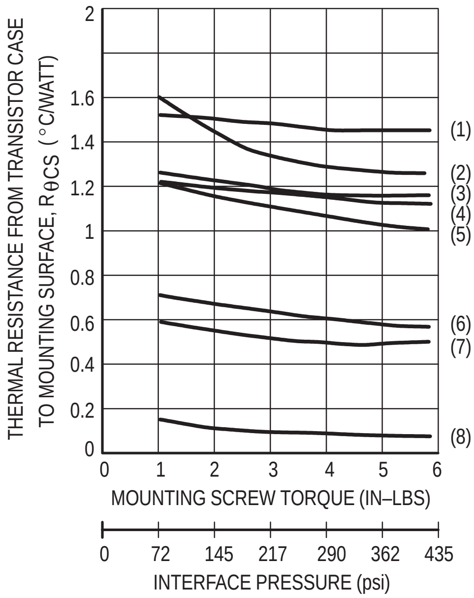
Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton™ or fiberglass. By comparing Figures 14–3c and 14–3d, it can be noted that Thermasil™, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad™ 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber–Duc™, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakekfield	Delta Pad 173–7	.790	1.175
Bergquist	Sil Pad™ K–4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad™ 400–9	.735	1.205
Thermalloy	Thermalsil™ II	.680	1.045
Shin–Etsu	TC–30AG	.664	1.260
Bergquist	Sil Pad™ 400–7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174–9	.574	.755
Bergquist	Sil Pad™ 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil™ III	.440	1.035
Chomerics	1671	.367	.655

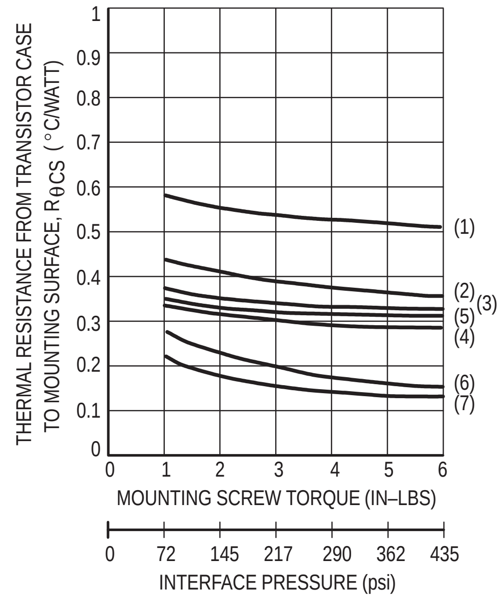
*Test Fixture Deviation from flat from Thermalloy EIR86–1010.



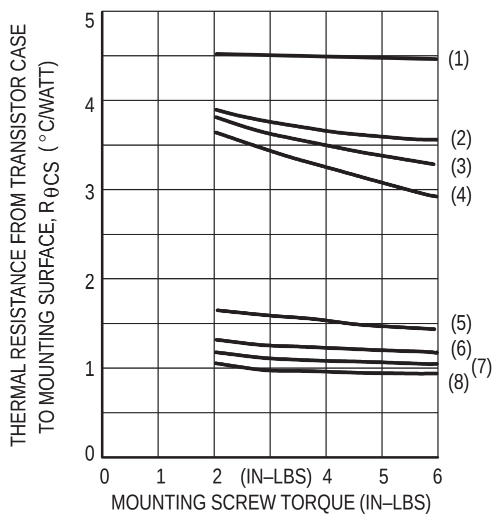
14–3a. TO–204AA (TO–3)
Without Thermal Grease

(1) **Thermalfilm**™, .002 (.05) thick.
(2) **Mica**, .003 (.08) thick.
(3) **Mica**, .002 (.05) thick.
(4) **Hard anodized**, .020 (.51) thick.
(5) **Aluminum oxide**, .062 (1.57) thick.
(6) **Beryllium oxide**, .062 (1.57) thick.
(7) **Bare joint** – no finish.
(8) **Grafoil**™, .005 (.13) thick.*

*Grafoil™ is not an insulating material.



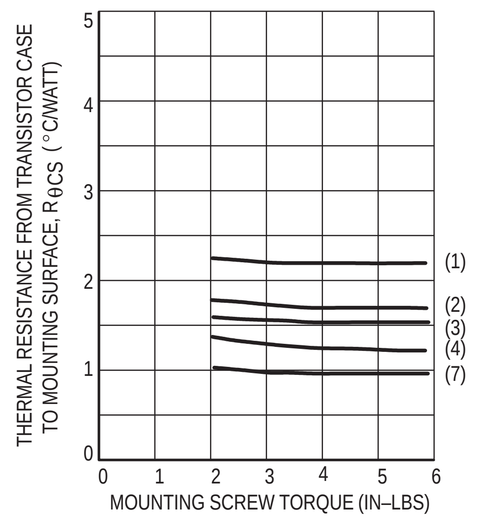
14–3b. TO–204AA (TO–3)
With Thermal Grease



14–3c. TO–220
Without Thermal Grease

(1) **Thermalfilm**™, .002 (.05) thick.
(2) **Mica**, .003 (.08) thick.
(3) **Mica**, .002 (.05) thick.
(4) **Hard anodized**, .020 (.51) thick.
(5) **Thermalsil II**, .009 (.23) thick.
(6) **Thermalsil III**, .007'6 (.15) thick.
(7) **Bare joint** – no finish.
(8) **Grafoil**™, .005 (.13) thick.*

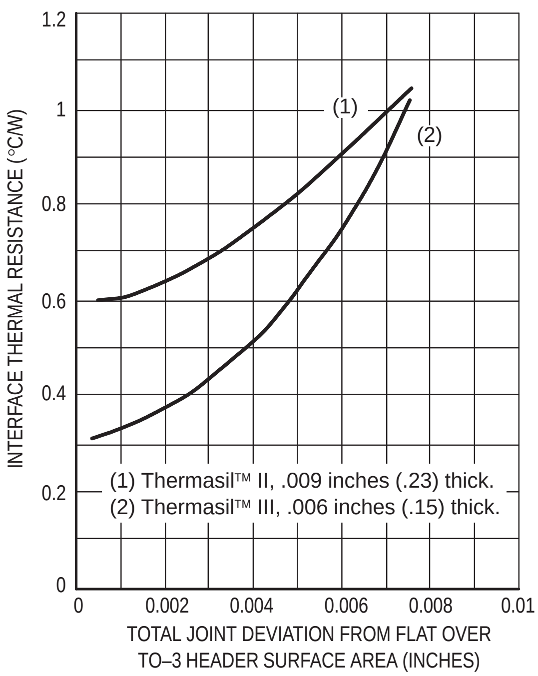
*Grafoil™ is not an insulating material.



14–3d. TO–220
With Thermal Grease

Figure 14–3. Interface Thermal Resistance for TO–204, TO–3 and TO–220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown on Figure 14–4. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil™ lll to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 14–4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho–Therm™ 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 3. Performance of Silicon Rubber Insulators Tested Per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Berquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho–Therm™, 1617	0.233	—
Q Pad™ (non–insulated)	—	0.009
Sil–Pad™, K–10	0.263	0.200
Thermasil™ III	0.267	—
Mica, greased	0.329	0.400
Sil–Pad™ 1000	0.400	0.300
Cho–therm™ 1674	0.433	—
Thermasil™ II	0.500	—
Sil–Pad™ 400	0.533	0.440
Sil–Pad™ K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Berquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950’s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The Power Modules, shown on Figure 14–6c, are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The isolated, Case 221C, illustrated in Figure 14–10, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 14–5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut™, the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.[4]

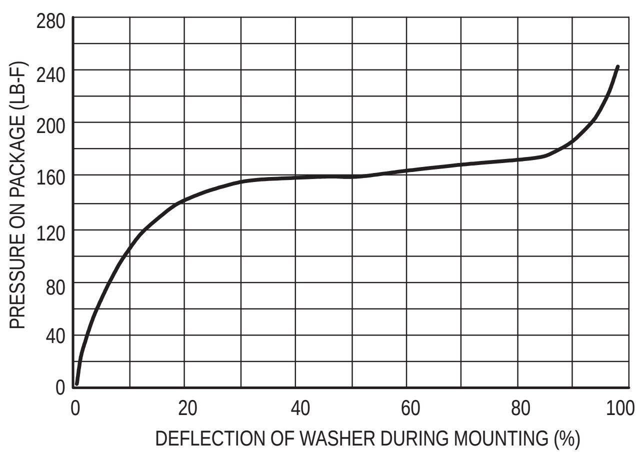


Figure 14–5. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small boardmounted or free–standing heat dissipaters with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or syncnuts) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet–metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange–mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field serviceable systems or low strength types for field serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

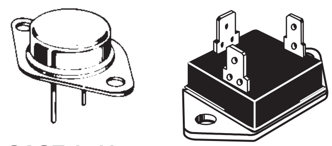
To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel or gold–plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Flange Mount

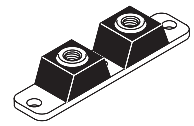
A large variety of parts fit into the flange mount category as shown in Figure 14–6. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 14–7. Machine screws (preferred) self–tapping screws, eyelets, or rivets may be used to secure the package. The aluminum IMS (insulated metal substrate) requires special care during mounting. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. The flatness of the mounting surface should have an overall flatness of 1 mil/inch measured between mounting holes.



CASE 1, 11
TO–204AA
(TO–3)

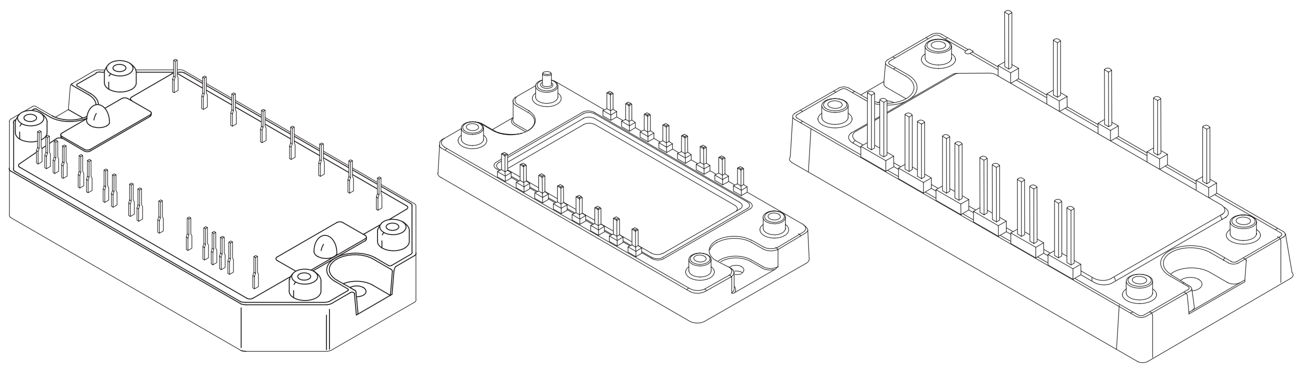
CASE 383–01

14–6a. TO–3 Variations



CASE 357c–03

14–6b. PowerTap™



Cheval™ **VersaPower™** **E–POWER™**

14–6c. Hybrid Power Modules Variations

Figure 14–6. A Large Array of Parts Fit into the Flange–Mount Classification

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 14–8. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 14–9. The rectangular washer shown in Figure 14–9a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch–pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO–220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 14–12c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

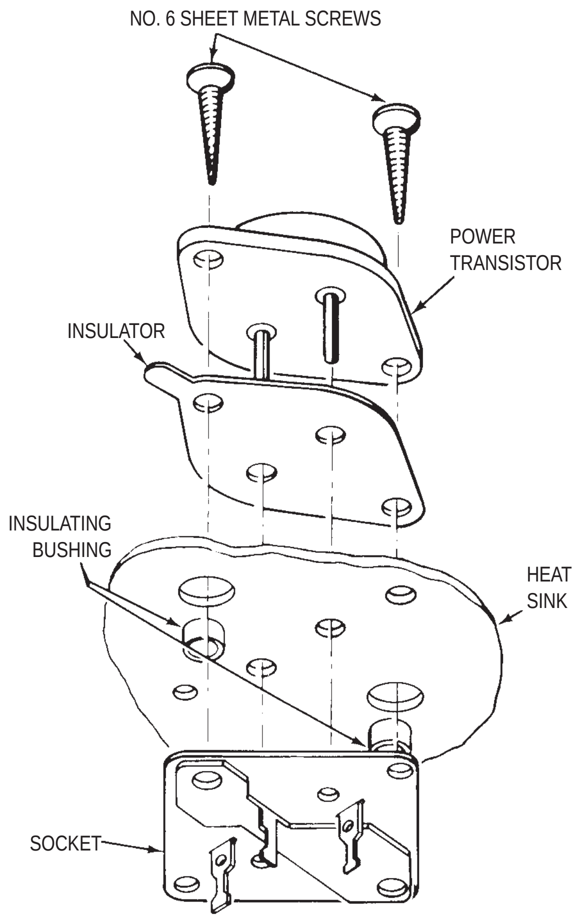


Figure 14–7. Hardware Used for a TO–204AA (TO–3) Flange Mount Part

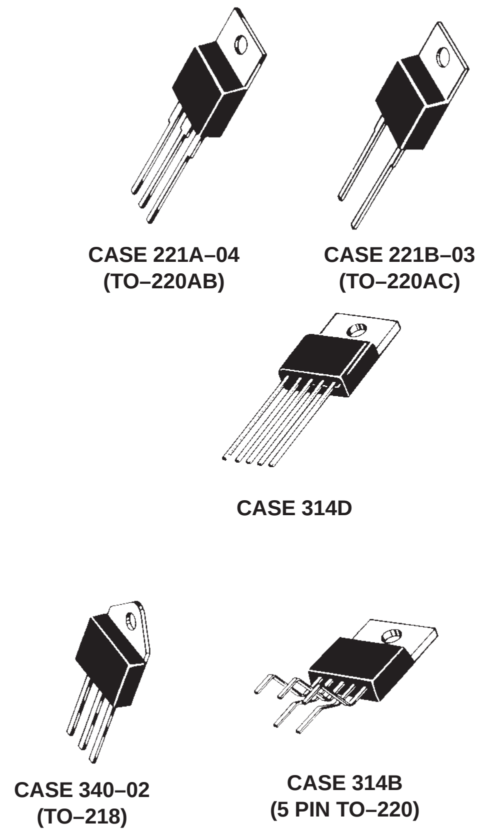


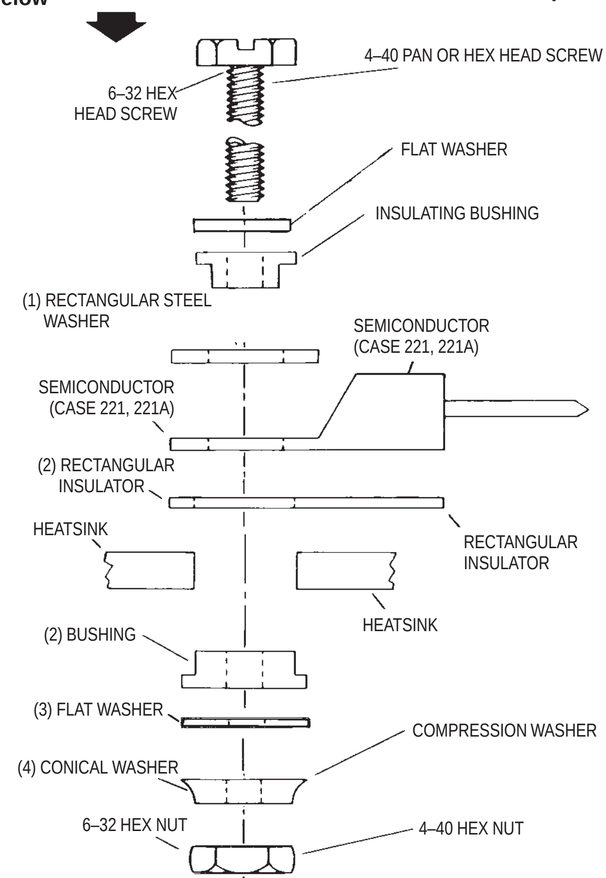
Figure 14–8. Several Types of Tab–Mount Parts

a) Preferred Arrangement for Isolated or Non–isolated Mounting. Screw is at Semiconductor Case Potential. 6–32 Hardware is Used.

Choose from Parts Listed Below

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4–40 Hardware is Used.

Use Parts Listed Below



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 14–9. Mounting Arrangements for Tab Mount TO–220

Plastic Body Mount

The Thermopad™ and isolated plastic power packages shown in Figure 14–10 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad™ (Case 77) parts this is accomplished by die–bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The isolated (Case 221C–02) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.

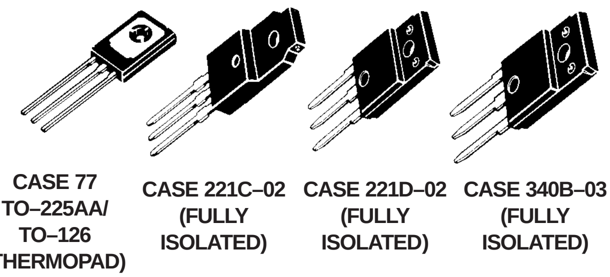


Figure 14–10. Plastic Body–Mount Packages

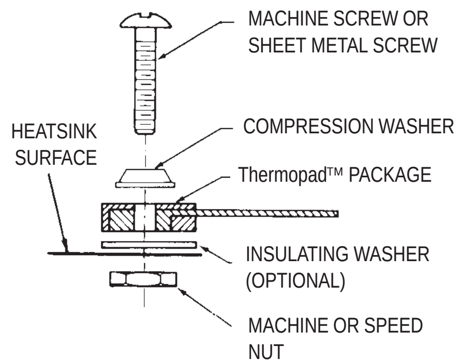
Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 14–5.

Figure 14–11 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

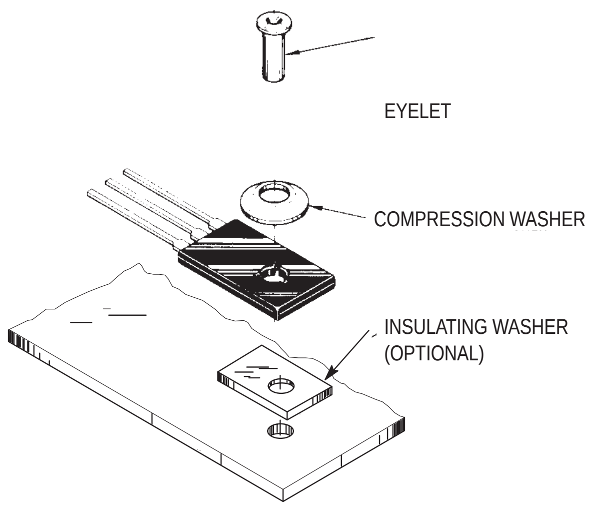
The isolated, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 14–12c, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 14–12b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 14–12a.

Surface Mount

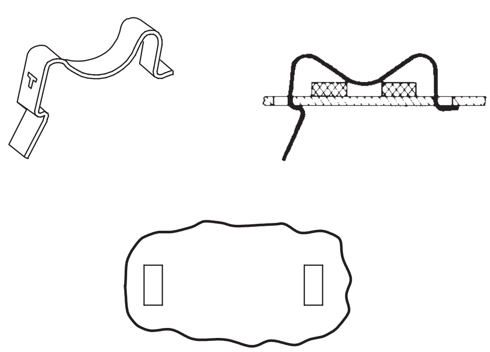
Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 14–13, for example, will accommodate a die up to 102 mils x 140 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.



14–11a. Machine Screw Mounting

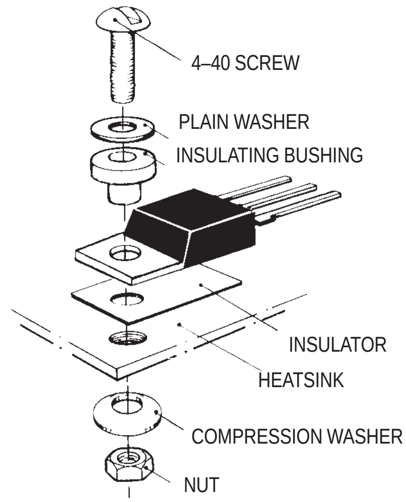


14–11b. Eyelet Mounting

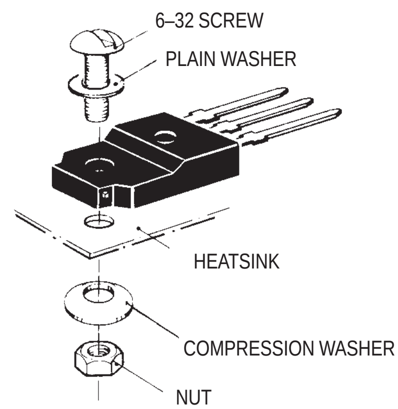


14–11c. Clips

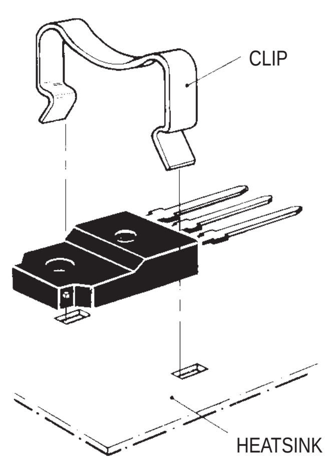
Figure 14–11. Recommended Mounting Arrangements for TO–225AA (TO–126) Thermopad Packages



14–12a. Screw–Mounted TO–220



14–12b. Screw–Mounted Isolated Package



14–12c. Clip–Mounted Isolated Package

Figure 14–12. Mounting Arrangements for the Isolated Package as Compared to a Conventional TO–220

CASE 369–07 **CASE 369A–13**

Figure 14–13. DPAK Parts

Standard Glass–Epoxy 2–ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 14–14 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.[7] The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

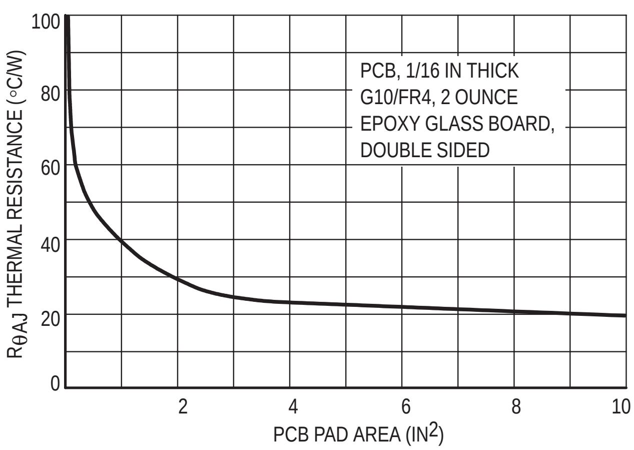
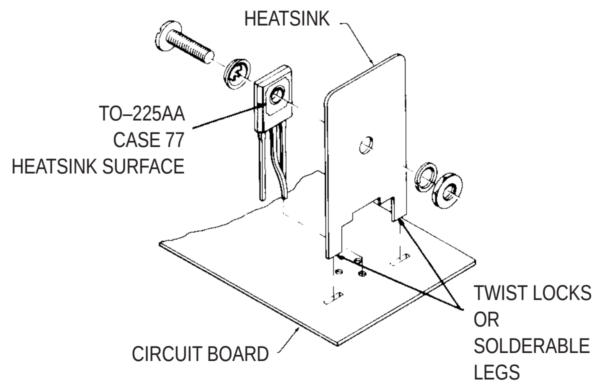


Figure 14–14. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board

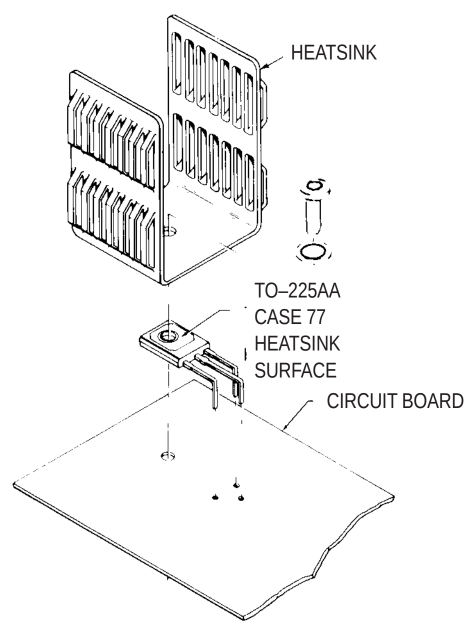
FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO–225AA) (TO–127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 14–15. The arrangement of part (14a) could be used with any plastic package, but the scheme of part (14b) is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.



14–15a. Simple Plate, Vertically Mounted



14–15b. Commercial Sink, Horizontally Mounted

Figure 14–15. Methods of Using Small Heatsinks With Plastic Semiconductor Packages

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal and plastic packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

Modules

The screw terminals of the power modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO–225AA (CASE 77) and 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire–wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol is generally satisfactory for use with plastic devices, since it does not damage the package.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, such as switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction–to case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

[1] MIL–HANDBOOK — 2178, SECTION 2.2.
[2] “Navy Power Supply Reliability — Design and Manufacturing Guidelines” NAVMAT P4855–1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
[3] Catalog #87–HS–9, (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.
[4] ITW Shakeproof, St. Charles Road, Elgin, IL 60120.
[5] Robert Batson, Elliot Fraunglass and James P Moran, “Heat Dissipation Through Thermalloy Conductive Adhesives,” EMTAS ’83. Conference, February 1 – 3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.
[6] Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.
[7] Herb Fick, “Thermal Management of Surface Mount Power Devices,” Powerconversion and Intelligent Motion, August 1987.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D\,(R_{\theta JC} + P_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
P_D = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat–sink),
$R_{\theta SA}$ = heat sink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

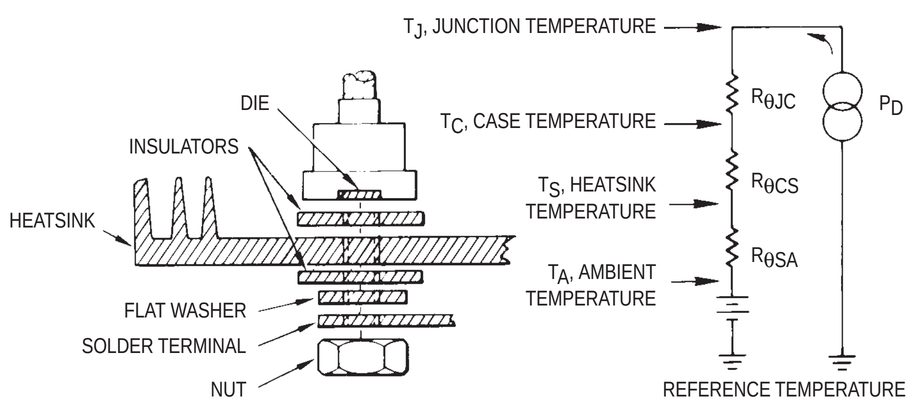


Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

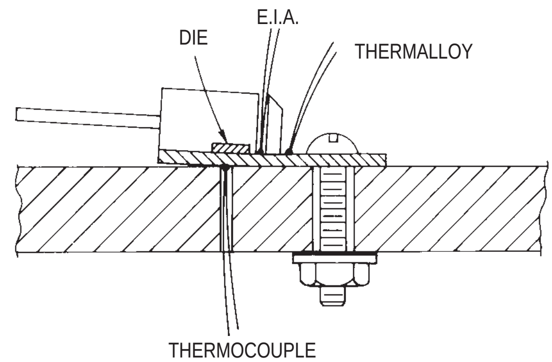


Figure B1. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 µ–inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application–oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C

Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber		
Aavid Eng.	—	—	—	—	—	—	X	X	X	X
AHAM–TOR	—	—	—	—	—	—	—	—	X	—
Asheville–Schoonmaker	—	—	—	—	—	X	—	—	—	—
Astrodynamis	X	—	—	—	—	—	—	—	X	—
Delbert Blinn	—	—	X	—	X	X	X	X	X	—
IERC	X	—	—	—	—	—	—	—	X	—
Staver	—	—	—	—	—	—	—	—	X	—
Thermalloy	X	X	X	X	X	X	X	X	X	X
Tran–tec	X	—	X	X	X	X	—	X	X	—
Wakefield Eng.	X	X	X	—	X	—	—	X	X	X

Other Sources for silicone rubber pads: Chomerics, Berquist

Suppliers Addresses

Aavid Engineering, Inc., P.O. Box 400, Laconia, New Hampshire 03247 (603) 524–1478

AHAM–TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676–4151

Asheville–Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607 (804) 244–7311

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935–4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835–2322

Chomerics, Inc.,16 Flagstone Drive, Hudson, New Hampshire 03051 1–800–633–8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 623–1257

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849–2481

The Staver Company, Inc., 41–51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666–8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243–4321

Tran–tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564–2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245–5900

Section 15
Basic Semiconductor Thermal Measurement

INTRODUCTION

This paper will provide the reader with a basic understanding of power semiconductor thermal parameters, how they are measured, and how they are used. With this knowledge, the reader will be able to better describe power semiconductors and answer many common questions relating to their power handling capability.

This paper will cover the following key topics.

- Understanding basic semiconductor thermal parameters.
- Semiconductor thermal test equipment.
- Thermal parameter test procedures.
- Using thermal parameters to solve often asked thermal questions.

UNDERSTANDING BASIC SEMICONDUCTOR THERMAL PARAMETERS

Heat flows from a higher to a lower temperature region. The quantity that resists or impedes this flow of heat energy is called thermal resistance or thermal impedance.

When the quantity of heat being generated by a device is equal to the quantity of heat being removed from it, a steady state condition is achieved.

To describe the thermal capability of a device, several key parameters and terms are used. They describe the steady state thermal capability of a power semiconductor device.

Key Parameters, Terms, and Definitions

T_J = *junction* temperature
T_C = *case* temperature
T_A = *ambient* temperature
TSP = **T**emperature **S**ensitive **P**arameter
T_R = *reference* temperature (i.e., *case* or *ambient*)
$R_{\theta JR}$ = junction–to–*reference* thermal resistance
$R_{\theta JC}$ = junction–to–*case* thermal resistance
$R_{\theta JA}$ = junction–to–*ambient* thermal resistance
$R_{\theta JR(t)}$ = junction–to–*reference* transient thermal resistance
P_D = power dissipation

The thermal behavior of a device can be described, for practical purposes, by an electrical equivalent circuit. This circuit consists of a resistor–capacitor network as shown in Figure 15–1.

Resistors R1, R2, and R3 are all analogous to individual thermal resistance, or quantities that impede heat flow.

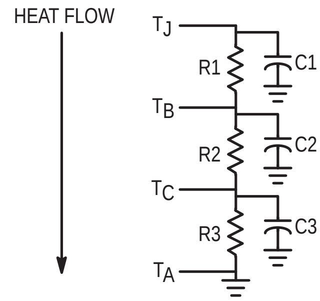


Figure 15–1. Thermal Electrical Equivalent Circuit

Heat generated in a device's junction flows from a higher temperature region through each resistor–capacitor pair to a lower temperature region.

Resistor R1 is the thermal resistance from the device's junction to its die–bond. Resistor R2 is the thermal resistance from the die–bond to the device's case. Resistor R3 is the thermal resistance from the device's case to ambient. The thermal resistance from the junction to some reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance $R_{\theta JC}$ from junction–to–case is equal to the sum of resistors R1 and R2. The thermal resistance $R_{\theta JA}$ from junction–to–ambient, therefore, is equal to the sum of resistors R1, R2 and R3.

The capacitors shown help model the transient thermal response of the circuit. When heat is instantaneously applied and or generated, there is a charging effect that takes place. This response follows an RC time constant determined by the resistor–capacitor thermal network. Thermal resistance, at a given time, is called transient thermal resistance, $R_{\theta JR(t)}$.

To further understand transient thermal response, refer to Motorola Application Note AN569, "Transient Thermal Resistance — General Data And Its Use." [4] A detailed discussion of this will not be included here.

Using the key parameters and terms shown earlier, only a few equations are necessary to solve often asked thermal questions.

$$R_{\theta JR} = (T_J - T_R) \ / \ \text{power} \quad (1)$$
$$P_D = (\text{max. device temperature} - T_R) \ / \ R_{\theta JR} \quad (2)$$
$$T_J = P_D * R_{\theta JR} + T_R \quad (3)$$

SEMICONDUCTOR THERMAL TEST EQUIPMENT

The procedure used determines the test equipment needed for measurement. Below you will find the equipment used for both a manual and an automated approach to thermal measurement.

Manual technique:

Power supply	*(supplies power to the device under test)*
Thermocouple	*(measures T_R)*
Multimeter	*(measures current and voltage)*
Heat exchanger	*(needed to mount device to and remove heat)*
Chiller	*(needed to remove heat from device)*
Test fixture	*(provides power and sampling pulse train)*

Automated systems available:

Analysis Tech	*(Phase 6, 7, 8, and 9)*
Sage	*(Star 150)*
TESEC	*(DV240)*

The automated systems shown above each provide different levels of automation. Analysis Tech has the most complete automation and TESEC the least. One nice feature of the Analysis Tech system is that it will output the 3 resistor–capacitor values for the electrical equivalent circuit. These values are very useful for modeling the thermal effects in computer simulation software such as SPICE. The level of automation you need depends both on your thermal measurement goals and available budget.

The main advantages of an automated approach are:

- Ease of use
- Less operator dependence on measurement
- Consistency
- Accuracy
- System network capability for data transfer

THERMAL PARAMETER TEST PROCEDURE

The basic procedure for measuring thermal parameters is as follows:

1) Calibrate the TSP (Temperature Sensitive Parameter).
2) Apply continuous power and TSP sampling pulses.
3) Measure T_J, T_R, and applied test power.
4) Calculate thermal resistance, $R_{\theta J(R)}$, and Maximum Power, P_D.

Calibrating the TSP, Temperature Sensitive Parameter

Since it is basically impossible to put a physical thermometer onto a device's junction to measure its temperature while under power, we must find another approach. Fortunately, we can use the device's forward junction voltage to tell us its temperature. The forward voltage drop of a diode's pn junction has a very linear relationship with temperature. We can use this relationship to tell us what the junction temperature is under any power condition.

To determine the actual voltage temperature relationship of a TSP for a given device, simply calibrate the TSP at a constant sense current over temperature as shown in Figure 15–2. The TSP sense current used should be small so as to not cause additional heating during calibration.

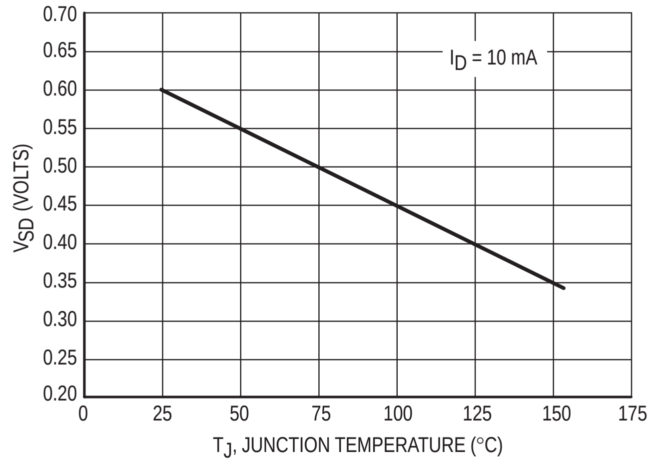


Figure 15–2. Typical Temperature Calibration Curve for a TMOS™ Body Diode

The forward voltage drop of a MOSFET body diode decreases linearly over temperature at rate of about 2 millivolts per degree Celsius when measured at a sense current of 10 mA.

Other device electrical parameters have similar linear relationships to temperature as well. The following are several other temperature sensitive parameters used in the industry to determine a device's junction temperature.

Common TSP	Device Type
V_{th}, $V_{DS(on)}$, $R_{DS(on)}$	MOSFET
V_{th}, $V_{CE(sat)}$	IGBT
V_{BE}, $V_{CE(sat)}$	Bipolar
V_F	Diode

Make sure to develop the actual electrical to thermal correlation of the TSP and check it for linearity prior to its use. The linearity of this parameter is critical for accurate thermal measurement.

Applying Continuous Power and TSP Sampling Pulses

With a properly chosen and calibrated TSP, we can now provide test signals to the device and make thermal measurements.

We begin by applying a continuous power of known current and voltage to the device. A continuous train of sampling pulses monitors the TSP, and thus the junction temperature. The TSP sampling pulse must provide a sense current equal to that used during calibration. While monitoring the TSP, adjust the applied power so as to insure a sufficient rise in T_J. Adjusting the applied power to achieve a T_J rise of about 100° above the reference temperature will generate enough temperature delta to insure good measurement resolution.

The TSP sample time must be very short so as to not allow for any appreciable cooling of the junction prior to re–applying power. The power and sample pulse train shown in Figure 15–3 has a duty cycle of 99.9% which for all practical purposes is considered continuous power.

Obviously, with this much power being applied to the device under test, the device's case will get very hot. To keep the

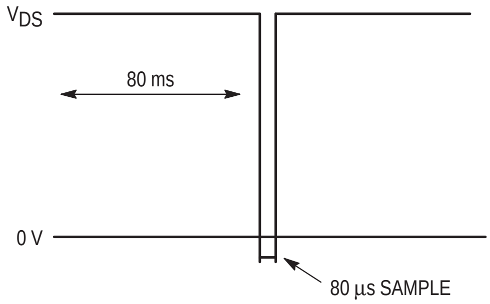


Figure 15–3. Example of a Power and Sample Pulse Train During $R_{\theta JC}$ Measurement of a TMOS Device

A continuous pulse train consisting of an 80 ms power pulse followed by an 80 µs diode sample is used to apply both power to the device as well as a sample pulse for TSP measurement.

device cool while under test, we need to mount it to a heat sink of some sort. A heat exchanger with chilled water flowing through it provides a good heat sink. In this way, we can keep the device's case temperature down (i.e., near 25°C) and maintain good measurement resolution (i.e., large temperature delta between the junction and reference location).

Measuring T_J, T_R, and Applied Power

After T_J has stabilized, we must record its value along with the reference temperature, T_R, and applied power. To calculate the devices maximum power rating, P_D, and thermal resistance, $R_{\theta JR}$, we need to have these measurements.

The devices junction temperature, T_J, is taken from the TSP electrical measurement. With the correlation between the TSP electrical measurement and temperature already established, determining T_J is pretty much straightforward.

A thermocouple placed at the reference location measures the reference temperature, T_R. Most power semiconductor manufacturer's use the devices' case, however, the lead, ambient, or all three can be used as reference locations.

Key elements to insure accurate reference temperature measurement are:

- Good thermocouple to reference contact
- Consistent thermocouple placement location

The reference thermocouple needs to make a good thermal contact to its reference location. This applies to reference locations other than ambient. Without a good thermal contact, measurement error will occur. To improve this contact, use both thermal grease and device clamping pressure.

Use thermal grease to insure good thermal conductivity and to eliminate air gaps. Applying thermal grease between the device and the heat sink used to keep the case temperature near 25°C will help in two ways. First, it will help keep the case temperature down during measurement by improving the thermal contact to the heat sink. Second, it will also improve the thermocouple to case contact as well. As stated earlier, the case is usually used as the reference location for thermal measurements. Thermal grease helps to maintain good thermal contact and insure measurement accuracy.

Applying about 85 to 90 PSI between the thermocouple and the reference location (i.e., device's case) also improves the thermal contact as shown in Figure 15–4. The application of pressure to the device seems to smooth out thermal grease thickness variations and eliminate air gaps at the contact interface.

Taking these precautions into consideration will help insure a good thermal contact to the reference location surface (i.e., device case).

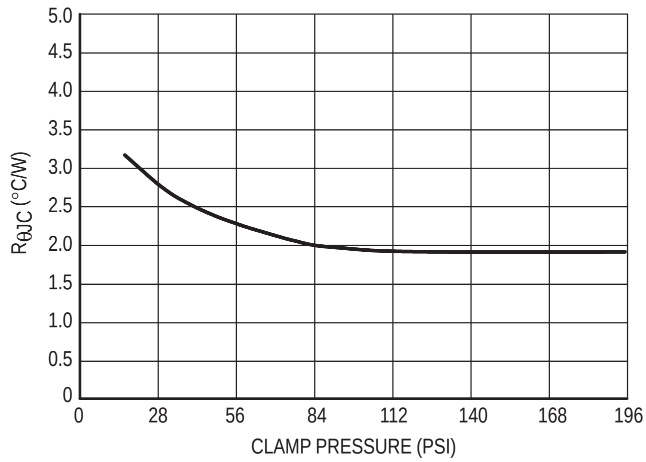


Figure 15–4. $R_{\theta JC}$ versus Clamp Pressure

The value of measured thermal resistance drops and becomes consistent at about 85–90 PSI insuring good thermal contact between the thermal couple and the devices case. [1]

The reference thermocouple needs to be placed at the same location for every device. Any change in the placement of this thermocouple will result in error or at the very least inconsistencies between measurements. A different thermal resistance exists between the junction and the location of each thermocouple placement. Usually for the best readings, the reference thermocouple should be placed at the hottest location on the package (i.e. for TO–220 devices, at the center of the die on the back side of the devices metal case). In any event, to be accurate and consistent, always place the reference thermocouple in the same location for each device measured.

Calculating Thermal Resistance, $R_{\theta J(R)}$, and Maximum Power, P_D

We can use equations (1) and (2) presented earlier, along with our measurements, to calculate the devices thermal resistance and maximum power capability.

Assuming we measured the following: T_J = 100°C, applied test power = 50 W, T_C = 25°C, and maximum device temperature rating = 150°C, we use equation (1) to calculate $R_{\theta JC}$.

$$R_{\theta JC} = (100 - 25)/50$$
$$= 1.5°C/W \text{ (measured value)}$$

Most manufacturer's will guardband the measured $R_{\theta JR}$ reading to establish their device limits. This helps take into consideration all of the variables involved which cause inconsistencies in readings. A guardband of 25% for thermal measurements is considered good practice.

Multiplying the measured thermal resistance from above by 1.25 to guardband it by 25%, we get the following specified $R_{\theta JC}$.

$R_{\theta JC} = 1.5 * 1.25$
$= 1.9°C/W$ (manufacturer's guaranteed limit)

As shown in Figure 15–5, the thermal resistance from junction to case is largely dependent on the die size of the device. This implies that silicon has a much larger thermal resistance, or opposition to heat flow, than that of the copper header to which it is bonded to.

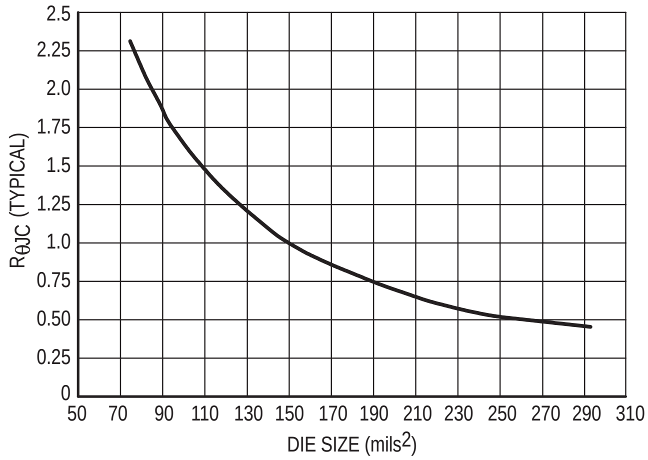


Figure 15–5. $R_{\theta JC}$ versus Die Size for TMOS™ Devices in TO–220, D^2PAK, DPAK & TO–247 Packages

To determine a devices power handling capability, P_D, we use the specified $R_{\theta JC}$ taken from above along with equation (2).

$P_D = (150 – 25)/1.9$
$= 66$ W (manufacturer's guaranteed limit)

USING THERMAL PARAMETERS TO SOLVE OFTEN ASKED THERMAL QUESTIONS

One can use measured or specified thermal parameters to solve many common questions asked about power semiconductor devices. The two examples shown below use thermal parameters to solve frequently asked questions.

Example #1

Calculate the device's junction temperature: Using equation (3) with a known $R_{\theta JC}$ of 1.25°C/W, case temperature of 85°, and applied power of 35 W.

$T_J = 35 * 1.25 + 85$
$= 128.8°C$

Example #2

Calculate the power handling capability: Using equation (2) with a known $R_{\theta JC}$ of 1.0°C/W, a starting case temperature of 75°C and a maximum rated T_J of 150°C.

$P_D = (150 – 75)/1.0$
$= 75$ W

SUMMARY

This paper presents a description of basic semiconductor thermal measurement as well as the use of thermal data in real world examples. Included are terms, definitions, equations and test equipment required. This provides the reader with information useful in answering many common questions regarding the basic thermal capabilities of power semiconductor devices.

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[4] Roehr, Bill and Bryce Shiner. "Transient Thermal Resistance — General Data and its Use," AN569 in Motorola *Power Applications Manual,* 1990: (23–38), Motorola Literature Distribution Center, Ph. #1 (800) 441–2447.

Section 16
Reliability and Quality

INTRODUCTION

In today's semiconductor marketplace two important elements for the success of a company are product quality and reliability. Both are interrelated — reliability is the quality extended over the expected life of the product. For any manufacturer to remain in business, their products must meet and/or exceed the basic quality and reliability standards. Motorola, as a semiconductor supplier, has successfully achieved these standards by supplying product for the most strenuous applications to perform in the most adverse environments.

It is recognized that the best way to accomplish an assured quality performance is by moving away from the previous methods of "testing in" quality and embracing the newer concept of "building in" quality. At Motorola, we use a twofold approach toward reaching the ultimately achievable level of quality and reliability. First, we develop and implement a process that is inherently reliable. Then we exercise meticulous care in adhering to the specifications of the process every step of the way — from start to finish. This allows the development and application of inspections and procedures that will uncover potentially hidden failure modes. It is this dedication to long–term reliability that will ultimately lead to the manufacture of the "perfect product."

Motorola approaches the ideal in IGBT product reliability by instigating a four–step program of quality and reliability:

1. Stringent in–process controls and inspections.
2. Thoroughly evaluated designs and materials.
3. Process average testing, including 100% QA redundant testing.
4. Ongoing reliability verifications through audits and reliability studies.

These quality and reliability procedures, coupled with rigorous incoming inspections and outgoing quality control inspections add up to a product with quality built in — from raw silicon to delivered service.

RELIABILITY TESTS

Motorola IGBT's are subjected to a series of extensive reliability tests to verify conformance. These tests are designed to accelerate the failure mechanisms encountered in practical applications, thereby ensuring satisfactory reliable performance in "real world" applications.

The following describes the reliability tests that are routinely performed on Motorola's IGBT's.

High Temperature Reverse Bias (HTRB):
Per MIL–STD–750, Method 1039.

The HTRB test is designed to check the stability of the device under "reverse bias" conditions of the main blocking junction at high temperature, as a function of time.

The stability and leakage current over a period of time, for a given temperature and voltage applied across the junction, is indicative of junction surface stability. It is therefore a good indicator of device quality and reliability.

For IGBT's, voltage is applied between the collector and emitter with the gate shorted to the emitter. I_{CES}, $V_{(BR)CES}$, I_{GES}, $V_{GE(th)}$, and $V_{CE(on)}$ are the dc parameters monitored. A failure will occur when the leakage achieves such a high level that the power dissipation causes the devices to go into a thermal runaway. The leakage current of a stable device should remain relatively constant, only increasing slightly over the testing period.

Typical conditions:
V_{CE} = 100% of maximum rating
V_{GE} = 0V (shorted)
T_A = 150°C
Duration: 1000 hrs for qualification

High Temperature Gate Bias (HTGB):
Per MIL–STD–750, Method 1039.

The HTGB test is designed to electrically stress the gate oxide at the maximum rated dc bias voltage at high temperature. The test is designed to detect for drift caused by random oxide defects and ionic oxide contamination.

For IGBTs, voltage is applied between the gate and emitter with the collector shorted to the emitter. I_{GES}, $V_{GE(th)}$, and $V_{CE(on)}$ are the dc parameters monitored. Any oxide defects will lead to early device failures.

Typical conditions:
V_{GE} = ±20 V
V_{CE} = 0 (shorted)
T_J = 150°C
Duration: 1000 hrs for qualification

High Temperature Storage Life (HTSL) Test:
Per MIL–STD–750, Method 1032.

The HTSL test is designed to indicate the stability of the devices, their potential to withstand high temperatures and the internal manufacturing integrity of the package. Although devices are not exposed to such extreme high temperatures in the field, the purpose of this test is to accelerate any failure mechanisms that could occur during long periods at storage temperatures.

The test is performed by placing the devices in a mesh basket, then placed in a high temperature chamber at a controlled ambient temperature, as a function of time.

Typical conditions:
T_A = 150°C on Plastic package
Duration: 1000 hrs for qualification

High Humidity High Temperature Reverse Bias (H^3TRB) Test: Per MIL–STD–750, Method 1039.

The H^3TRB test is designed to determine the resistance of component parts and constituent materials to the combined deteriorative effects of prolonged operation in a high temperature/high humidity environment. This test only applies to nonhermetic devices.

Humidity has been a traditional enemy of semiconductors, particularly plastic packaged devices. Most moisture related degradations result, directly or indirectly, from penetration of moisture vapor through passivating materials, and from surface corrosion. At Motorola, this former problem has been effectively addressed and controlled through use of junction "passivation" process, die coating, and proper selection of package materials.

Typical conditions:
- V_{CE} = 100% of maximum rating
- V_{GE} = 0 (shorted)
- T_A = 85°C
- RH = 85%
- Duration: 1000 hrs for qualification

Autoclave Test (Pressure Cooker).

The Autoclave Test is designed to determine the moisture resistance of devices by subjecting them to high steam pressure levels. This test is only performed on plastic/epoxy encapsulated devices and not on hermetic packages (i.e., metal can devices). Within the pressure cooker a wire mesh tray is constructed inside to keep the devices approximately two inches above the surface of deionized water and to prevent condensed water from collecting on them. After achieving the proper temperature and atmospheric pressure, these test conditions are maintained for a minimum of 24 hours. The devices are then removed and air dried. Parameters that are usually monitored are leakage currents and voltage.

Typical conditions:
- T_A = 121°C
- P = 14.7 psi
- RH = 100%
- Duration: 72 hrs for qualification

Intermittent Operating Life:
(IOL or Power Cycling) Per MIL–STD–750, Method 1037.

The purpose of the IOL test is to determine the integrity of the chip and/or package assembly by cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied) as is normally experienced in a "real world" environment.

DC power is applied to the device until the desired function temperature is reached. The power is then switched off, and forced air cooling applied until the junction temperature decreases to ambient temperature.

$$\Delta T_J = \Delta T_C + R_{\theta JC} P_D$$
$$\Delta T_J = 100°C$$
(typically, which is an accelerated condition)
$$\Delta T_C = T_{C\ HIGH} - T_{C\ LOW}$$

The sequence is repeated for the specified number of cycles. The temperature excursion is carefully maintained for repeatability of results.

The Intermittent Operating Life test indicates the degree of thermal fatigue of the die bond interface between the chip and the mounting surface and between the chip and the wire bond interface.

For IGBT's, parameters used to monitor performance are thermal resistance, threshold voltage, on–resistance, gate–emitter leakage current and collector–emitter leakage current.

A failure occurs when thermal fatigue causes the thermal resistance or the on–resistance to increase beyond the maximum value specified by the manufacturer's data sheets.

Typical conditions:
- $V_{GE} \geq 10$ V
- ΔT_J = 100°C
- $R_{\theta JC}$ = Device dependent
- T_{on}, $T_{off} \geq 30$ seconds
- Duration: 15K cycles for qualification

Temperature Cycle (TC) Per MIL–STD–750, Method 1051.

The purpose of the Temperature Cycle Test is to determine the resistance of the device to high and low temperature excursions in an air medium and the effects of cycling at these extremes.

The test is performed by placing the devices alternatively in separate chambers set for high and low temperatures. The air temperature of each chamber is evenly maintained by means of circulation. The chambers have sufficient thermal capacity so that the specified ambient is reached after the devices have been transferred to the chamber.

Each cycle consists of an exposure to one extreme temperature for 15 minutes minimum, then immediately transferred to the other extreme temperature for 15 minutes minimum; this completes one cycle. Note that it is an immediate transfer between temperature extremes and thereby stressing the device greater than non–immediate transfer.

Typical Extremes

–65/+150°C

The number of cycles can be correlated to the severity of the expected environment. It is commonly accepted in the industry that ten cycles is sufficient to determine the quality of the device.

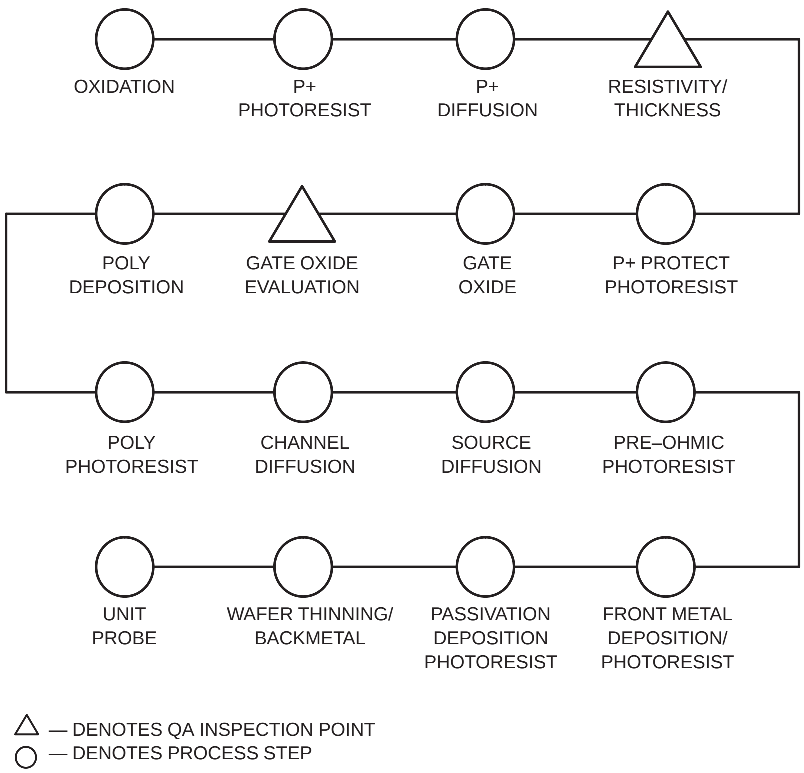
Typical Cycles for Evaluations

TO–220 and TO–247 devices: Minimum 100 cycles

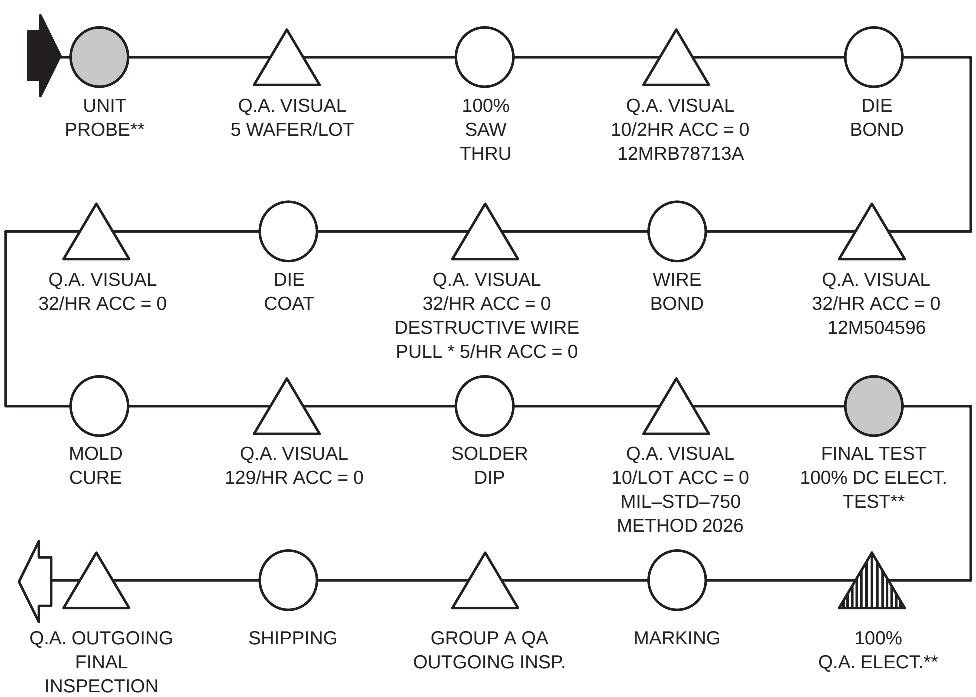
TO–220 and TO–247 devices: Maximum 1000 cycles

Temperature cycling identifies any excessive strains set up between materials within the device due to differences in coefficients of expansion.

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short."



IGBT WAFER FABRICATION



*100% NON–DESTRUCTIVE WIRE PULL AFTER WIRE BOND
**100% DC ELECTRICAL TESTING

— DENOTES QA INSPECTION POINT
— DENOTES PROCESS STEP

ASSEMBLY PROCESS FLOW

Environmental Package Related Test Programs:

A. Physical Dimensions — MIL–STD–750, Method 2066. This test is performed to determine the conformance to device outline drawing specifications.
B. Visual and mechanical examination — MIL–STD–750, Method 2071. A test to determine the acceptability of product to certain cosmetic and functional criteria such as marking legibility, stains, etc.
C. Resistance to Solvents — MIL–STD–202, Method 2025.3. A test to determine the solderability of device terminals.
D. Terminal Strength — MIL–STD–750, Method 2036. This test is a lead bend test to check for lead strength.
E. Constant Acceleration — MIL–STD–750, Method 2006. The parts are accelerated to 20,000 G's and higher to check for defects that would show up in this environment.
F. Vibration Variable Frequency — MIL–STD–750, Method 2056. Parts are vibrated in different planes and at different frequencies to check for loose particles or ruptured wire or die bonds.

Every manufacturing process exhibits a quality and reliability distribution. This distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

Accelerated Stress Testing

The nature of some tests in this report is such that they far exceed that which the devices would see in normal operating conditions. Thus, the test conditions "accelerate" the failure mechanisms in question and allow Motorola to predict failure rates in a much shorter amount of time than otherwise possible. Failure modes that are temperature dependent are characterized by the Arrhenius model.

$$AF = \frac{EA}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)$$

AF = Acceleration Factor
EA = Activation Energy (ev)
K = Boltzman's Constant (8.62 x 10^{-5} ev/°K)
T_2 = Operating Temperature (°K)
T_1 = Test Temperature (°K)

Therefore, the equivalent device hours are equal to the acceleration factor (as determined by the Arrhenius Model) times the actual device hours.

With the following charts (Figures 16–1, 16–2), one can determine a temperature dependent failure rate for our power MOSFETs under reverse and gate bias conditions when establishing their design circuits. For example, if the established operating temperature is set at 50°C, the charts show the failure rates to be 1 and 680 fits for high temperature reverse bias and high temperature gate bias, respectively.

Review of Data

High Temperature Reverse Bias (HTRB) indicates the stability of leakage current, which is related to the field distortion of IGBT's. HTRB enhances the failure mechanism by high temperature reverse bias testing, and therefore is a good indicator of device quality and reliability, along with verification that process controls are effective.

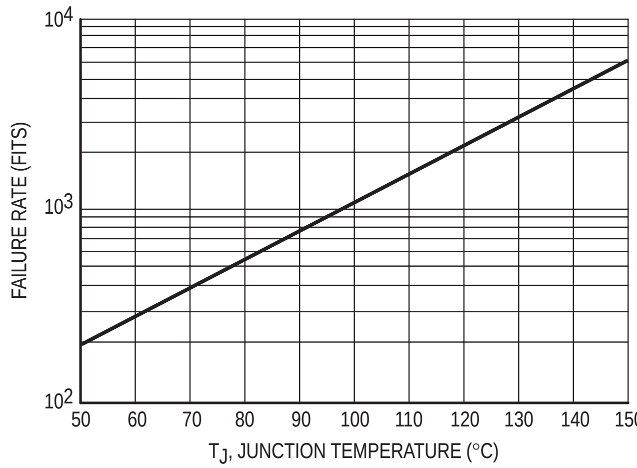


Figure 16–1. High Temperature Reverse Bias Failure Rate versus Junction Temperature

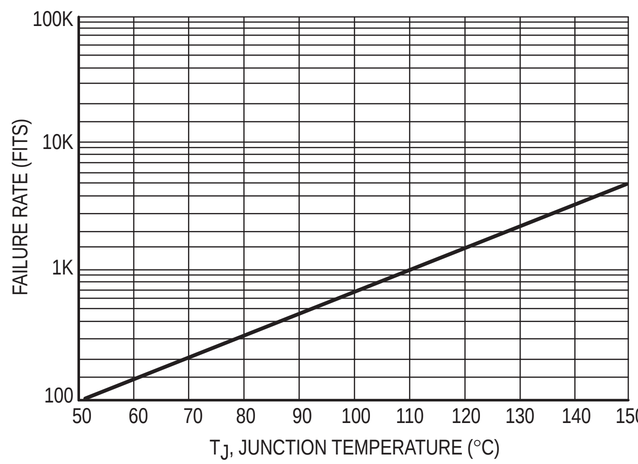


Figure 16–2. High Temperature Gate Bias Failure Rate versus Junction Temperature

High Temperature Gate Bias (HTGB) checks the stability of the device under "gate bias" forward conditions at accelerated high temperature, as a function of time. This test is performed to electrically stress the gate oxide to detect for drift caused by random oxide defect. This failure mechanism appears in the infant and random zones of the reliability "bath tub curve" at a very low rate of defect.

Intermittent Operating Life (IOL) is an excellent accelerated stress test to determine the integrity of the chip and/or package assembly to cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied). This test is perhaps the most important test of all, along with simulating what is normally experienced in a "real world" environment. IOL exercises die bond, wire bonds, turning on the device, turning off the device, relates the device performance, and verifying the thermal expansion of all materials are compatible. Motorola performs extensive IOL testing as a continual process control monitor that test relates to the "device system**" as a whole. Motorola also performs extensive analysis and comparison of delta function temperatures. Motorola has determined that to effectively stress the device a delta T_J of 100°C is necessary which far exceeds many customers' application and determines the reliability modeling of the device.

Temperature Cycling (TC) is also an excellent stress test to determine the resistance of the device to high and low temperature excursions in an air medium. Where IOL electrically stresses the "device system" from internally, temperature cycle stresses the "device system" thermally from external environment conditions.

High Temperature Storage Life (HTSL), High Humidity Temperature Reverse Bias (H^3TRB), Thermal Shock (TC) and "Pressure Cooker" (Autoclave) are routinely tested, however it is felt by Motorola Reliability Engineering that HTRB, HTGB, IOL and TC are of primary importance. Motorola has been in the semiconductor industry for many years and will remain there as a leader with continued reliability, quality and customer relations.

RELIABILITY AUDIT PROGRAM

At Motorola reliability is assured through the rigid implementation of a reliability audit program. All IGBT products are grouped into generic families according to voltage ranges and package types. These families are sampled weekly from the raw stock at final test, then submitted for audit testing. The extreme stress testing, in real–time for each product run, may uncover process abnormalities that are detectable by the in–process controls. Typical reliability audit tests include high temperature reverse bias, high temperature gate bias, intermittent operating life, temperature cycling, and autoclave. To uncover any hidden failure modes, the reliability tests are designed to exceed the testing conditions of normal quality and reliability testing.

Audit failures which are detected are sent to the product analysis laboratory for real–time evaluations. This highly specialized area is equipped with a variety of analytical capabilities, including electrical characterizations, wet chemical and plasma techniques, metallurgical cross–sectioning, scanning electron microscope, dispersive x–ray, auger spectroscopy, and micro/macro photography. Together, these capabilities allow the prompt and accurate analysis of failure mechanisms — ensuring that the results of the evaluations can be translated into corrective actions and directed to the appropriate areas of responsibility.

The Motorola reliability audit program provides a powerful method for uncovering even the slightest hint of potential process anomalies in the IGBT product line. It is this stringent and continuing concern with the reliability audits that gives positive assurance that customer satisfaction will be achieved.

POWER FET
IGBT RELIABILITY AUDIT PROGRAM

Test	Conditions	S/S	Frequency
HTRB	V_{CE} = 100% Max Rating V_{GE} = 0 V T_J = 150°C Duration = 72 Hours (short), 1000 Hours (long)	50/Family	Weekly
HTGB	V_{GES} = ± 20 V V_{CE} = 0 V T_J = 150°C Duration = 72 Hours (short), 1000 Hours (long)	50/Family	Weekly
IOL	Δ T_J = 100°C $V_{CE} \geq$ 10 V Duration = 5000 Cycles (short), 15,000 cycles (long)	36/Family	Weekly
Solder Heat	1 Cycle @ 260°C for 10 seconds followed by:	25/Family	Weekly
Temperature Cycle	100 Cycles (short) 500 Cycles (long) –65 to +150°C Dwell Time ≥ 15 minutes Requires Faraday Cages	50/Family	Weekly
Pressure Cooker	P = 15 psi, T = 121°C Duration = 48 Hours (short), 96 Hours (long) (Plastic Package Only)	50/Family	Weekly

AVERAGE OUTGOING QUALITY (AOQ)

AOQ refers to the number of devices per million that do not fall within specification limits at the time of shipment. By implementing the philosophy of building in quality and reliability, Motorola has continually improved its outgoing quality. This pursuit of quality has led to a vendor certification program which guarantees a specific level of quality for the customer which has in many cases reduced or eliminated the need for incoming inspections.

$$\text{AOQ} = \text{Process Average x Probability of Acceptance x } 10^6 \text{ (PPM)}$$

- $\text{Process Average} = \dfrac{\text{Total Projected Reject Devices}}{\text{Total Number of Devices}}$
- $\text{Projected Reject Devices} = \dfrac{\text{Defects in Sample}}{\text{Sample Size}} \text{ x Lot Size}$
- Total Number of Devices = Sum of all the units in each submitted lot
- $\text{Probability of Acceptance} = 1 - \dfrac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$
- 10^6 = Conversion to Parts Per Million

Essentials of Reliability:

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble free service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. Reliability can be redefined as the probability of failure free performance, under a given manufacturer's specifications, for a given period of time. The failure rate of semiconductors in general, when plotted versus a long period of time, exhibit what has been called the "bath tub curve" (Figure 16–3).

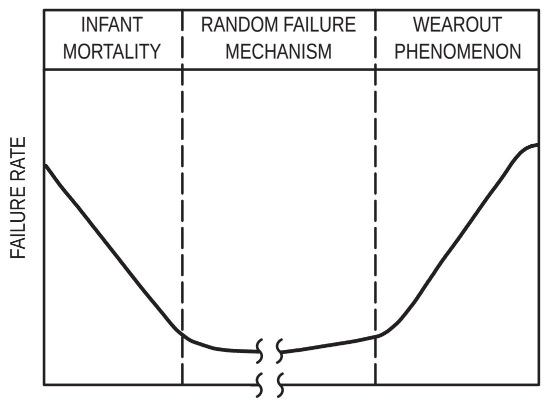


Figure 16–3. Failure Rate of Semiconductor

Reliability Mechanics

Since reliability evaluations usually involve only samples of an entire population of devices, the concept of the central limit theorem applies and a failure rate is calculated using the λ^2 distribution through the equation:

$$\lambda \leq \frac{\lambda^2\ (\alpha, 2r + 2)}{2\ nt}$$

λ^2 = chi squared distribution

where $\alpha = \dfrac{100 - cl}{100}$

λ = Failure rate

cl = Confidence limit in percent

r = Number of rejects

n = Number of devices

t = Duration of tests

The confidence limit is the degree of conservatism desired in the calculation. The central limit theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate, and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 16–4).

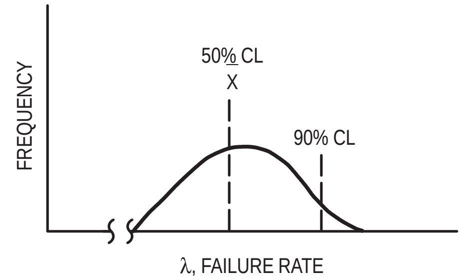


Figure 16–4. Confidence Limits and the Distribution of Sample Failure Rates

The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to λ^2 tables. The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the λ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_o(t)e^{-\emptyset/KT}$$

Where R(t) = reaction rate as a function of time and temperature

R_o = A constant

t = Time

T = Absolute temperature, °Kelvin (°C + 273°)

$\emptyset$ = Activation energy in electron volts (ev)

K = Boltzman's constant = 8.62×10^{-5} ev/°K

This equation can also be put in the form:

AF = Acceleration factor

T2 = User temperature

T1 = Actual test temperature

The Arrhenius equation states that reaction rate increases exponentially with the temperature. This produces a straight line when plotted on log–linear paper with a slope physically interpreted as the energy threshold of a particular reaction or failure mechanism.

Reliability Qualifications/Evaluations Outline:

Some of the functions of Motorola Reliability and Quality Assurance Engineering is to evaluate new products for introduction, process changes (whether minor or major), and product line updates to verify the integrity and reliability of conformance, thereby ensuring satisfactory performance in the field. The reliability evaluations may be subjected to a series of extensive reliability testing, such as those outlined in the "Tests Performed" section, or special tests, depending on the nature of the qualification requirement.

Section 17
Electrostatic Discharge and IGBT's

One of the major problems plaguing electronics components today is damage by electrostatic discharge (ESD). ESD can cause degradation or complete component failure. Shown in Table 1 are the susceptibility ranges of various technologies to ESD. As circuitry becomes more complex and dense, device geometries shrink, making ESD a major concern of the electronics industry.

GENERATION OF ESD

Electrostatic potential is a function of the relative position of non–conductors on the list of materials known as the Triboelectric Series, (see Table 2). Additional factors in charge generation are the intimacy of contact, rate of separation and humidity, which makes the material surfaces partially conductive. Whenever two non–conductive materials are flowing or moving with respect to each other, an electrostatic potential is generated.

Table 1. ESD Susceptibility of Various Technologies

Device Type	Range of ESD Susceptibility (Volts)
Power MOSFET	100–2,000
IGBT	4000–6000
Power Darlingtons	20,000–40,000
JFET	140–10,000
Zener Diodes	40,000
Schottky Diodes	300–2,500
Bipolar Transistors	380–7,000
CMOS	250–2,000
ECL (ICs)	500
TTL	300–2,500

Table 2. Triboelectric Series

Air Human Skin Glass Human Hair Wool Fur Paper Cotton	Increasingly Positive
Wood Hard Rubber Acetate Rayon Polyester Polyurethane PVC (Vinyl) Teflon	Increasingly Negative

A more complete table appears in DOD–HDBK–263

From Table 2, it can be seen that cotton is relatively neutral. The materials that tend to reject moisture are the most significant contributors to ESD. Table 3, also excerpted from DOD–HDBK–263, gives examples of the potentials that can be generated under various conditions.

Table 3. Typical Electrostatic Voltages

Means of Static Generation	Electrostatic Voltages	
	10 to 20 Percent Relative Humidity	65 to 90 Percent Relative Humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes per work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

From these three Tables, it is apparent that sensitive electronic components can be damaged or destroyed if precautions are not taken, and that the necessary voltages can be *easily* generated.

ESD and Power MOSFETs

Being MOS devices, insulated gate bipolar transistors can be damaged by ESD due to improper handling or installation. However, IGBT devices are not as susceptible as CMOS. Due to their large input capacitances, they are able to absorb more energy before being charged to the gate–breakdown voltage. Nevertheless, once breakdown begins, there is enough energy stored in the gate–source capacitance to cause complete perforation of the gate oxide. With a gate–to–emitter rating of $V_{GE} = \pm\ 20$ V maximum and electrostatic voltages typically being 100–25,000 volts, it becomes very clear that these devices require special handling procedures. Figure 17–1 shows curve tracer drawings of a good device, and the same device degraded by ESD.

Static Protection

The basic method for protecting electronic components combines the prevention of static build up with the removal of existing charges. The mechanism of charge removal from charged objects differs between insulators and conductors. Since charge cannot flow through an insulator, it cannot be removed by contact with a conductor. If the item to be discharged is an insulator (plastic box, person's clothing, etc.), ionized air is required. If the object to be discharged is a conductor (metal tray, conductive bag, person's body, etc.), complete discharge can be accomplished by grounding it.

A complete static–safe work station should include a grounded conductive table top, floor mats, grounded operators (wrist straps), conductive containers, and an ionized air blower to remove static from non–conductors. All soldering irons should be grounded. All non–conductive items such as styrofoam coffee cups, cellophane wrappers, paper, plastic handbags, etc. should be removed from the work area. A periodic survey of the work area with a static meter is good practice and any problems detected should be corrected

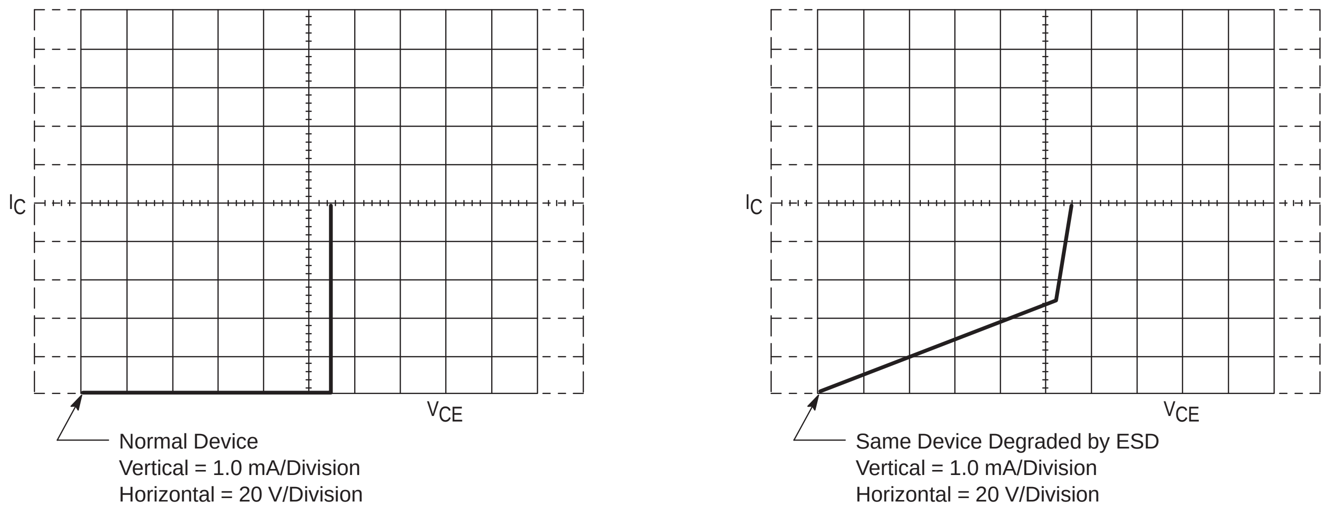


Figure 17–1. Curve Tracer Drawings of V_{CE} versus I_C of a Good Device (Left), and a Device in which the Gate was Damaged with ESD (Right). The Gate in this Device is Likely a Resistive Short.

immediately. Above all, education of all personnel in the proper handling of static–sensitive devices is key to preventing ESD failures.

By following the above procedures, and using the proper equipment, ESD sensitive devices can be handled without being damaged. The key items to remember are:

1 – Handle all static sensitive components at a static safeguarded work area.

2 – Transport all static sensitive components in static shielding containers or packages.

3 – Education of all personnel in proper handling of static sensitive components.

Test Method:

Military specifications MIL–STD–883B Method 3015.1, MIL–STD–750C, Method 1020, DOD–HDBK263, and DOD–STD–1686 classify the sensitivity of semiconductor devices to electrostatic discharge as a function of exposure to the output of a charged network (Table 4). Through measurements and general agreement, the “human–body model” (HBM) was specified as a network that closely approximated the charge storage capability (100 pF) and the series resistance (1.5 k) of a typical individual (Figure 17–2). Discharge of this network directly into a device indicates that the model assumes a “hard” ground is in contact with the part. Although all pin combinations should be evaluated in both polarities (a total of six combinations for IGBT’s), preliminary tests usually show that gate–oxide breakdown is most likely, and that reverse–biased junctions are about an order of magnitude more sensitive than forward–biased ones. The amount of testing, and components required can therefore be reduced to sensible levels, yet still yield statistically sound data. The damage mechanism, which can be identified through failure analysis of shorted or degraded samples, is usually oxide puncture or junction meltthrough.

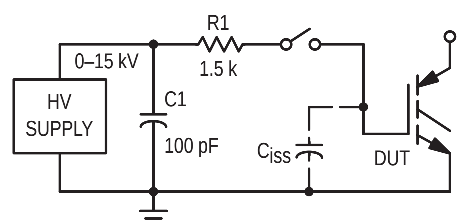


Figure 17–2. The Human–Body Equivalent Network with C_{iss} Parasitic Element in Dashed Lines

Significance of Sensitivity Data

Assuming that corrective measures cannot be immediately applied in a manufacturing area, or that produces manufactured using MOS gated components are likely to be exposed to ESD events in the field, the sensitivity of the device can be used as a general indicator of the likelihood of failure. Additionally, the extent and cost of protective measures increases as device susceptibility increases.

Table 4. Sensitivity of Semiconductors to ESD from a Charged Network (HBM)

Device Sensitivity (C_1 Peak Voltage)	MIL–STD–883 Class	DOD–HDBK–263 Class	Typical Preventive Measures(2)
0–1000	A (Sensitive)	Class 1	Careful Case, Keyboard Design, Wrist Straps, Ionized Air, Conductive Flooring, Conductive Clothing, etc. Field–Strength Alarm.
1000–2000	A	Class 2	
2000–4000	B (Nonsensitive)	Class 3	Antistatic Carpet Spray, Wrist Straps, Conductive Packaging Materials.
4000–15,000(1)	B	Class 3	Humidity Adjustment

NOTES: 1. Data collected in many applications have shown that under special conditions voltages considerably in excess of 15 kV can be generated with certain materials in the Triboelectric Series. (Table 3)

2. These examples are intended only as very general guidelines. The actual accuracy of a given method is highly variable, as a large number of interdependent factors influence electrostatic field generation. Operator awareness, complemented with a high quality hand–held electrostatic field–strength meter *referenced to ground,* can be very effective in controlling losses due to ESD.

MEASURING DEVICE SENSITIVITY

A Simple ESD Pulser

As shown in the circuit diagram, Figure 17–3, the tester consists of a high voltage supply utilizing a Darlington transistor oscillator driving a television flyback transformer. The high voltage is rectified by a commercially–available color television semiconductor tripler module. A single low–voltage power supply of about 20 volts is used for the entire tester. The high voltage power supply is adjusted by means of a ten–turn potentiometer and an I.C. series regulator. Use of a Bourns Knobpot®, having a clock–type turns–counting dial, gives coarse adjustment indication.

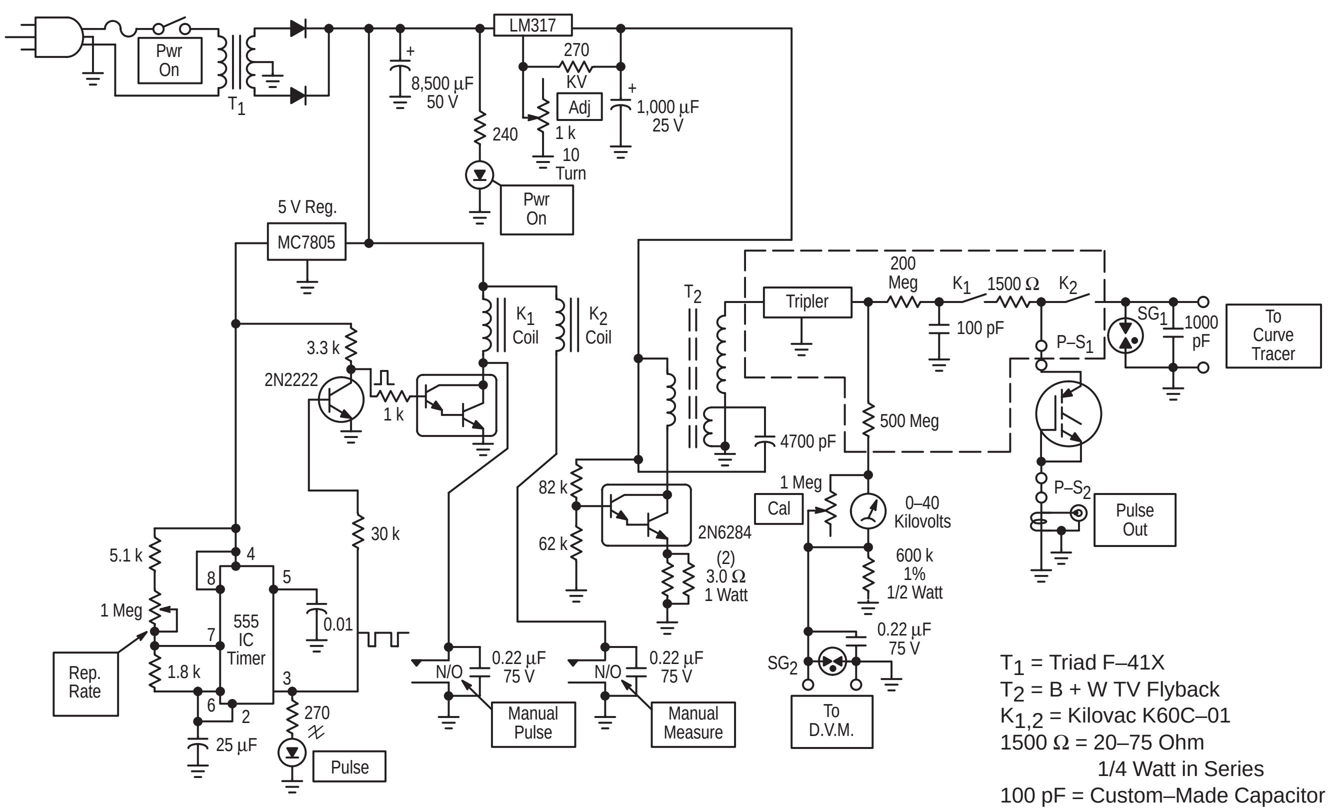


Figure 17–3. ESD (Electrostatic Discharge) Tester with 40 Kilovolt Capability

A small manually–operated ESD pulser is relatively easy to construct. Although this tester is capable of testing over the entire voltage range of DOD–HDBK–263 and is capable of much higher voltages than would be used for characterizing TMOS devices, its design is typical.

The high voltage is monitored by means of components removed from a color television hand–held high voltage probe. The probe is disassembled, and the meter, accurate to about 5%, was mounted on the front panel. An additional resistor is placed in series with the divider string, and front panel jacks are provided to connect it to an external digital voltmeter (DVM). A calibration potentiometer is provided, so that the instrument can be placed on a regular schedule of periodic calibration and maintenance. Bipolar transistors are used as drivers for the relays in the DUT circuit. Most ESD measurements were made by hand, alternately pushing the pulse button, then, after a safe delay, or “cooling period,” the measurement button.

High–Voltage Components

The high–voltage circuit has been stippled for clarity. High–voltage vacuum reed relays are not used because they are limited in working voltage by the physical separation between the coil windings and the end of the glass envelope. Kilovac, of Santa Barbara, California, manufactures miniaturized vacuum relays to 100 kV. One type, the K–60–C, is ceramic–cased, and of small size suitable for the tester. The terminal spacing limits it to 15 kV operation, so the relay is purchased without the normal silicone rubber encapsulation and the tester high–voltage compartment is immersed in ordinary colorless mineral oil. The manufacturer further increases the voltage rating by filling the relay with sulfur hexafluoride gas (SF6) under pressure, which eliminates contact arcing.

High–voltage capacitors of reasonable size are obtained from the Maida Capacitor Company. The dielectric is carefully chosen to have a low voltage coefficient. Many ceramic dielectrics have a voltage coefficient as large as 40%, and the capacitance would not meet the +10% capacitance tolerance requirement in MIL–STDs 750 and 883A at extended voltages.

The 1.5 kOhm series resistor must be specially designed to be ESD–resistant. It is constructed by the series connection of 20–75 ohm, 1/4 watt carbon composition resistors. This is necessary because the breakdown of the resistors during pulsing would cause the test circuit to become the zero–ohm model, and improper ESD sensitivity values would be obtained.

The High–Voltage Compartment

The high–voltage section of the tester was built in a dielectric filled compartment. Mineral oil, castor oil, parafin oil, silicone oil, and transformer oil, all will work equally well. Beware that these liquids are flammable. Use of polychlorinated biphenyl (PCB), a fireproof dielectric liquid, should be avoided, as it is toxic. The inclusion of the 600 megohm divider resistor and the small custom–made high voltage ceramic capacitor in the oil–filled compartment eliminated the need for corona shields, large physical spacings, and silicone rubber terminal coverings. Operation to 43 kV is very reliable.

The design of flyback transformers has been perfected over the years for continuous operation in air, and it is not placed in the oil–filled compartment.

Test Method

The threshold, or step–stress, method is used to classify device sensitivity, as discussed in DOD–HDBK–263 in paragraph 6.6.2. This method is a time–saver compared to the categorization method, and is very useful with discrete devices. Additionally, the ESD sensitivity of a device can be determined exactly. The waveform is monitored with the use of a Tektronix 2467, 350 MHz real–time oscilloscope with a CT–1 current transformer and P6040 probe. The transformer was placed on the ground side of the device under test.

FAILURE CRITERIA

The tester is deliberately kept simple in design, so the relays are operated manually with pushbuttons. The voltage is manually adjusted in increasing increments until any change in the characteristics of the device under test is indicated on the curve tracer. No coincidence lockout circuit is provided. Simultaneous closure of K1 and K2 would shunt the DUT with the curve–tracer input capacitance. In some cases, the curve tracer could be damaged. Technically–oriented operators should be used.

It is easily understood that the resolution of the tester in this manual configuration is limited by the size of the voltage steps between relay closures. Automating this operation could be quite complex, depending on the test strategy and data reduction methods. Certainly, this tester lends itself to microprocessor or computer control, and interface circuits to accomplish this are already on the market. The voltage increment can then be set very small for good accuracy, and the system can be left unattended to find the threshold, stop testing, print out the data, and continue with the next part. Such testers, intended primarily for I.C.s., are commercially available.

Warning:

Caution is advised in the construction and operation of this circuit, as the potentials and stored energies in this circuit may be ***lethal.*** Every effort should be made to shield operators from the possibility of contact. Motorola cannot be responsible for claims resulting from the use, or misuse, of this circuit.

TEST RESULTS

Measurement of ESD sensitivity thresholds using the 100 pF–1.5 k circuit has produced the results shown below. An important conclusion from this data is that the ESD sensitivity decreases as the die size (and power–handling capability) increase. Part of the explanation for this phenomenon is that C_{ISS} increases as die size increases. Referring to Figure 17–2, we are discharging the HBM network into a larger and larger capacitive load. Also, these devices fall at or below the 2,000 volt limit, defined by Mil–Std–750C as that which classifies a device as static–sensitive. IGBT’s, then, should be handled with proper precautions.

Chapter Four

Data Sheets

Table of Contents

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

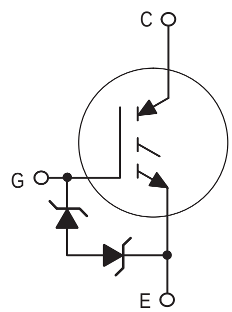
Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N–Channel Enhancement–Mode Silicon Gate

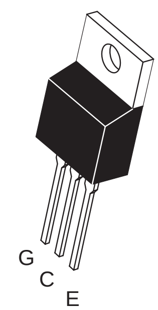
MGP4N60E

IGBT IN TO–220
4.0 A @ 90°C
6.0 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 60 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 3.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	6.0 4.0 8.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	62.5 0.51	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.0 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 1.5 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 1.5 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 3.0 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 3.0 Adc)		g_{fe}	—	1.8	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	342	—	pF
Output Capacitance		C_{oes}	—	40	—	
Transfer Capacitance		C_{res}	—	3.0	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 3.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	34	—	ns
Rise Time		t_r	—	30	—	
Turn–Off Delay Time		$t_{d(off)}$	—	36	—	
Fall Time		t_f	—	216	—	
Turn–Off Switching Loss		E_{off}	—	0.10	0.15	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 3.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	33	—	ns
Rise Time		t_r	—	32	—	
Turn–Off Delay Time		$t_{d(off)}$	—	56	—	
Fall Time		t_f	—	340	—	
Turn–Off Switching Loss		E_{off}	—	0.165	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 3.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	18.1	—	nC
		Q_1	—	3.8	—	
		Q_2	—	7.8	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

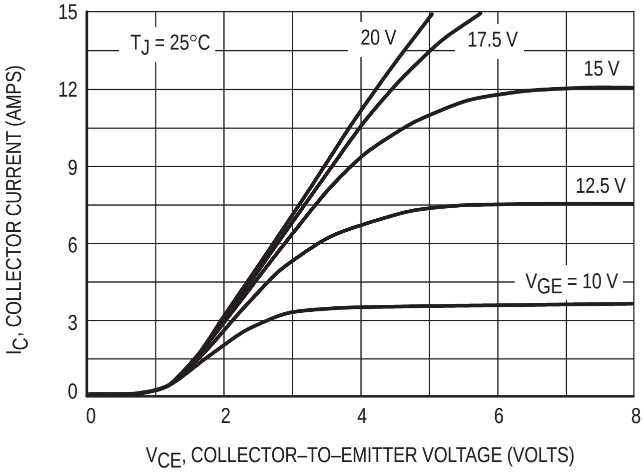


Figure 1. Output Characteristics

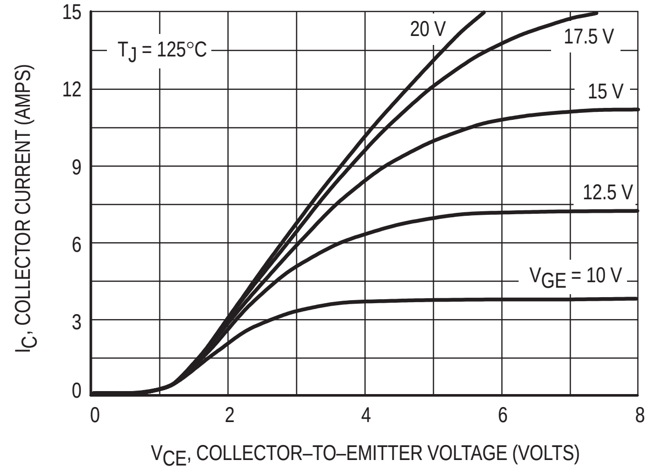


Figure 2. Output Characteristics

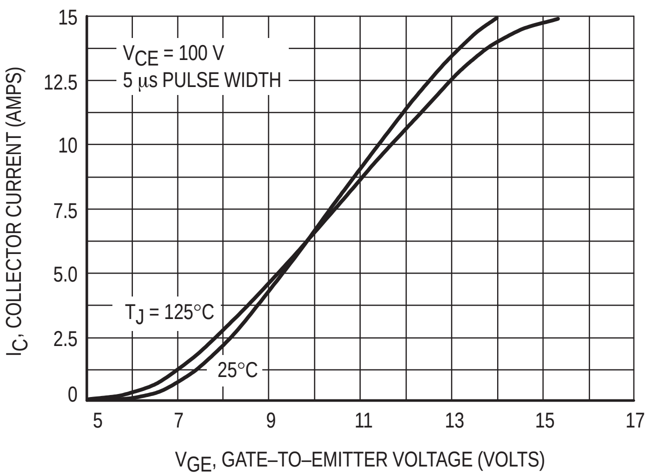


Figure 3. Transfer Characteristics

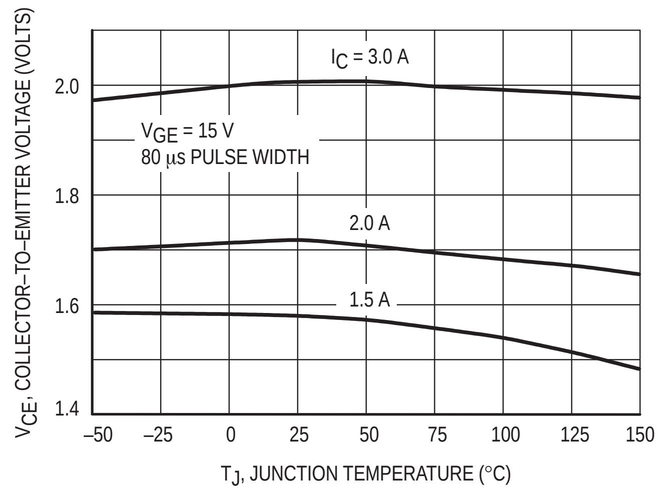


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

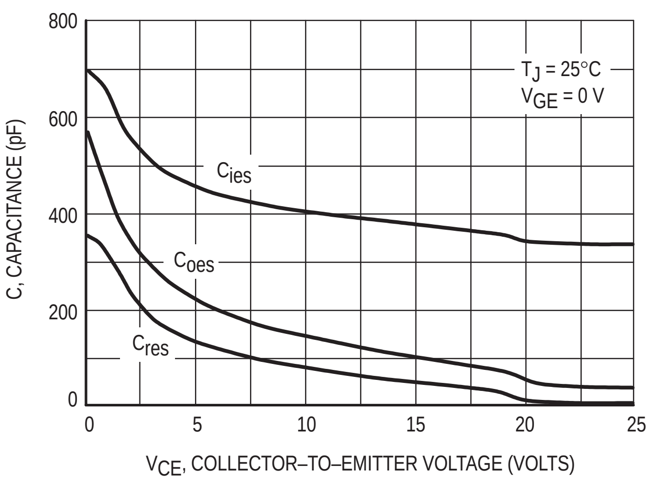


Figure 5. Capacitance Variation

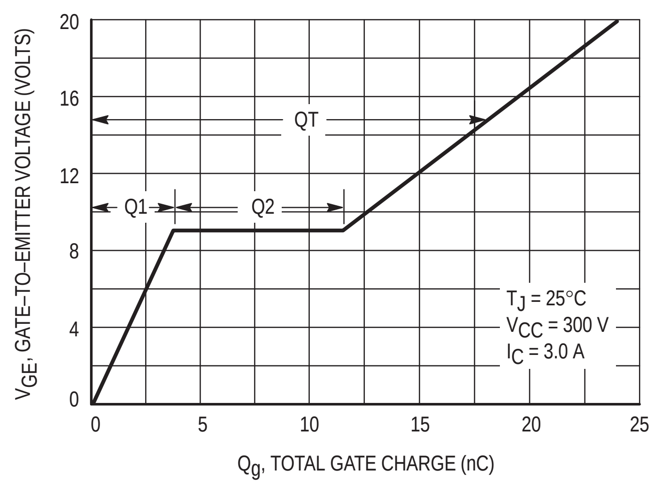


Figure 6. Gate–To–Emitter Voltage versus Total Charge

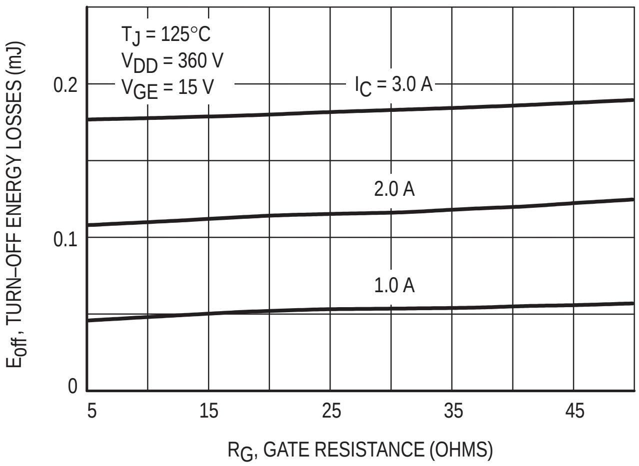


Figure 7. Turn–Off Losses versus Gate Resistance

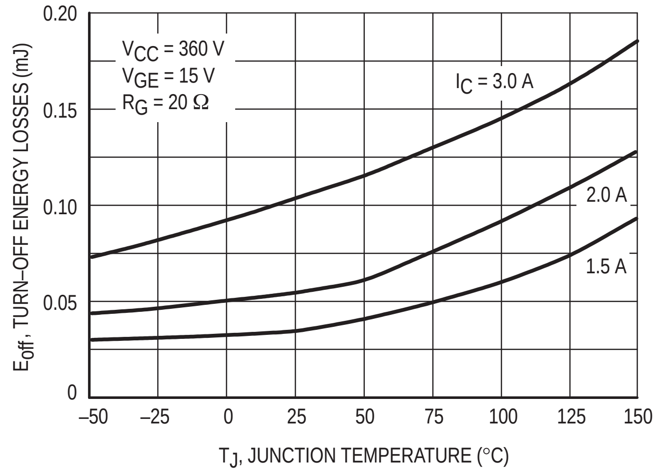


Figure 8. Turn–Off Losses versus Junction Temperature

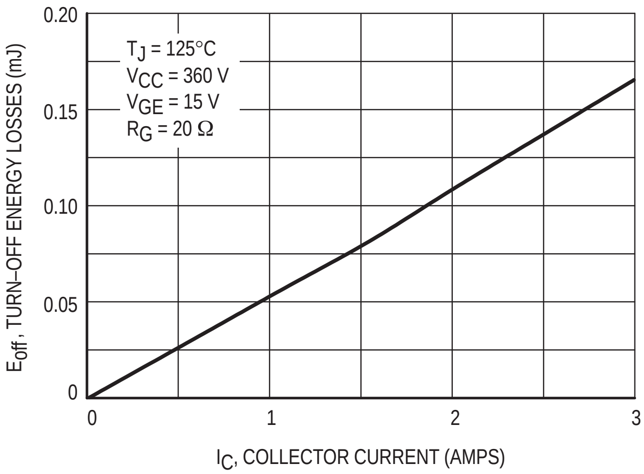


Figure 9. Turn–Off Losses versus Collector Current

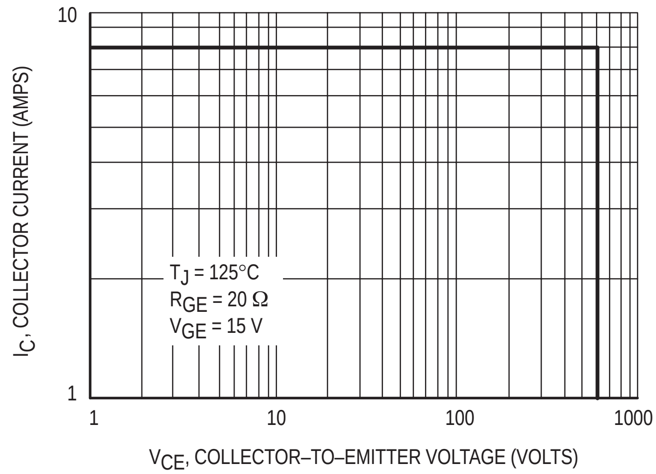


Figure 10. Reverse Biased Safe Operating Area

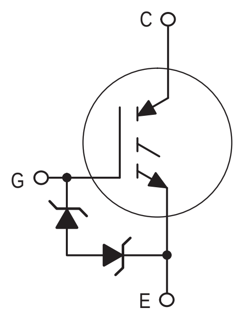
Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N–Channel Enhancement–Mode Silicon Gate

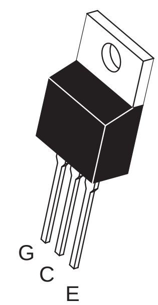
MGP7N60E

IGBT IN TO–220
7.0 A @ 90°C
10 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 70 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 5.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	10 7.0 14	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	81 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.5 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 2.5 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 2.5 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 5.0 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 5.0 Adc)		g_{fe}	—	2.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	610	—	pF
Output Capacitance		C_{oes}	—	60	—	
Transfer Capacitance		C_{res}	—	10	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 5.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	22	—	ns
Rise Time		t_r	—	24	—	
Turn–Off Delay Time		$t_{d(off)}$	—	64	—	
Fall Time		t_f	—	196	—	
Turn–Off Switching Loss		E_{off}	—	0.20	0.34	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 5.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	31	—	ns
Rise Time		t_r	—	24	—	
Turn–Off Delay Time		$t_{d(off)}$	—	195	—	
Fall Time		t_f	—	220	—	
Turn–Off Switching Loss		E_{off}	—	0.35	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 5.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	27.2	—	nC
		Q_1	—	7.0	—	
		Q_2	—	13.7	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

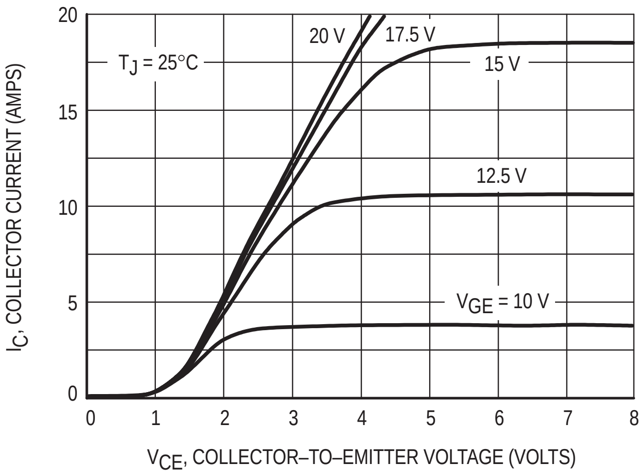


Figure 1. Output Characteristics

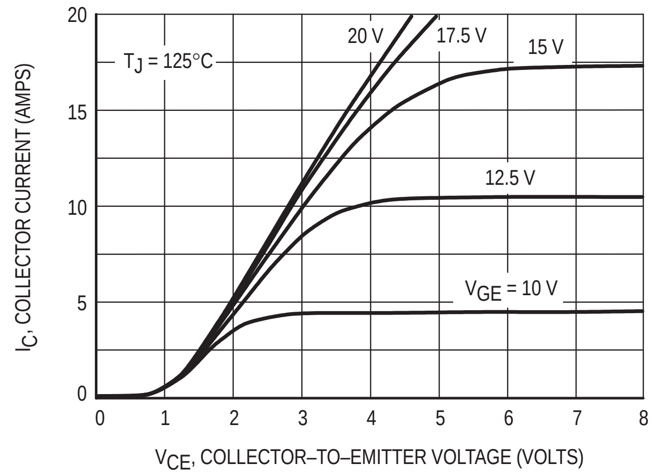


Figure 2. Output Characteristics

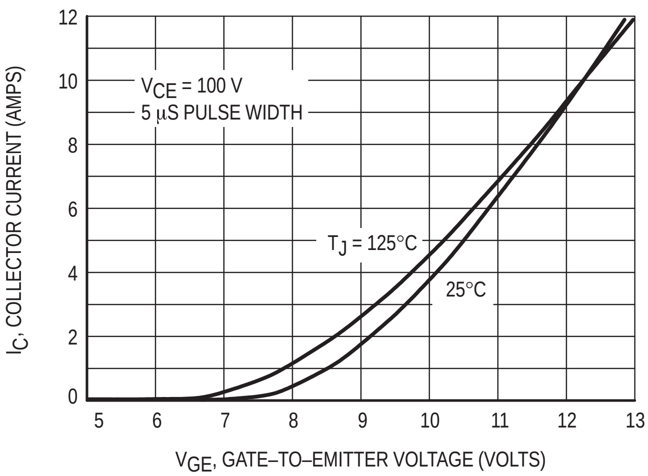


Figure 3. Transfer Characteristics

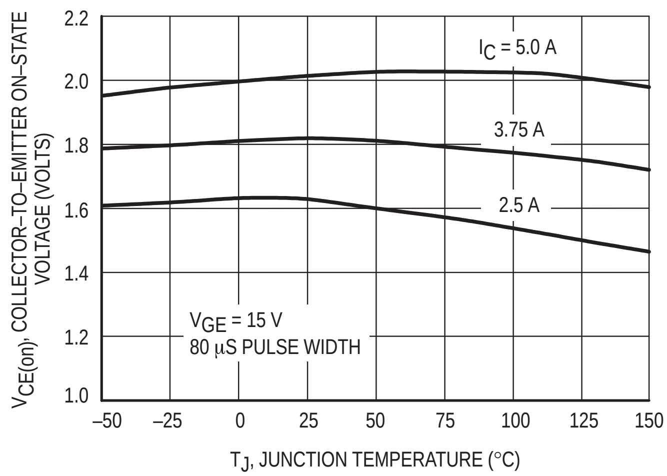


Figure 4. V_{CE} versus Junction Temperature

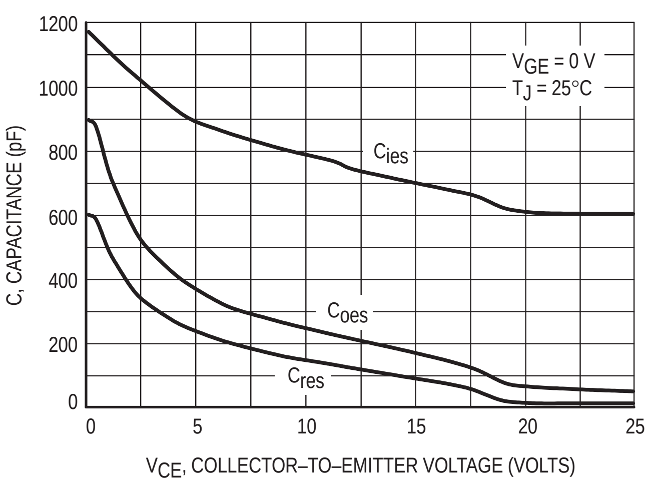


Figure 5. Capacitance Variation

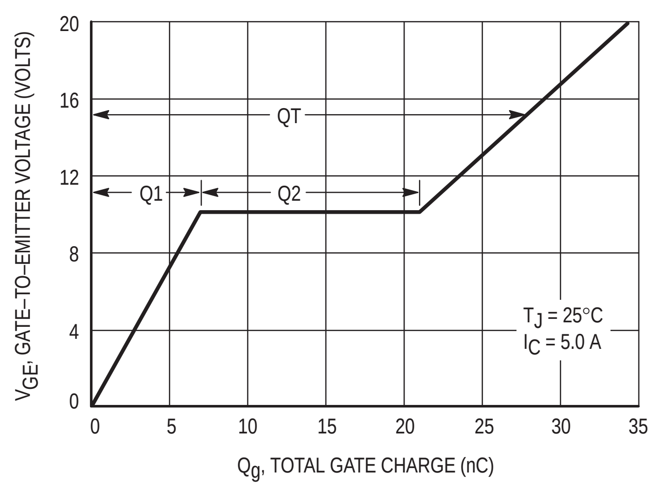


Figure 6. V_{GE} versus Total Charge

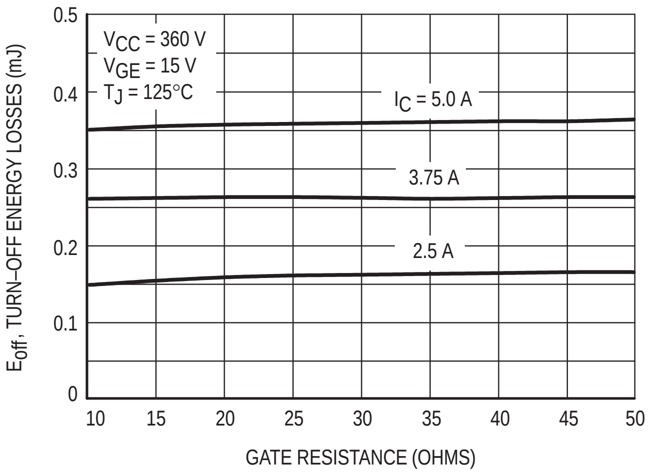


Figure 7. Turn–Off Losses versus Gate Resistance

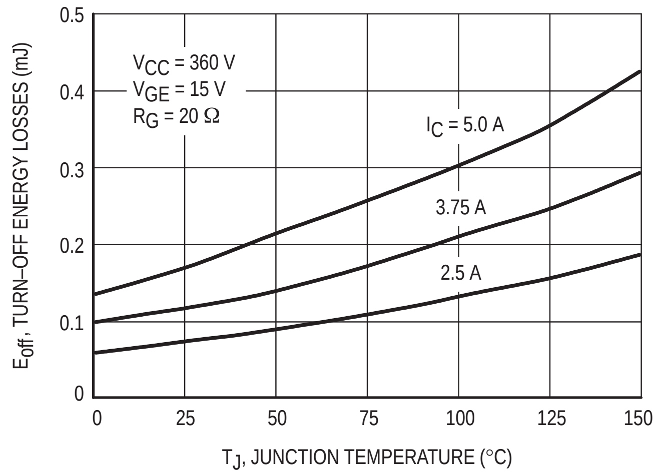


Figure 8. Turn–Off Losses versus Junction Temperature

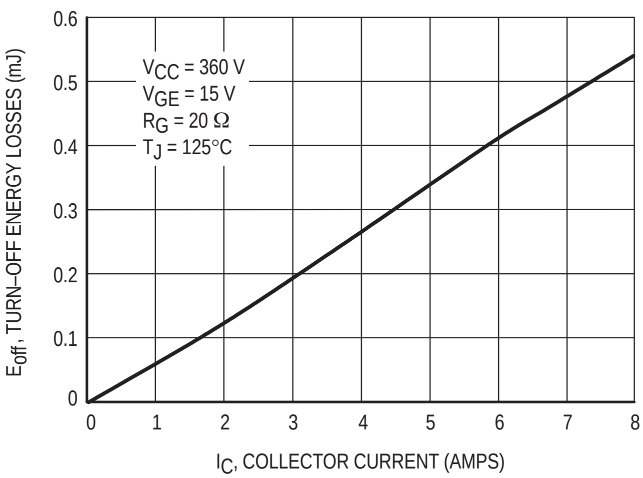


Figure 9. Turn–Off Energy Losses versus Collector Current

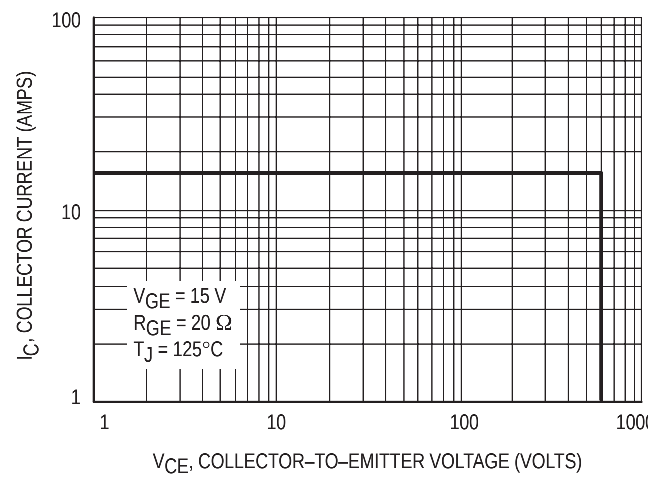


Figure 10. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

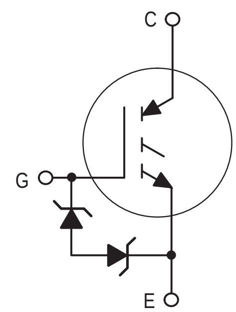
N–Channel Enhancement–Mode Silicon Gate

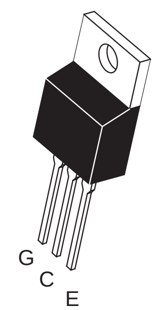
MGP11N60E

IGBT IN TO–220
11 A @ 90°C
15 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 60 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 8.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	15 11 22	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 4.0 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 4.0 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 8.0 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 8.0 Adc)		g_{fe}	—	3.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	779	—	pF
Output Capacitance		C_{oes}	—	81	—	
Transfer Capacitance		C_{res}	—	13	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	46	—	ns
Rise Time		t_r	—	34	—	
Turn–Off Delay Time		$t_{d(off)}$	—	102	—	
Fall Time		t_f	—	226	—	
Turn–Off Switching Loss		E_{off}	—	0.32	0.40	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	42	—	ns
Rise Time		t_r	—	26	—	
Turn–Off Delay Time		$t_{d(off)}$	—	214	—	
Fall Time		t_f	—	228	—	
Turn–Off Switching Loss		E_{off}	—	0.48	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	39.2	—	nC
		Q_1	—	8.7	—	
		Q_2	—	17.4	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

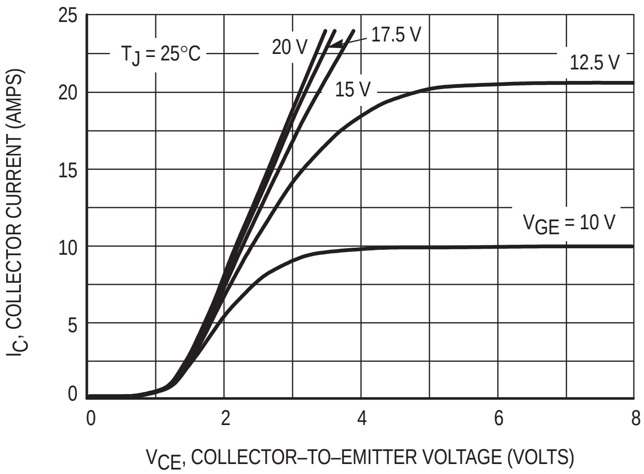


Figure 1. Output Characteristics

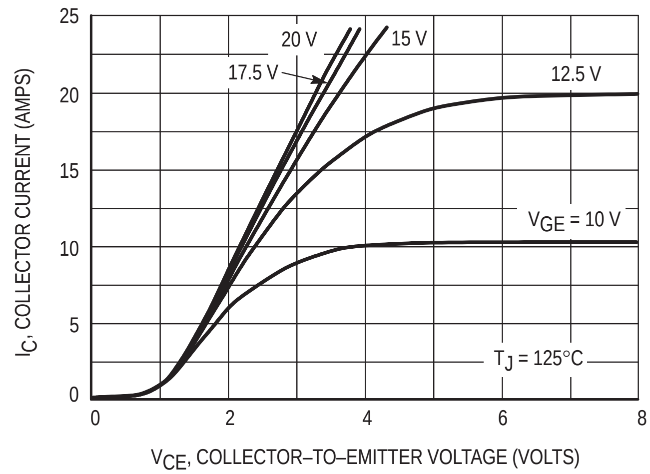


Figure 2. Output Characteristics

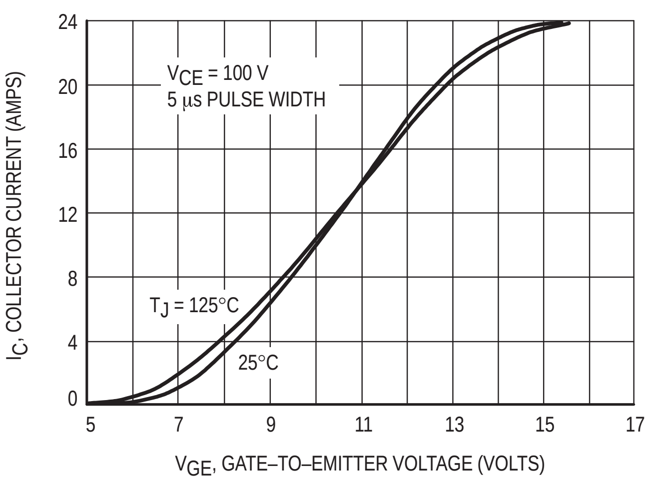


Figure 3. Transfer Characteristics

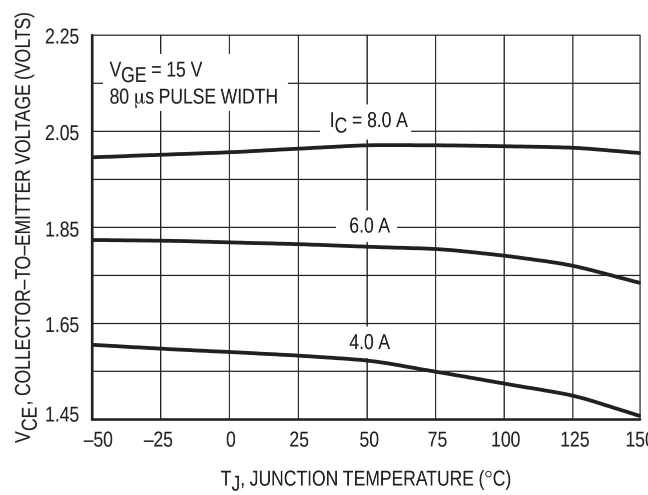


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

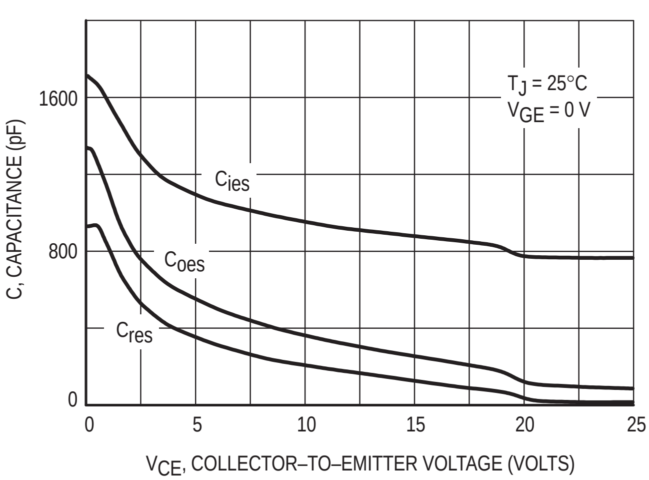


Figure 5. Capacitance Variation

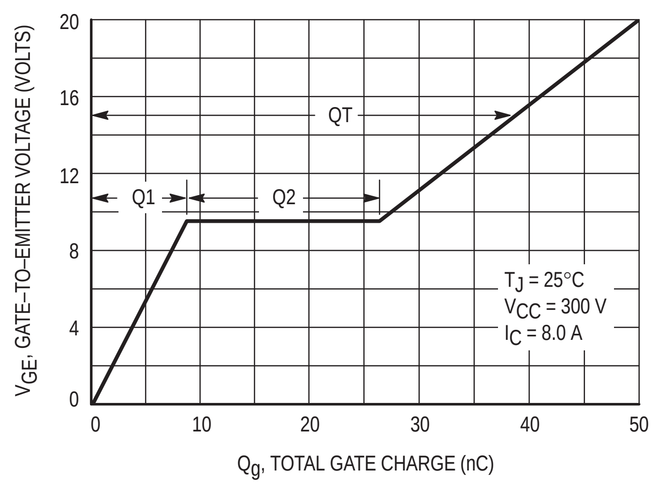


Figure 6. Gate–To–Emitter Voltage versus Total Charge

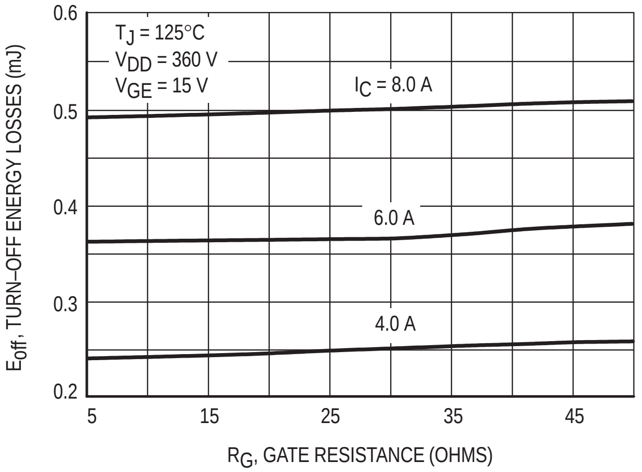


Figure 7. Turn–Off Losses versus Gate Resistance

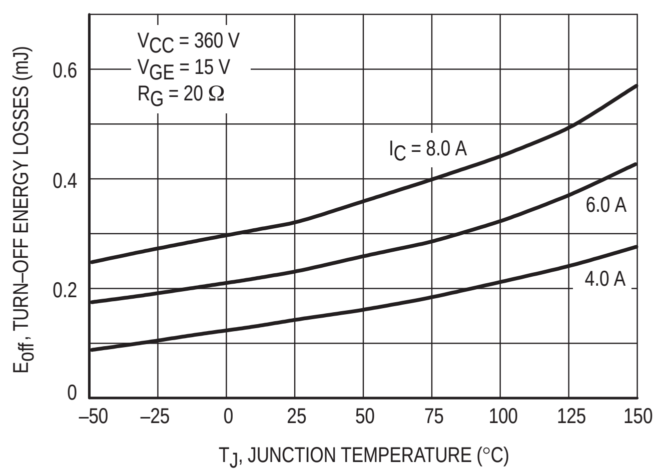


Figure 8. Turn–Off Losses versus Junction Temperature

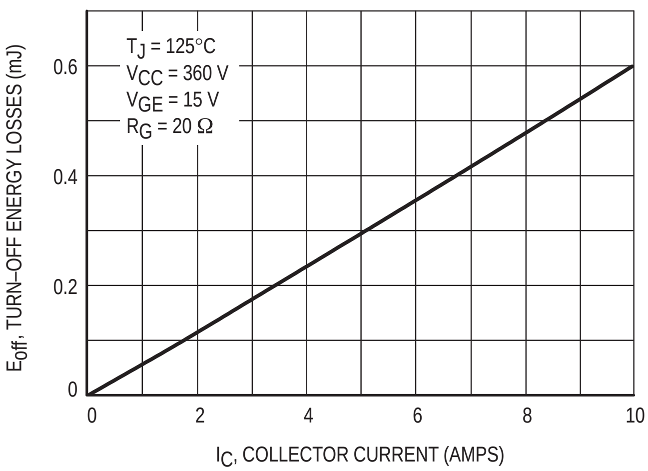


Figure 9. Turn–Off Losses versus Collector Current

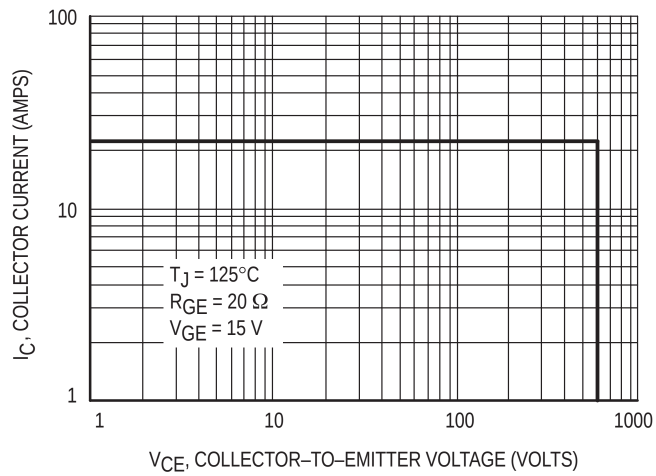


Figure 10. Reverse Biased Safe Operating Area

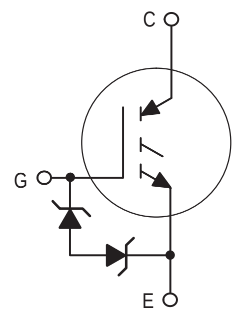
Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N–Channel Enhancement–Mode Silicon Gate

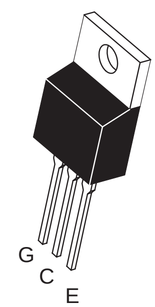
MGP14N60E

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 63 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 10 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes

IGBT IN TO–220
14 A @ 90°C
18 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	18 14 28	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	112 0.89	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.1 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)CES}$	 600 —	 — 870	 — —	Vdc mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		I_{CES}	 — —	 — —	 10 200	μAdc
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc) (V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 10 Adc)		$V_{CE(on)}$	 — — —	 1.6 1.5 2.0	 1.9 — 2.4	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	 4.0 —	 6.0 10	 8.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)		g_{fe}	—	5.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1020	—	pF
Output Capacitance		C_{oes}	—	104	—	
Transfer Capacitance		C_{res}	—	17	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	38	—	ns
Rise Time		t_r	—	40	—	
Turn–Off Delay Time		$t_{d(off)}$	—	120	—	
Fall Time		t_f	—	204	—	
Turn–Off Switching Loss		E_{off}	—	0.35	0.45	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	32	—	ns
Rise Time		t_r	—	30	—	
Turn–Off Delay Time		$t_{d(off)}$	—	208	—	
Fall Time		t_f	—	212	—	
Turn–Off Switching Loss		E_{off}	—	0.63	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	57	—	nC
		Q_1	—	12	—	
		Q_2	—	25	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	 —	 7.5	 —	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

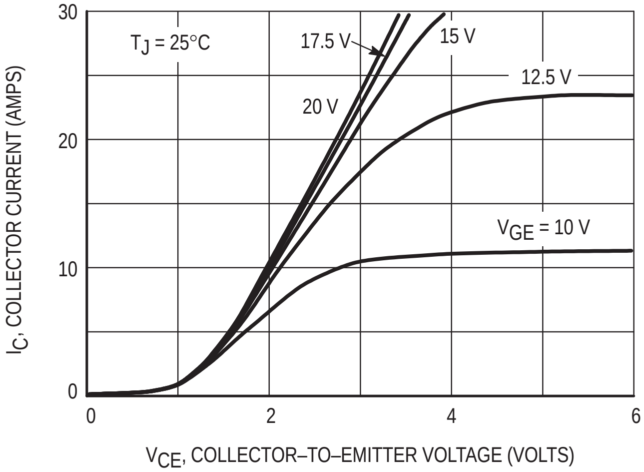


Figure 1. Output Characteristics

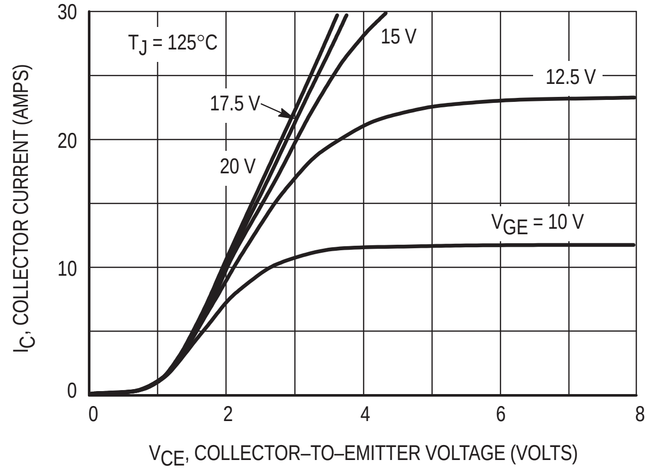


Figure 2. Output Characteristics

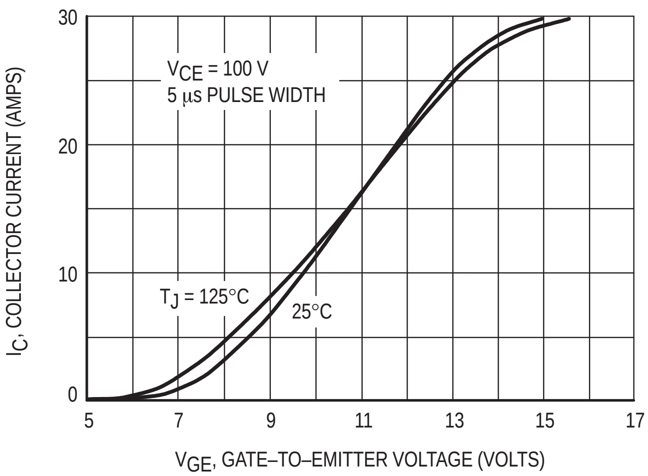


Figure 3. Transfer Characteristics

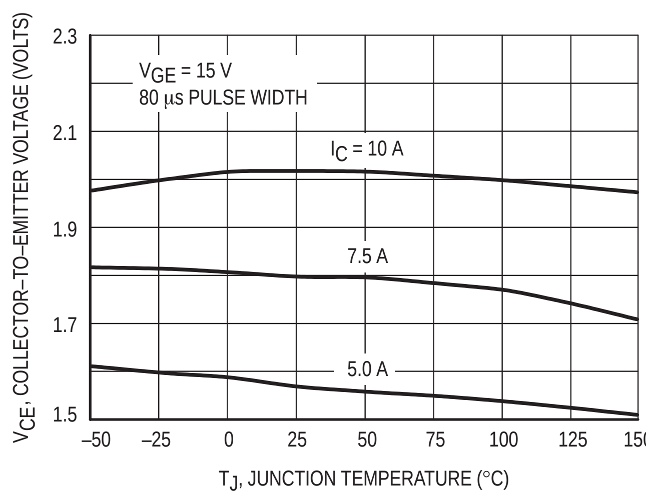


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

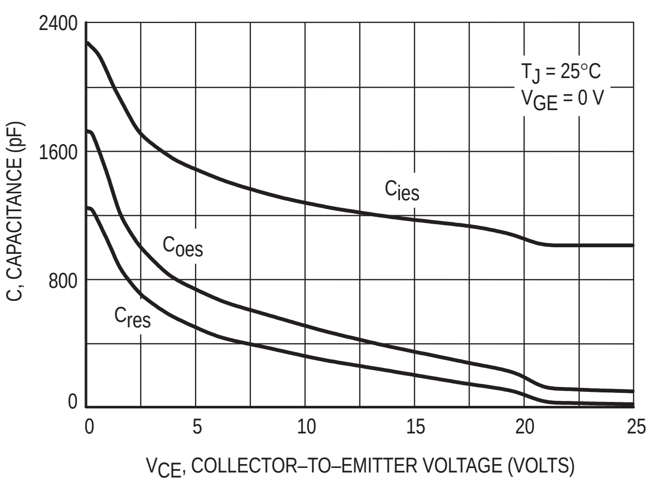


Figure 5. Capacitance Variation

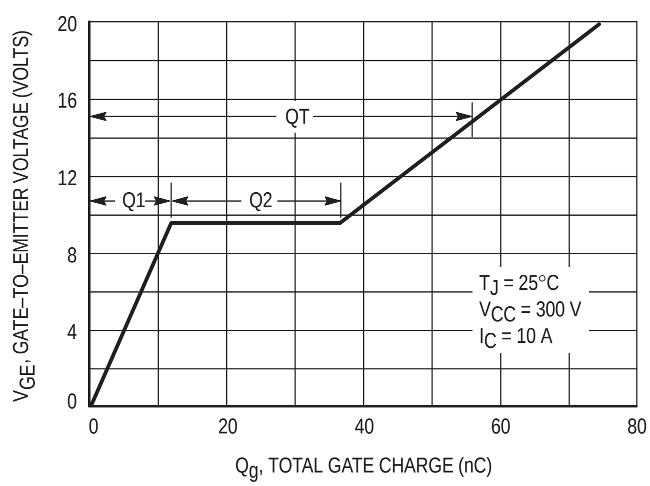


Figure 6. Gate–To–Emitter Voltage versus Total Charge

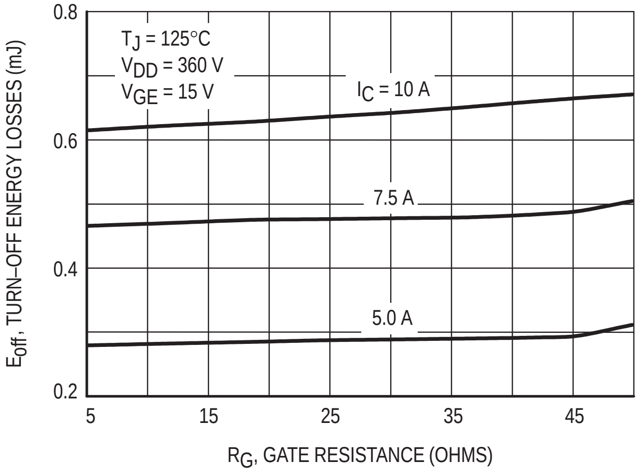


Figure 7. Turn–Off Losses versus Gate Resistance

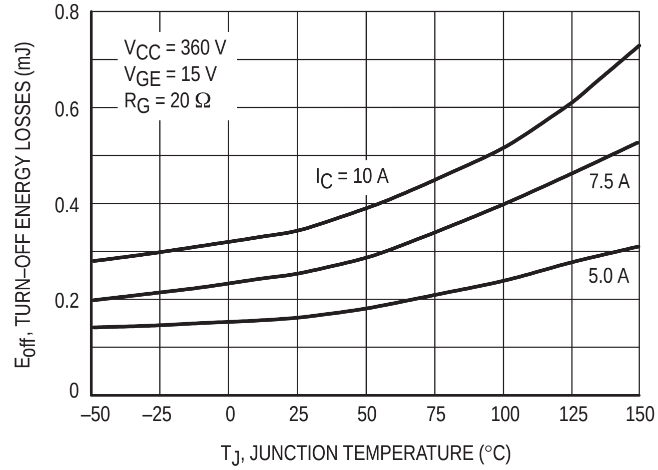


Figure 8. Turn–Off Losses versus Junction Temperature

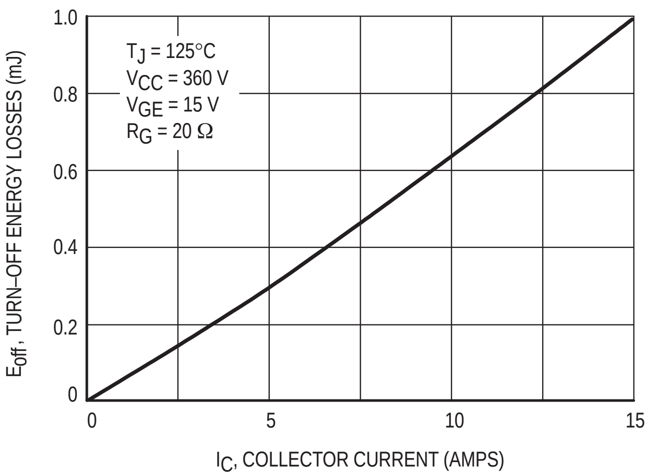


Figure 9. Turn–Off Losses versus Collector Current

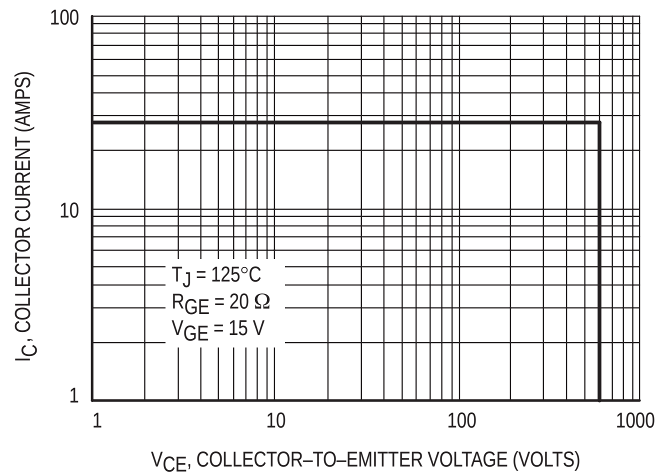


Figure 10. Reverse Biased Safe Operating Area

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

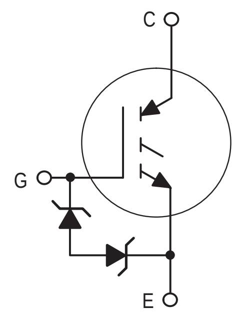
MGP21N60E

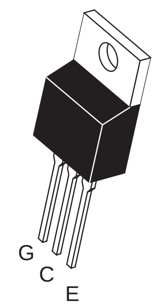
Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N–Channel Enhancement–Mode Silicon Gate

IGBT IN TO–220
21 A @ 90°C
31 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 65 µJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 µs minimum at 125°C, 400 V
- Low On–Voltage 2.1 V typical at 20 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	31 21 42	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	142 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	µs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.9 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc) Temperature Coefficient (Positive)		$V_{(BR)CES}$	600 —	— 870	— —	Vdc mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		I_{CES}	— —	— —	10 200	μAdc
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 10 Adc) (V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 20 Adc)		$V_{CE(on)}$	— — —	1.7 1.5 2.2	2.1 — 2.5	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	8.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1605	—	pF
Output Capacitance		C_{oes}	—	146	—	
Transfer Capacitance		C_{res}	—	23	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	29	—	ns
Rise Time		t_r	—	60	—	
Turn–Off Delay Time		$t_{d(off)}$	—	238	—	
Fall Time		t_f	—	140	—	
Turn–Off Switching Loss		E_{off}	—	0.80	1.15	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	28	—	ns
Rise Time		t_r	—	62	—	
Turn–Off Delay Time		$t_{d(off)}$	—	338	—	
Fall Time		t_f	—	220	—	
Turn–Off Switching Loss		E_{off}	—	1.3	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	86	—	nC
		Q_1	—	18	—	
		Q_2	—	39	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

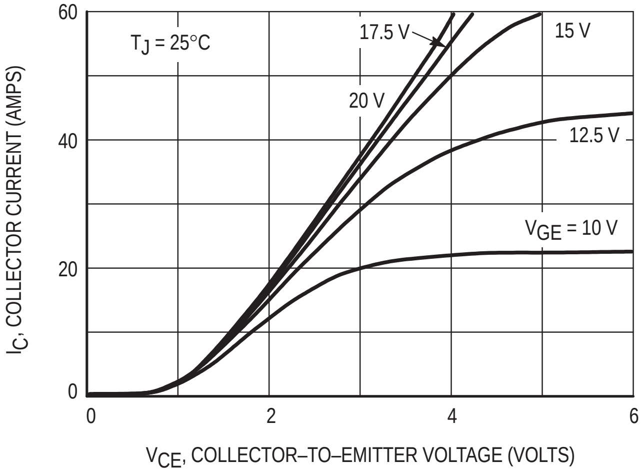


Figure 1. Output Characteristics

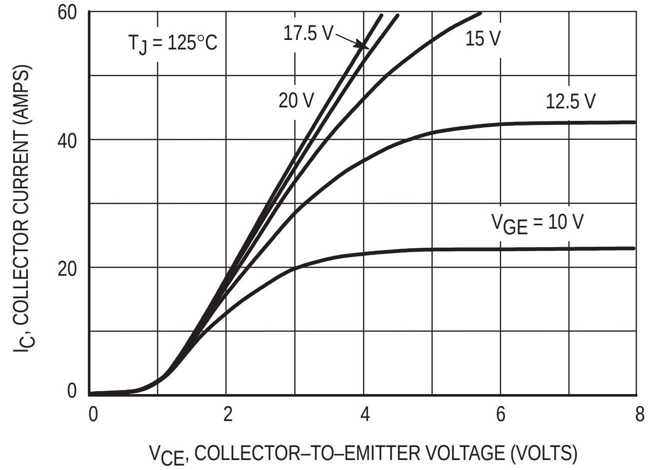


Figure 2. Output Characteristics

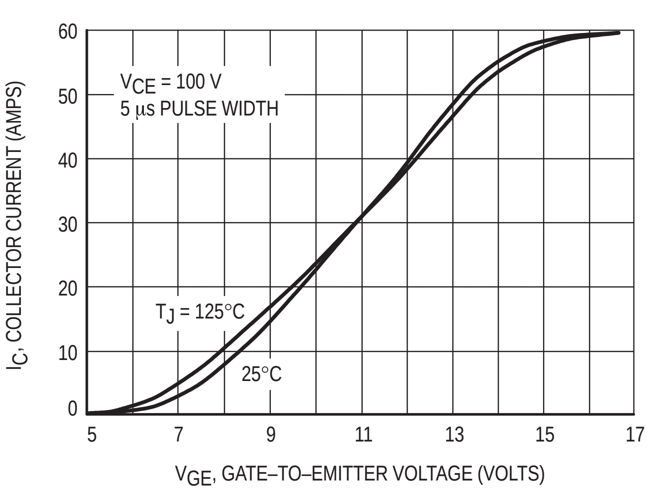


Figure 3. Transfer Characteristics

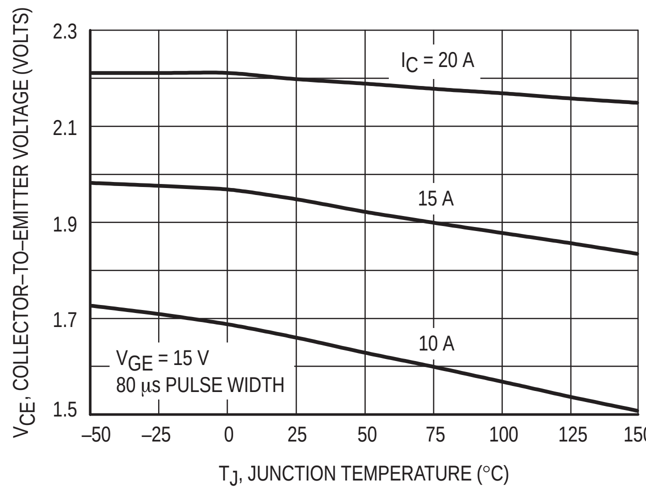


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

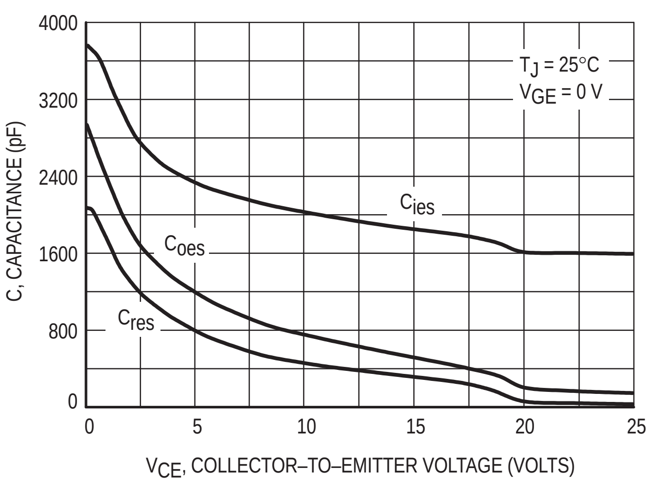


Figure 5. Capacitance Variation

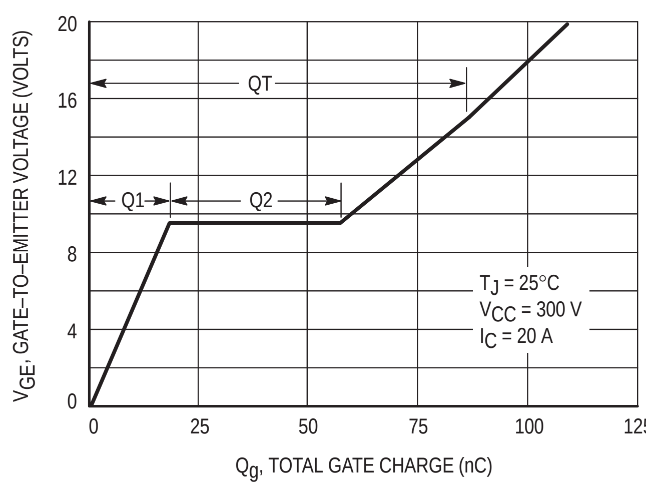


Figure 6. Gate–To–Emitter Voltage versus Total Charge

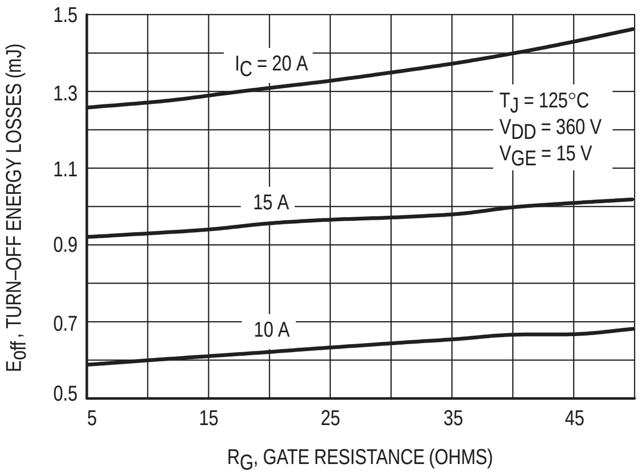


Figure 7. Turn–Off Losses versus Gate Resistance

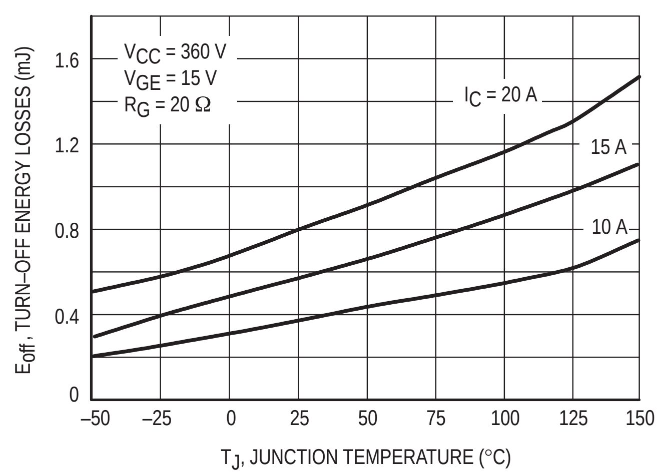


Figure 8. Turn–Off Losses versus Junction Temperature

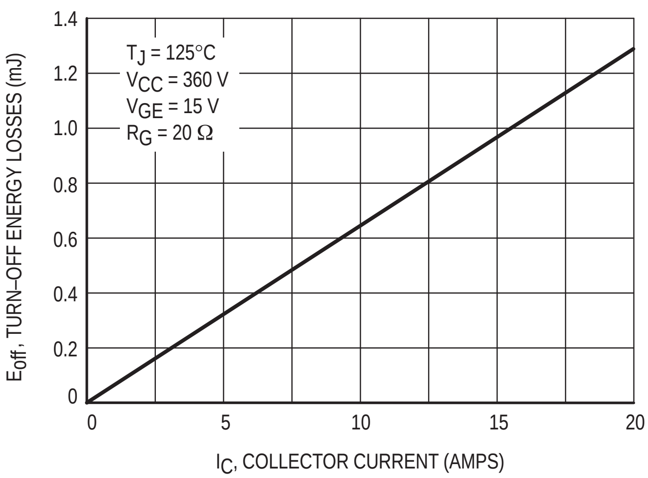


Figure 9. Turn–Off Losses versus Collector Current

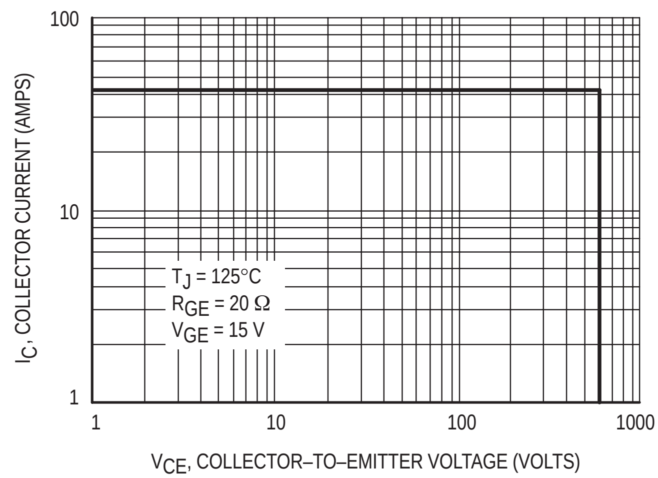


Figure 10. Reverse Biased Safe Operating Area

Product Preview

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

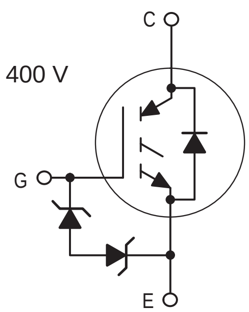
N–Channel Enhancement–Mode Silicon Gate

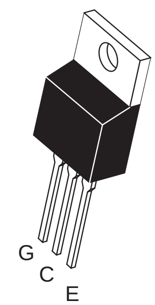
MGP4N60ED

IGBT & DIODE IN TO–220
4.0 A @ 90°C
6.0 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 60 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 3.0 A, 125°C
- Soft Recovery Free Wheeling Diode is Included in the Package
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	6.0 4.0 8.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	62.5 0.51	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	2.0 3.6 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 1.5 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 1.5 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 3.0 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 3.0 Adc)		g_{fe}	—	1.8	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	342	—	pF
Output Capacitance		C_{oes}	—	40	—	
Transfer Capacitance		C_{res}	—	3.0	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 3.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	34	—	ns
Rise Time		t_r	—	30	—	
Turn–Off Delay Time		$t_{d(off)}$	—	36	—	
Fall Time		t_f	—	216	—	
Turn–Off Switching Loss		E_{off}	—	0.10	0.15	mJ
Turn–On Switching Loss		E_{on}	—	TBD	TBD	
Total Switching Loss		E_{ts}	—	TBD	TBD	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 3.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	33	—	ns
Rise Time		t_r	—	32	—	
Turn–Off Delay Time		$t_{d(off)}$	—	56	—	
Fall Time		t_f	—	340	—	
Turn–Off Switching Loss		E_{off}	—	0.17	—	mJ
Turn–On Switching Loss		E_{on}	—	TBD	—	
Total Switching Loss		E_{ts}	—	TBD	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 3.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	18.1	—	nC
		Q_1	—	3.8	—	
		Q_2	—	7.8	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

DIODE CHARACTERISTICS

Diode Forward Voltage Drop (I_{EC} = 1.5 Adc) (I_{EC} = 1.5 Adc, T_J = 125°C) (I_{EC} = 3.0 Adc)		V_{FEC}	 — — —	 1.7 TBD 2.0	 — — 2.3	Vdc
Reverse Recovery Time	(I_F = 3.0 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/µs)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	µC
Reverse Recovery Time	(I_F = 3.0 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/µs, T_J = 125°C)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	µC

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)	L_E	—	7.5	—	nH

Product Preview

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

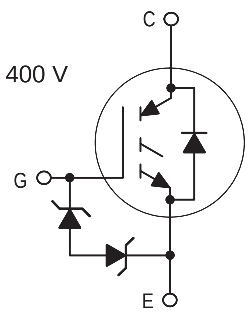
N–Channel Enhancement–Mode Silicon Gate

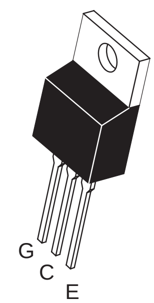
MGP7N60ED

IGBT & DIODE IN TO–220
7.0 A @ 90°C
10 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 70 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On–Voltage 2.0 V typical at 5.0 A, 125°C
- Soft Recovery Free Wheeling Diode is Included in the Package
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	10 7.0 14	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	81 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.5 2.7 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 µAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	µAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	µAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 2.5 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 2.5 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 5.0 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 5.0 Adc)		g_{fe}	—	2.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	610	—	pF
Output Capacitance		C_{oes}	—	60	—	
Transfer Capacitance		C_{res}	—	10	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 5.0 Adc, V_{GE} = 15 Vdc, L = 300 µH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	22	—	ns
Rise Time		t_r	—	24	—	
Turn–Off Delay Time		$t_{d(off)}$	—	64	—	
Fall Time		t_f	—	196	—	
Turn–Off Switching Loss		E_{off}	—	0.20	0.34	mJ
Turn–On Switching Loss		E_{on}	—	TBD	TBD	
Total Switching Loss		E_{ts}	—	TBD	TBD	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 5.0 Adc, V_{GE} = 15 Vdc, L = 300 µH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	31	—	ns
Rise Time		t_r	—	24	—	
Turn–Off Delay Time		$t_{d(off)}$	—	195	—	
Fall Time		t_f	—	220	—	
Turn–Off Switching Loss		E_{off}	—	0.35	—	mJ
Turn–On Switching Loss		E_{on}	—	TBD	—	
Total Switching Loss		E_{ts}	—	TBD	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 5.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	27.2	—	nC
		Q_1	—	7.0	—	
		Q_2	—	13.7	—	

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

DIODE CHARACTERISTICS

Diode Forward Voltage Drop (I_{EC} = 2.5 Adc) (I_{EC} = 2.5 Adc, T_J = 125°C) (I_{EC} = 5.0 Adc)		V_{FEC}	 — — —	 1.7 TBD 2.0	 — — 2.3	Vdc
Reverse Recovery Time	(I_F = 5.0 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	μC
Reverse Recovery Time	(I_F = 5.0 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs, T_J = 125°C)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	μC

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)	L_E	—	7.5	—	nH

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

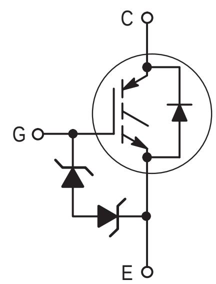
N–Channel Enhancement–Mode Silicon Gate

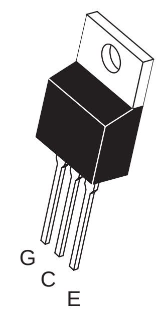
MGP11N60ED

IGBT & DIODE IN TO–220
11 A @ 90°C
15 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected, and rugged short circuit device.

- Industry Standard TO–220 Package
- High Speed: E_{off} = 60 µJ per Amp typical at 125°C
- High Voltage Short Circuit Capability – 10 µs minimum at 125°C, 400 V
- Low On–Voltage — 2.0 V typical at 8.0 A
- Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	15 11 22	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	µs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.3 2.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 4.0 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 4.0 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 8.0 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 8.0 Adc)		g_{fe}	—	3.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	779	—	pF
Output Capacitance		C_{oes}	—	81	—	
Transfer Capacitance		C_{res}	—	13	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include "tail"	$t_{d(on)}$	—	46	—	ns
Rise Time		t_r	—	34	—	
Turn–Off Delay Time		$t_{d(off)}$	—	102	—	
Fall Time		t_f	—	226	—	
Turn–Off Switching Loss		E_{off}	—	0.32	0.40	mJ
Turn–On Switching Loss		E_{on}	—	0.11	—	
Total Switching Loss		E_{ts}	—	0.43	—	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include "tail"	$t_{d(on)}$	—	42	—	ns
Rise Time		t_r	—	26	—	
Turn–Off Delay Time		$t_{d(off)}$	—	214	—	
Fall Time		t_f	—	228	—	
Turn–Off Switching Loss		E_{off}	—	0.48	—	mJ
Turn–On Switching Loss		E_{on}	—	0.16	—	
Total Switching Loss		E_{ts}	—	0.64	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	39.2	—	nC
		Q_1	—	8.7	—	
		Q_2	—	17.4	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 3.25 Adc)		V_{FEC}	—	1.63	—	Vdc
(I_{EC} = 3.25 Adc, T_J = 125°C)			—	1.24	—	
(I_{EC} = 6.5 Adc)			1.7	2.0	2.3	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 8.0 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/µs)	t_{rr}	—	57	—	ns
		t_a	—	18	—	
		t_b	—	39	—	
Reverse Recovery Stored Charge		Q_{RR}	—	107	—	µC
Reverse Recovery Time	(I_F = 8.0 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/µs, T_J = 125°C)	t_{rr}	—	91	—	ns
		t_a	—	28	—	
		t_b	—	63	—	
Reverse Recovery Stored Charge		Q_{RR}	—	275	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

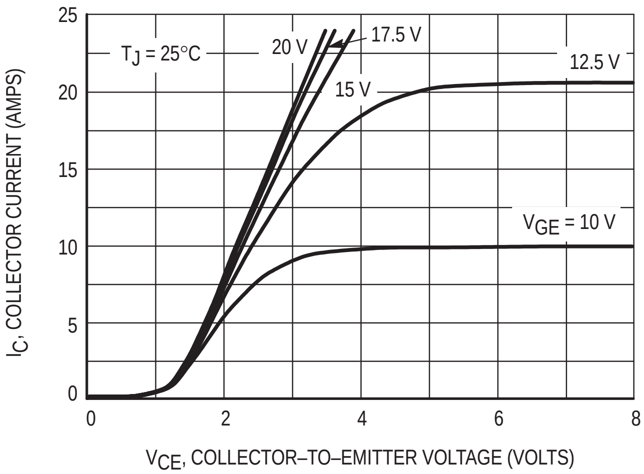


Figure 1. Output Characteristics

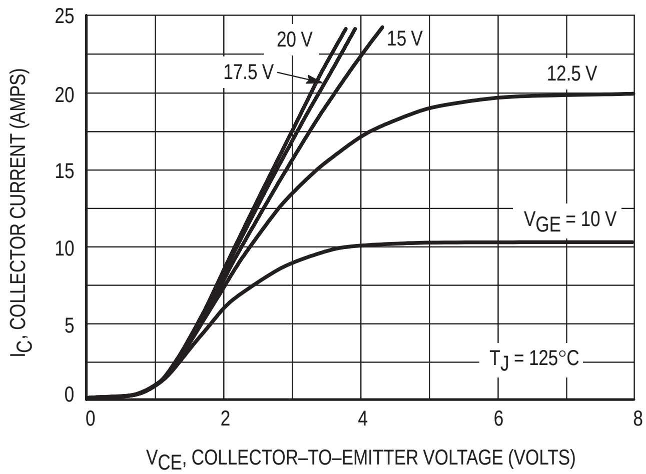


Figure 2. Output Characteristics

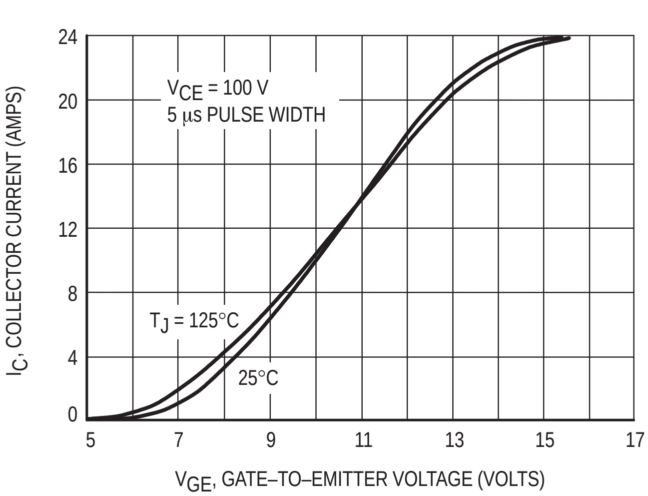


Figure 3. Transfer Characteristics

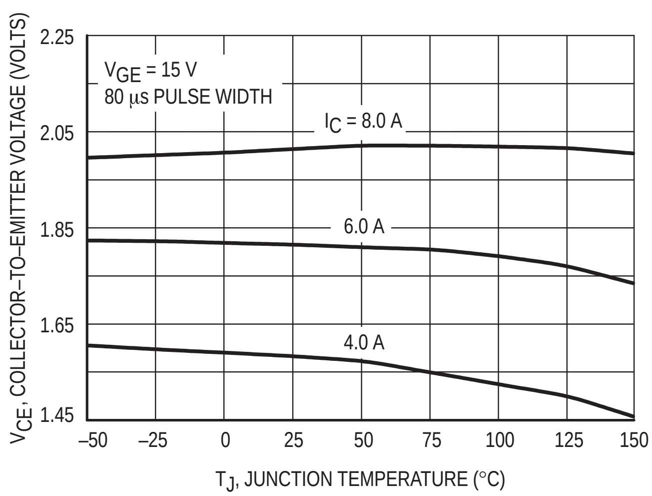


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

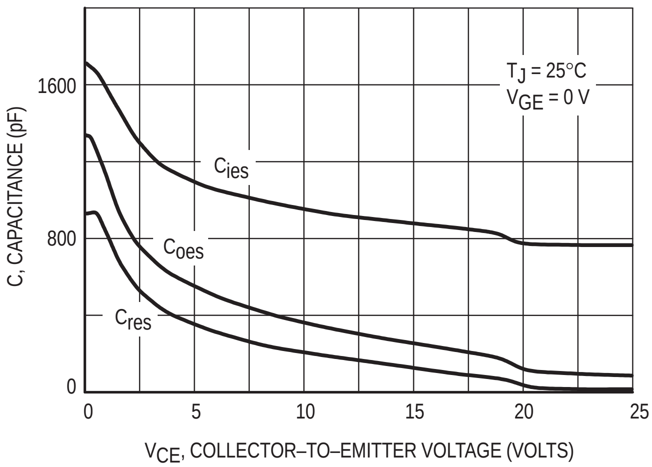


Figure 5. Capacitance Variation

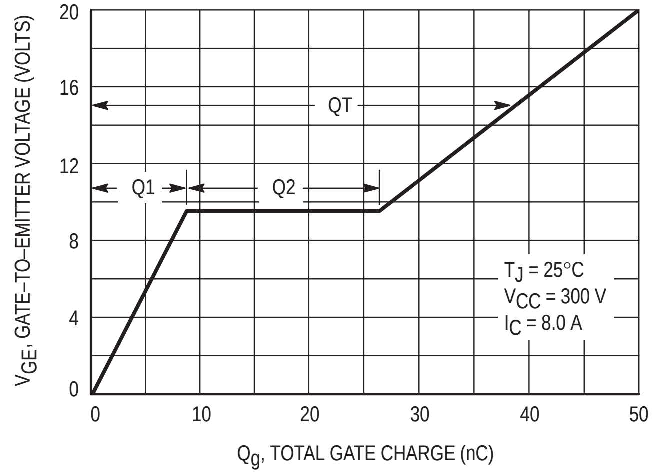


Figure 6. Gate–To–Emitter Voltage versus Total Charge

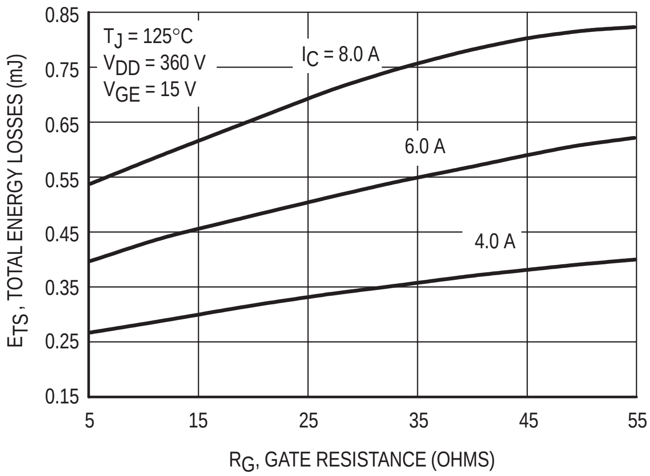


Figure 7. Total Energy Losses versus Gate Resistance

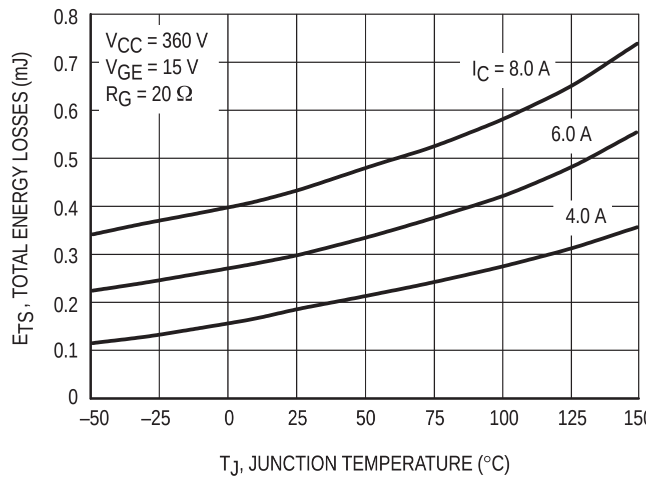


Figure 8. Total Energy Losses versus Junction Temperature

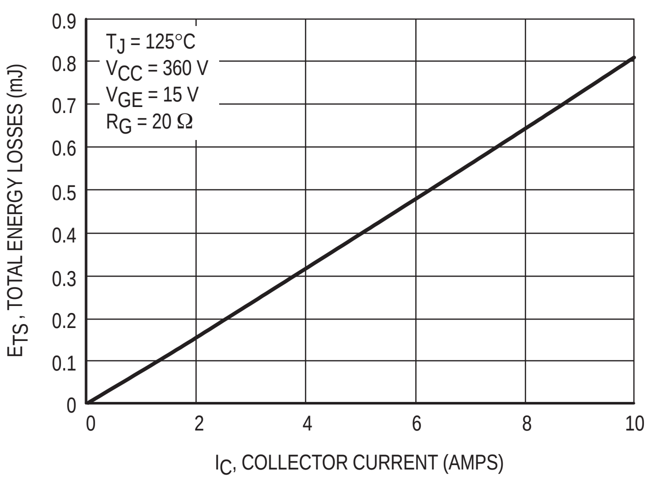


Figure 9. Total Energy Losses versus Collector Current

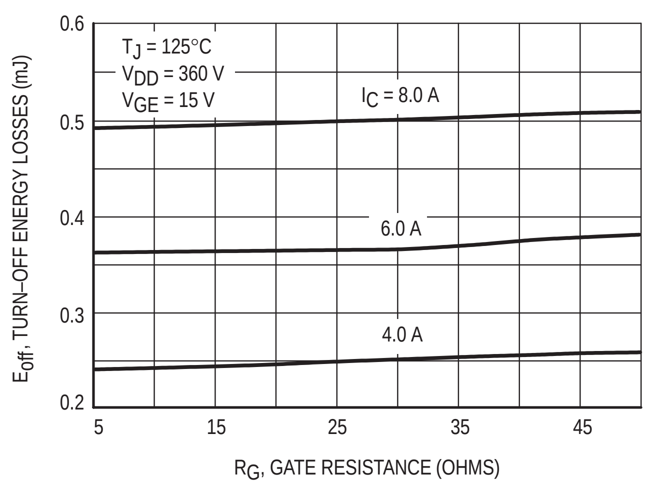


Figure 10. Turn–Off Losses versus Gate Resistance

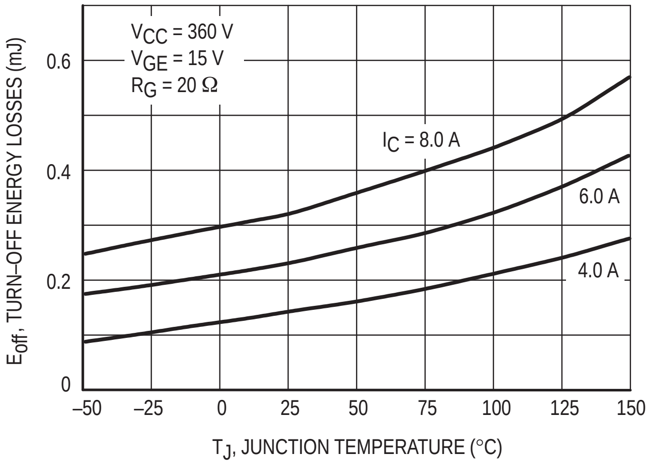


Figure 11. Turn–Off Losses versus Gate Resistance

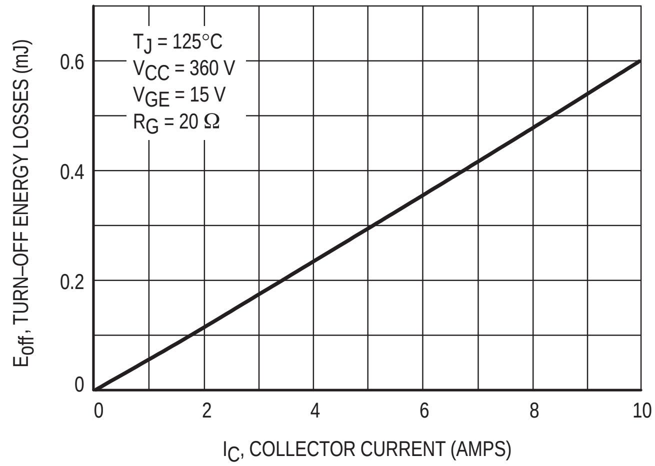


Figure 12. Turn–Off Losses versus Junction Temperature

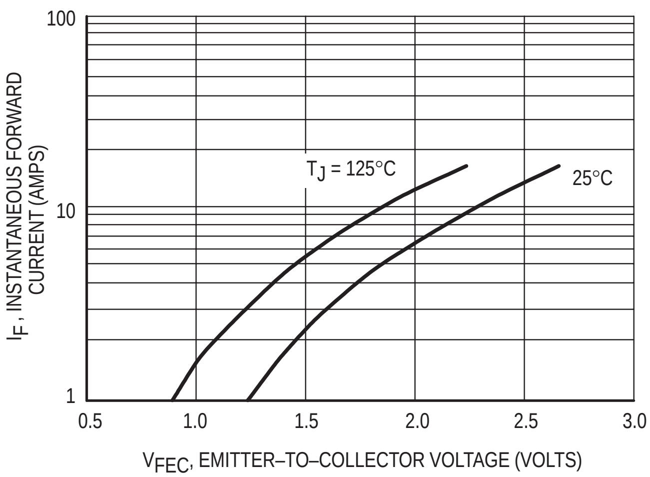


Figure 13. Forward Characteristics versus Current

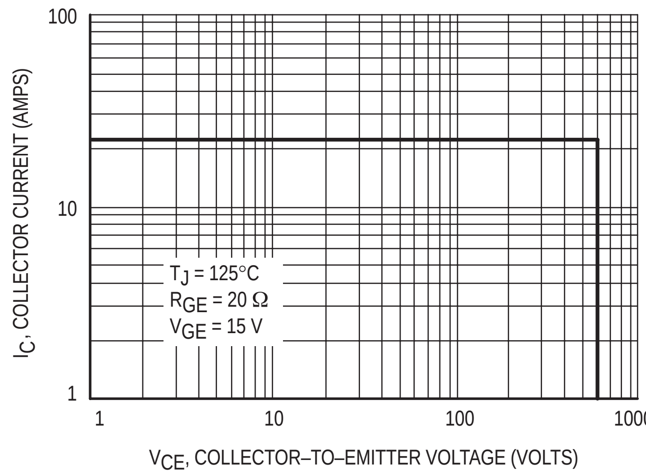


Figure 14. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

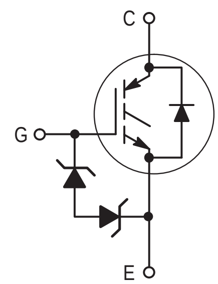
N–Channel Enhancement–Mode Silicon Gate

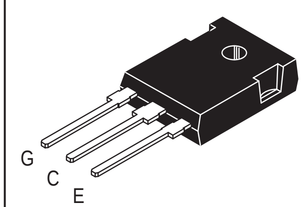
MGW14N60ED

IGBT IN TO–247
14 A @ 90°C
18 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–247 Package
- High Speed: E_{off} = 60 µJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 µs minimum at 125°C, 400V
- Low On–Voltage — 2.0V typical at 10A, 125°C
- Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 340K–01
STYLE 4
TO–247 AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	18 14 28	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	112 0.89	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	µs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.1 1.9 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS(1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)		g_{fe}	—	5.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1020	—	pF
Output Capacitance		C_{oes}	—	104	—	
Transfer Capacitance		C_{res}	—	17	—	
SWITCHING CHARACTERISTICS(1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	38	—	ns
Rise Time		t_r	—	40	—	
Turn–Off Delay Time		$t_{d(off)}$	—	120	—	
Fall Time		t_f	—	204	—	
Turn–Off Switching Loss		E_{off}	—	0.35	0.45	mJ
Turn–On Switching Loss		E_{on}	—	0.27	0.35	
Total Switching Loss		E_{ts}	—	0.62	0.80	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	32	—	ns
Rise Time		t_r	—	30	—	
Turn–Off Delay Time		$t_{d(off)}$	—	208	—	
Fall Time		t_f	—	212	—	
Turn–Off Switching Loss		E_{off}	—	0.63	—	mJ
Turn–On Switching Loss		E_{on}	—	0.40	—	
Total Switching Loss		E_{ts}	—	1.03	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	57	—	nC
		Q_1	—	12	—	
		Q_2	—	25	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 5.0 Adc)		V_{FEC}	—	1.6	1.9	Vdc
(I_{EC} = 5.0 Adc, T_J = 125°C)			—	1.3	—	
(I_{EC} = 10 Adc)			1.7	2.0	2.3	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 10 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs)	t_{rr}	—	75	—	ns
		t_a	—	31	—	
		t_b	—	44	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.16	—	μC
Reverse Recovery Time	(I_F = 10 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs, T_J = 125°C)	t_{rr}	—	139	—	ns
		t_a	—	45	—	
		t_b	—	94	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.40	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

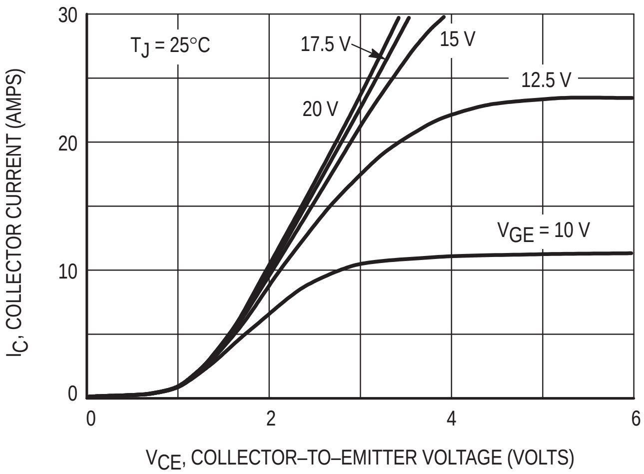


Figure 1. Output Characteristics

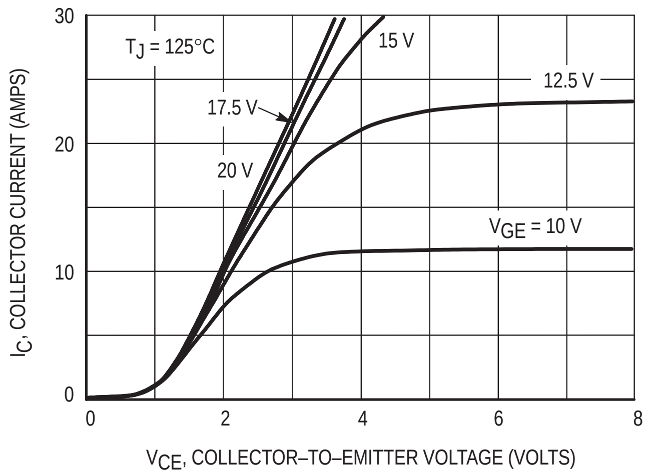


Figure 2. Output Characteristics

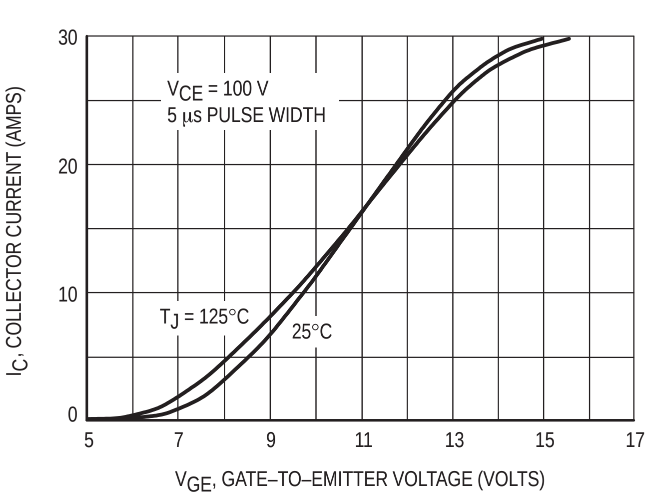


Figure 3. Transfer Characteristics

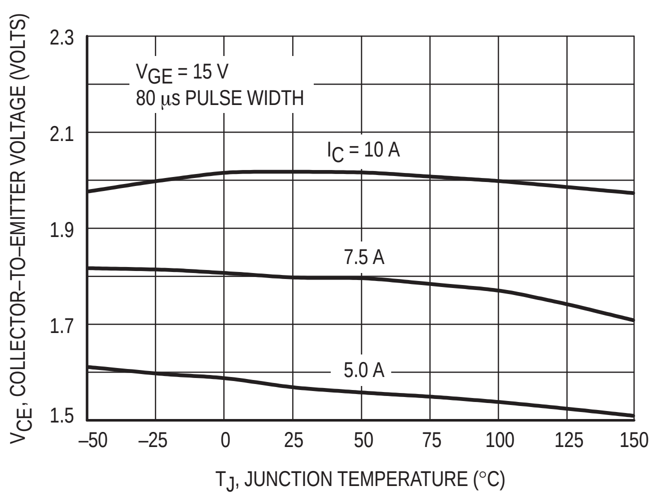


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

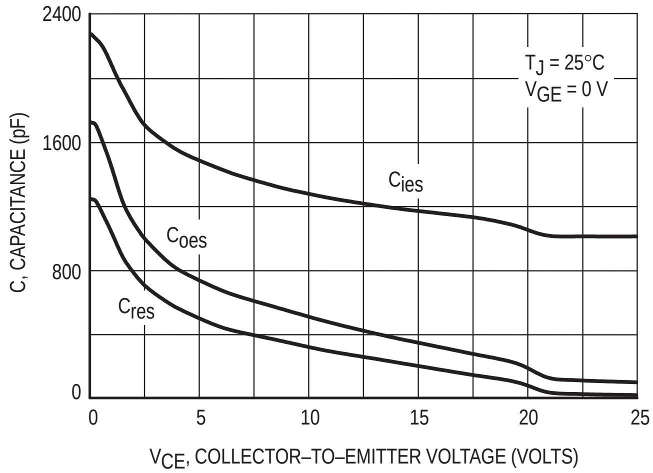


Figure 5. Capacitance Variation

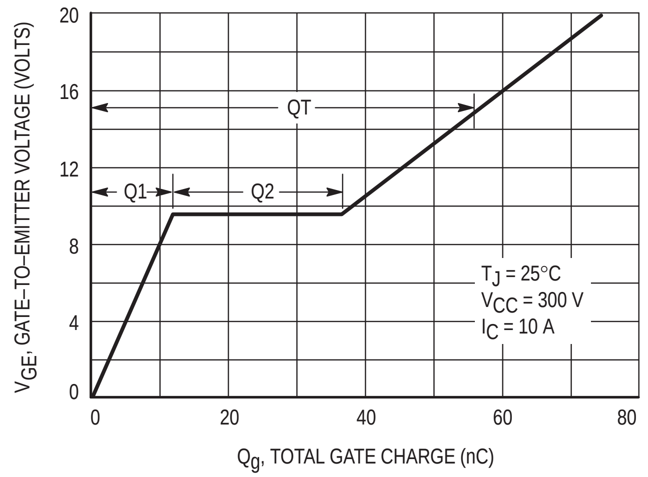


Figure 6. Gate–to–Emitter Voltage versus Total Charge

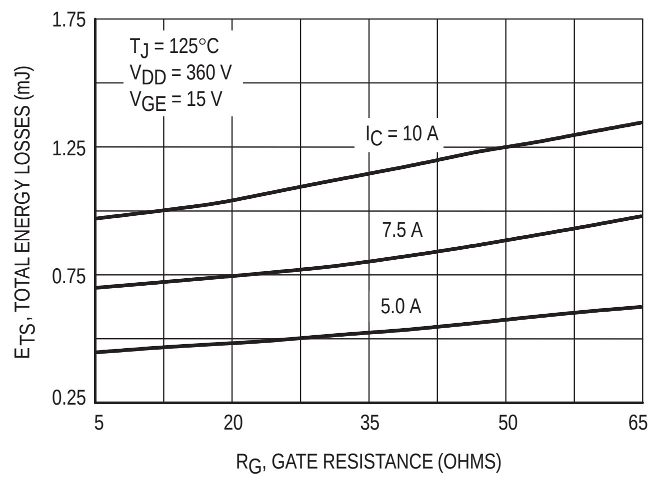


Figure 7. Total Energy Losses versus Gate Resistance

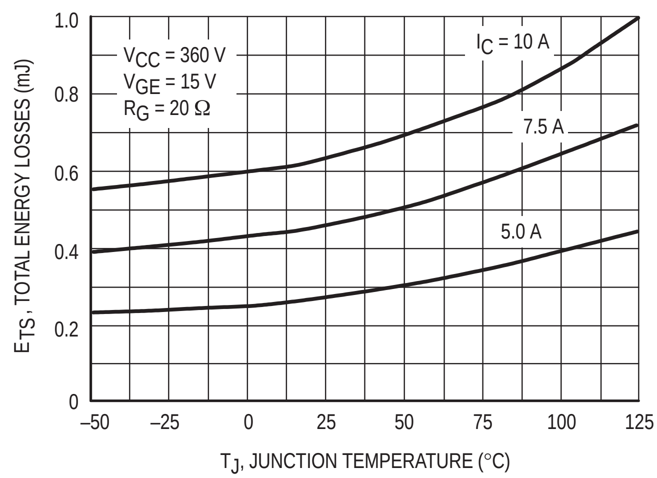


Figure 8. Total Energy Losses versus Junction Temperature

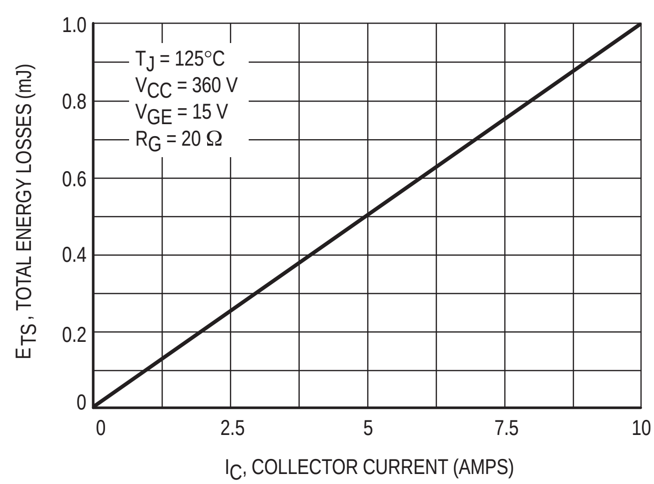


Figure 9. Total Energy Losses versus Collector Current

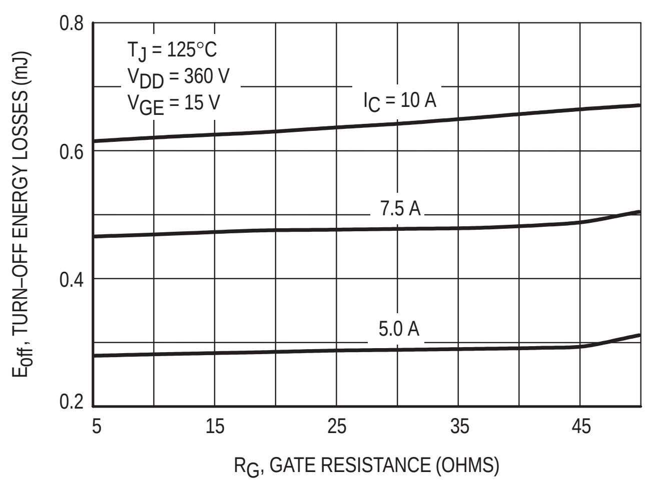


Figure 10. Turn–Off Energy Losses versus Gate Resistance

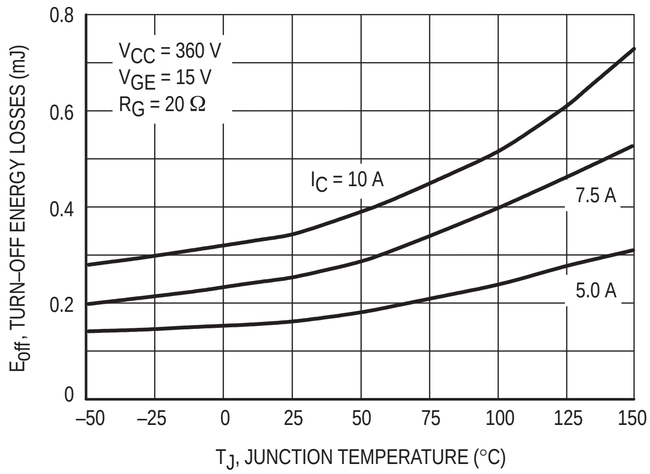


Figure 11. Turn–Off Energy Losses versus Junction Temperature

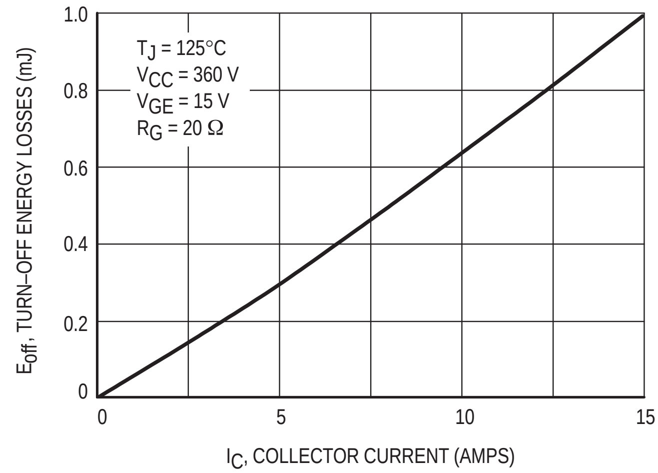


Figure 12. Turn–Off Energy Losses versus Collector Current

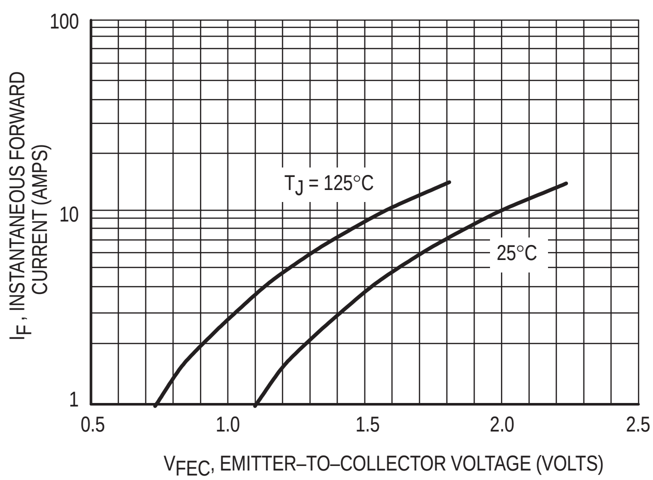


Figure 13. Forward Characteristics versus Current

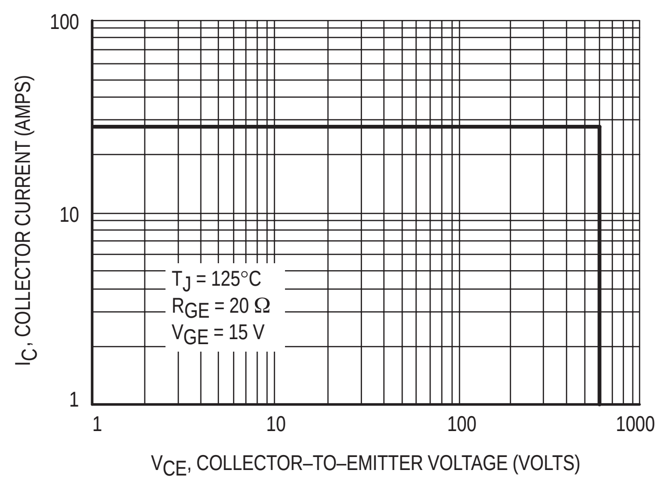


Figure 14. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

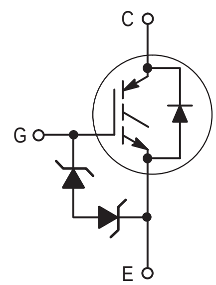
N–Channel Enhancement–Mode Silicon Gate

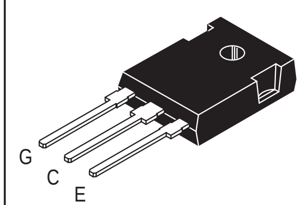
MGW21N60ED

IGBT IN TO–247
21 A @ 90°C
31 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected, and rugged short circuit device.

- Industry Standard TO–247 Package
- High Speed: E_{off} = 65 µJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 µs minimum at 125°C, 400 V
- Low On–Voltage — 2.1 V typical at 20 A, 125°C
- Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 340K–01
STYLE 4
TO–247 AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	31 21 42	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	142 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	µs
Thermal Resistance — Junction to Case – IGBT — Junction to Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.88 1.4 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 10 Adc)		$V_{CE(on)}$	—	1.7	2.1	Vdc
(V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 20 Adc)			—	2.2	2.5	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	8.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1605	—	pF
Output Capacitance		C_{oes}	—	146	—	
Transfer Capacitance		C_{res}	—	23	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	29	—	ns
Rise Time		t_r	—	60	—	
Turn–Off Delay Time		$t_{d(off)}$	—	238	—	
Fall Time		t_f	—	140	—	
Turn–Off Switching Loss		E_{off}	—	0.8	1.15	mJ
Turn–On Switching Loss		E_{on}	—	0.6	—	
Total Switching Loss		E_{ts}	—	1.4	—	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	28	—	ns
Rise Time		t_r	—	62	—	
Turn–Off Delay Time		$t_{d(off)}$	—	338	—	
Fall Time		t_f	—	220	—	
Turn–Off Switching Loss		E_{off}	—	1.3	—	mJ
Turn–On Switching Loss		E_{on}	—	0.8	—	
Total Switching Loss		E_{ts}	—	2.1	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	86	—	nC
		Q_1	—	18	—	
		Q_2	—	39	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 10 Adc)		V_{FEC}	—	1.6	1.9	Vdc
(I_{EC} = 10 Adc, T_J = 125°C)			—	1.3	—	
(I_{EC} = 17 Adc)			1.7	2.0	2.3	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 20 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/µs)	t_{rr}	—	94	—	ns
		t_a	—	32	—	
		t_b	—	62	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.16	—	µC
Reverse Recovery Time	(I_F = 20 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/µs, T_J = 125°C)	t_{rr}	—	145	—	ns
		t_a	—	50	—	
		t_b	—	95	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.75	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

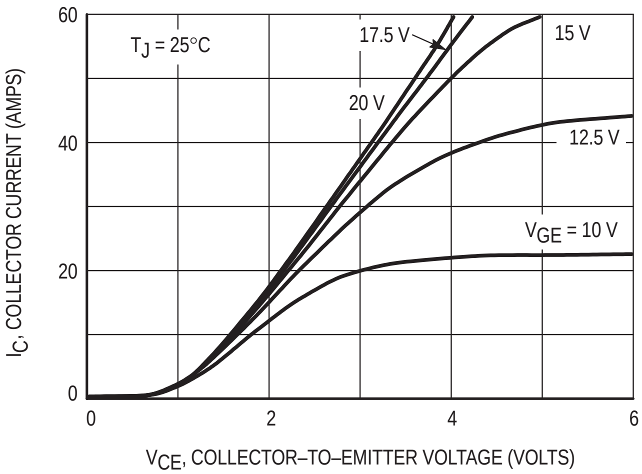


Figure 1. Output Characteristics

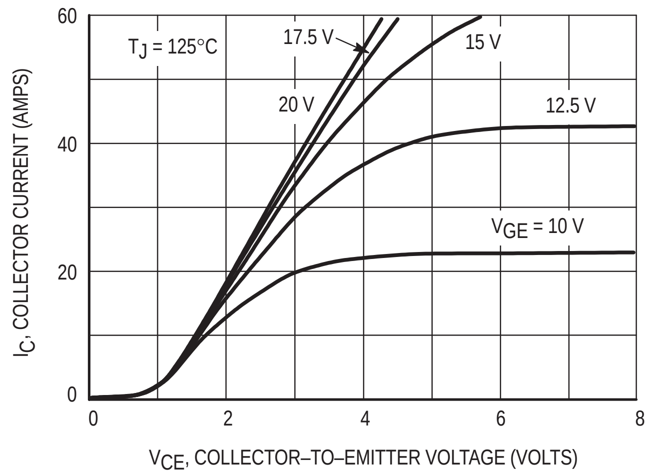


Figure 2. Output Characteristics

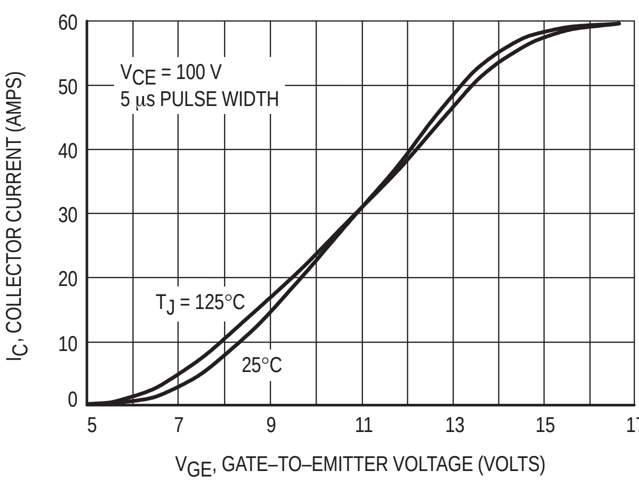


Figure 3. Transfer Characteristics

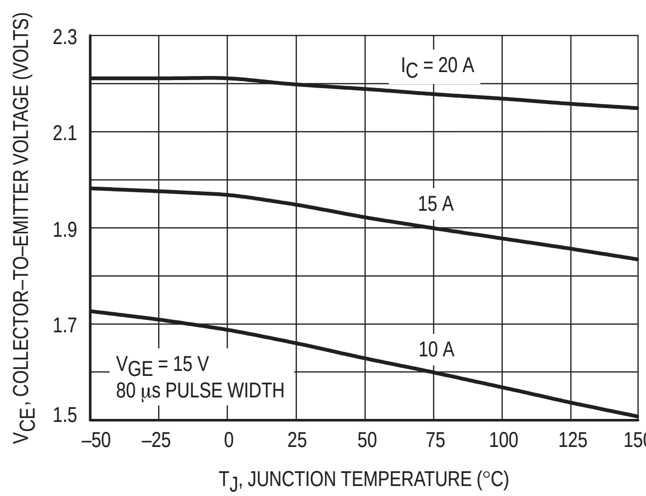


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

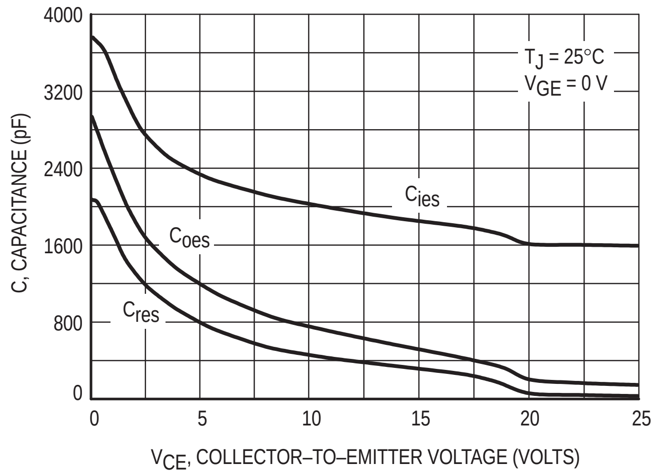


Figure 5. Capacitance Variation

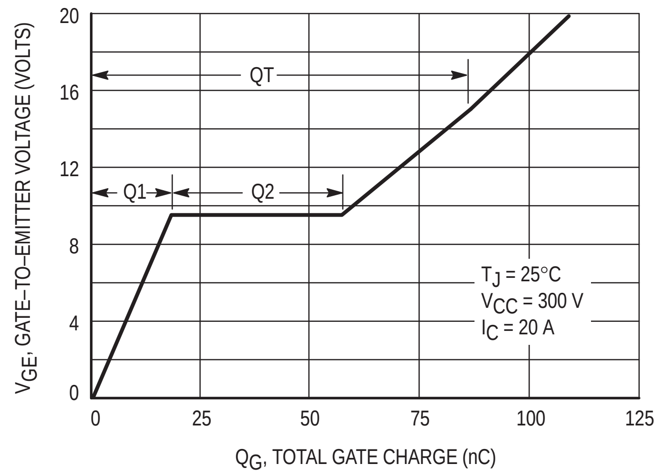


Figure 6. Gate–To–Emitter Voltage versus Total Charge

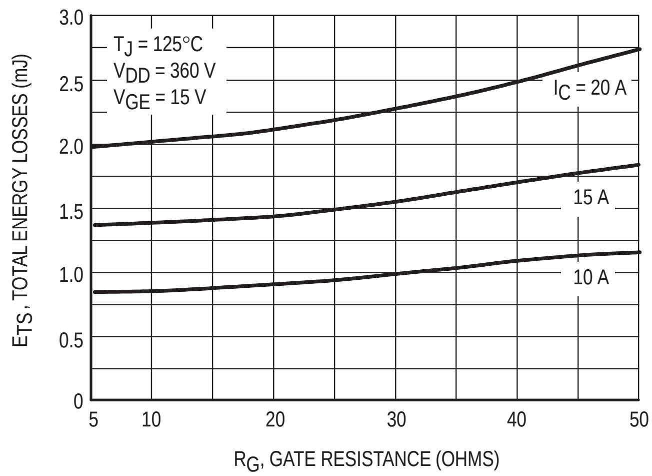


Figure 7. Total Energy Losses versus Gate Resistance

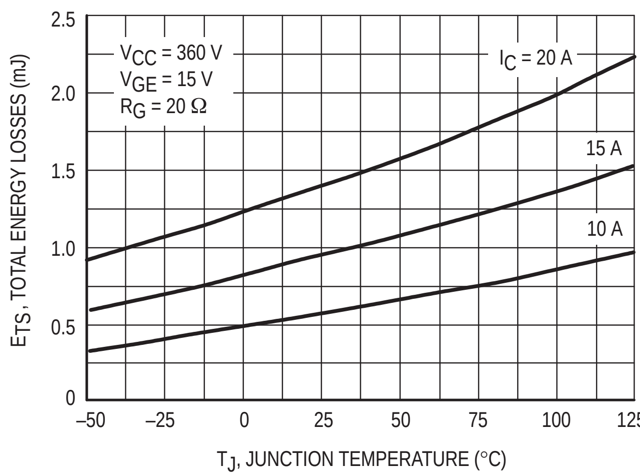


Figure 8. Total Energy Losses versus Junction Temperature

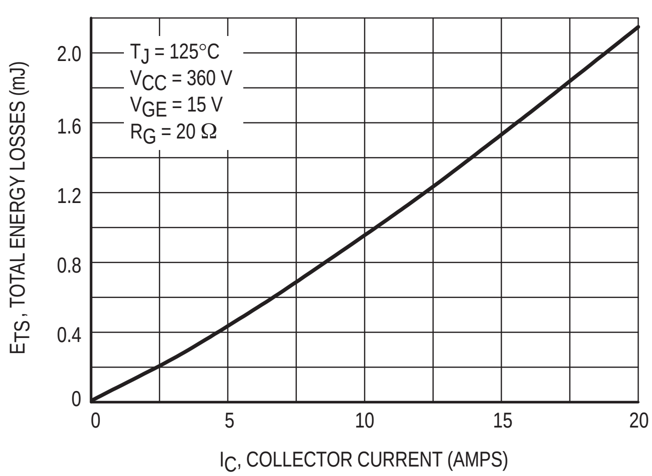


Figure 9. Total Energy Losses versus Collector Current

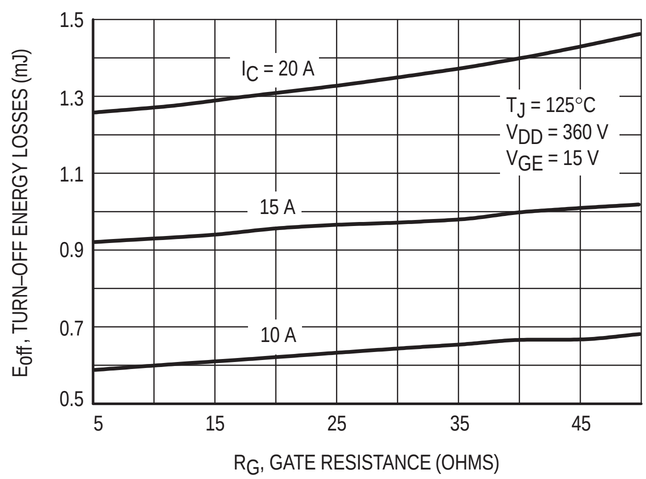


Figure 10. Turn–Off Losses versus Gate Resistance

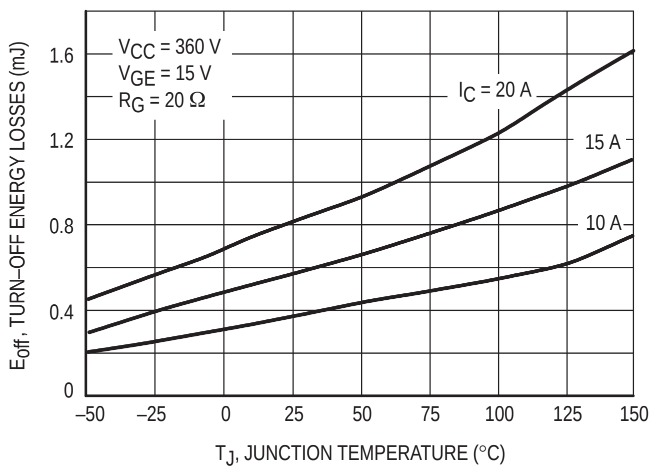


Figure 11. Turn–Off Losses versus Junction Temperature

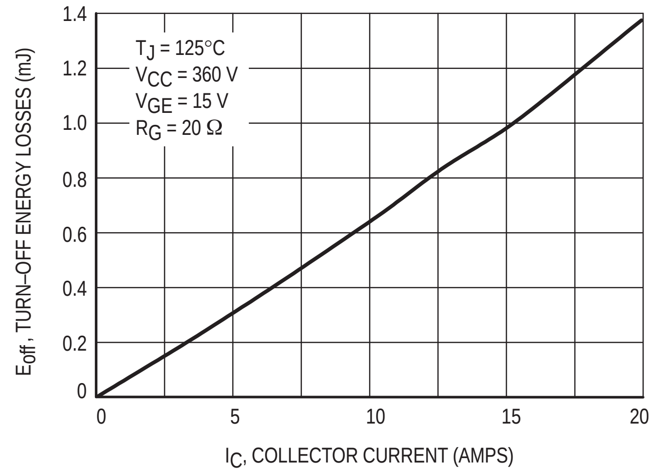


Figure 12. Turn–Off Losses versus Collector Current

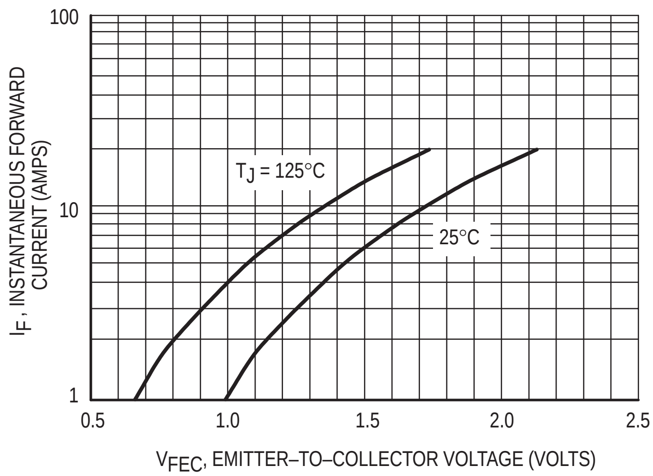


Figure 13. Forward Characteristics versus Current

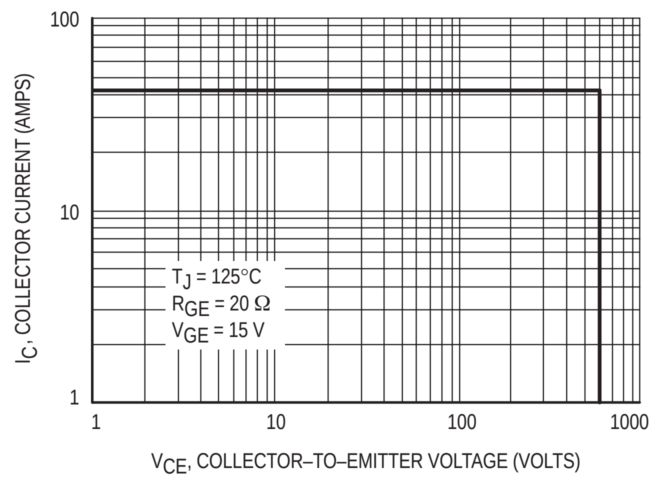


Figure 14. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

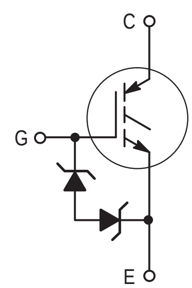
N–Channel Enhancement–Mode Silicon Gate

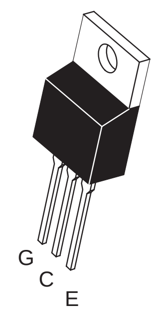
MGP15N60U

IGBT IN TO–220
15 A @ 90°C
26 A @ 25°C
600 VOLTS
VERY LOW
ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. It also provides low on–voltage which results in efficient operation at high current.

- Industry Standard TO–220 Package
- High Speed E_{off}: 63 μJ/A typical at 125°C
- Low On–Voltage – 1.7 V typical at 8.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	26 15 52	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 4.0 Adc)		$V_{CE(on)}$	—	1.4	1.7	Vdc
(V_{GE} = 15 Vdc, I_C = 4.0 Adc, T_J = 125°C)			—	1.3	—	
(V_{GE} = 15 Vdc, I_C = 8.0 Adc)			—	1.7	2.0	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	3.0	5.5	7.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 8.0 Adc)		g_{fe}	—	7.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	806	—	pF
Output Capacitance		C_{oes}	—	78	—	
Transfer Capacitance		C_{res}	—	13	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	35	—	ns
Rise Time		t_r	—	34	—	
Turn–Off Delay Time		$t_{d(off)}$	—	105	—	
Fall Time		t_f	—	200	—	
Turn–Off Switching Loss		E_{off}	—	250	—	μJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	36	—	ns
Rise Time		t_r	—	39	—	
Turn–Off Delay Time		$t_{d(off)}$	—	206	—	
Fall Time		t_f	—	255	—	
Turn–Off Switching Loss		E_{off}	—	510	—	μJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 8.0 Adc, V_{GE} = 15 Vdc)	Q_T	—	39.2	—	nC
		Q_1	—	8.7	—	
		Q_2	—	17.4	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

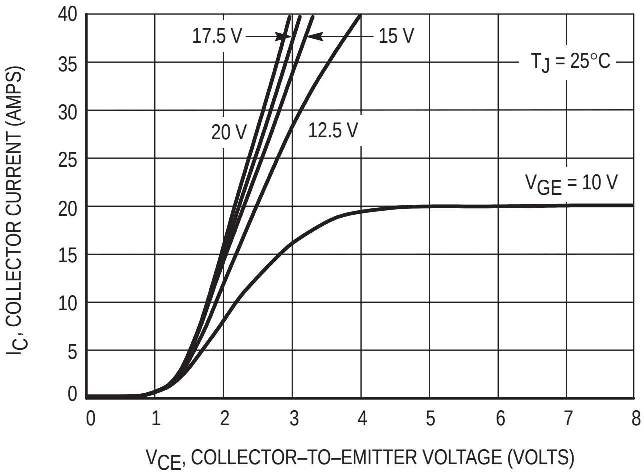


Figure 1. Output Characteristics

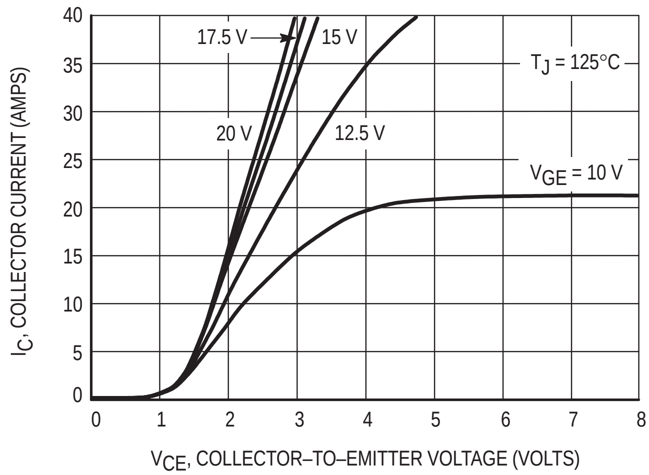


Figure 2. Output Characteristics

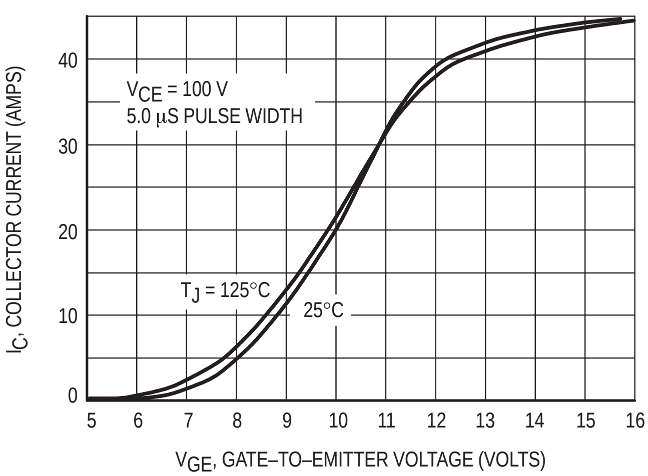


Figure 3. Transfer Characteristics

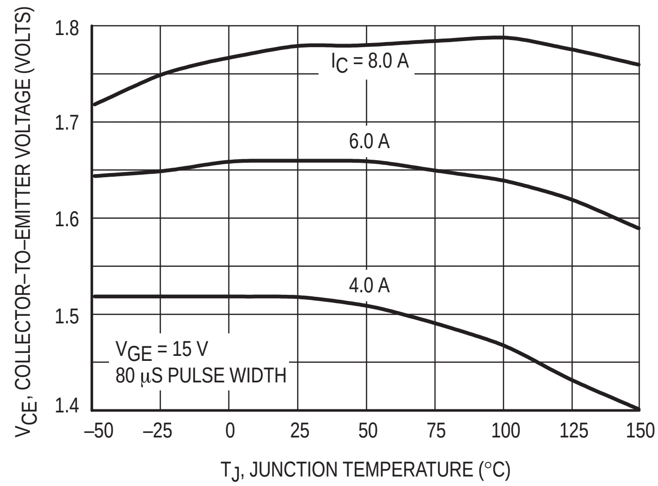


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

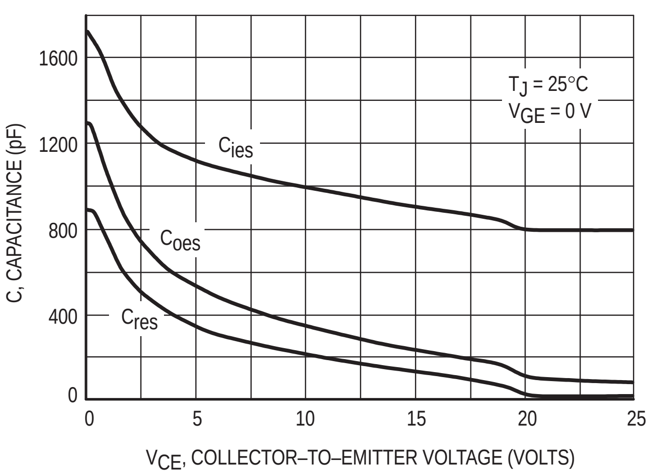


Figure 5. Capacitance Variation

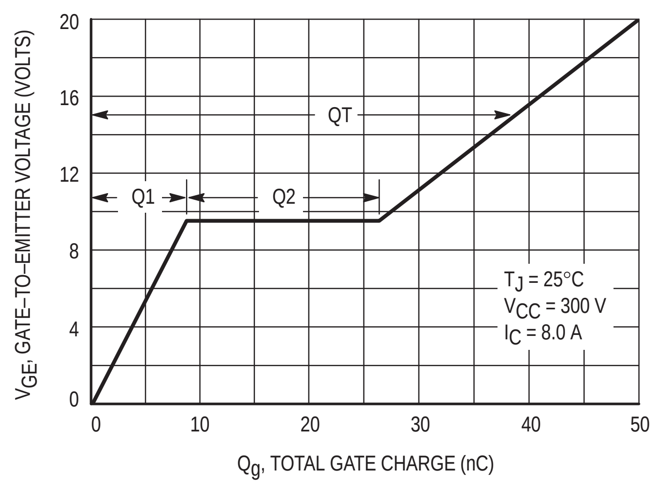


Figure 6. Gate–To–Emitter Voltage versus Total Charge

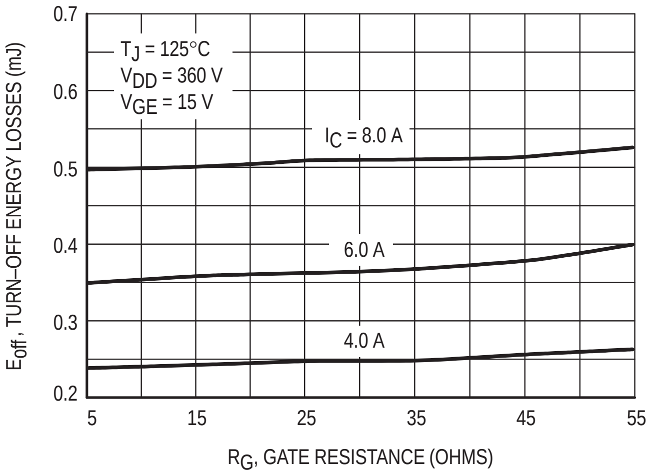


Figure 7. Turn–Off Energy Losses versus Gate Resistance

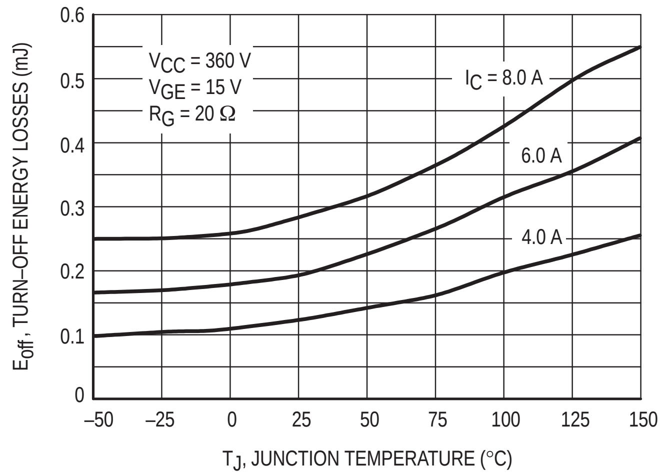


Figure 8. Turn–Off Energy Losses versus Junction Temperature

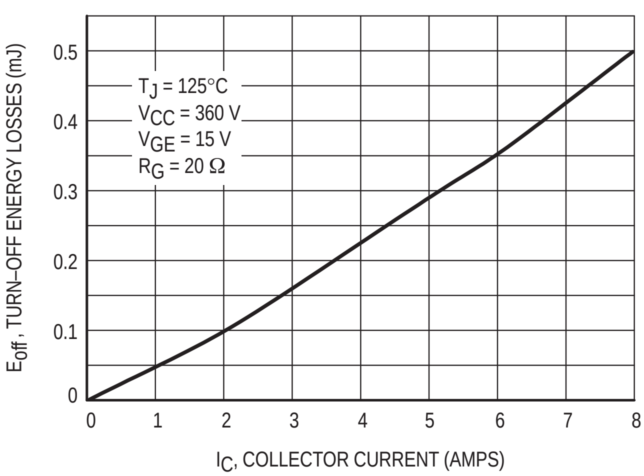


Figure 9. Turn–Off Energy Losses versus Collector Current

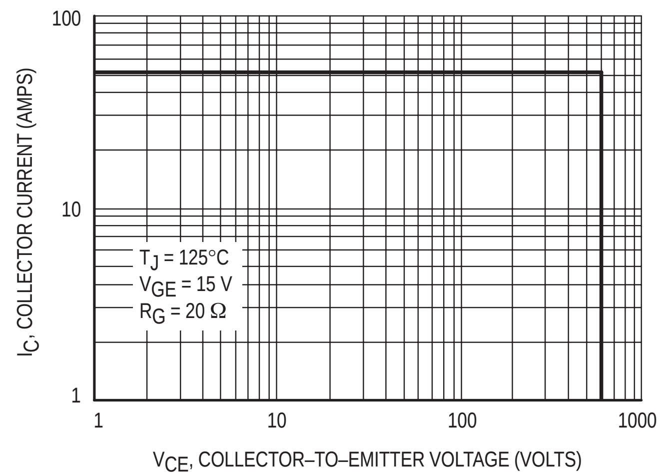


Figure 10. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

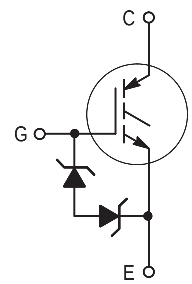
N–Channel Enhancement–Mode Silicon Gate

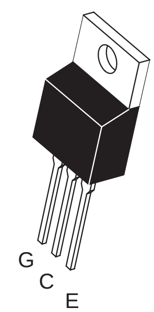
MGP20N60U

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. It also provides low on–voltage which results in efficient operation at high current.

- Industry Standard TO–220 Package
- High Speed E_{off}: 63 μJ/A typical at 125°C
- Low On–Voltage – 1.7 V typical at 10 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes

IGBT IN TO–220
20 A @ 90°C
31 A @ 25°C
600 VOLTS
VERY LOW
ON–VOLTAGE





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	31 20 62	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	112 0.89	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.12 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 µAdc) Temperature Coefficient (Positive)	$V_{(BR)CES}$	 600 —	 — 870	 — —	Vdc mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)	$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)	I_{CES}	 — —	 — —	 10 200	µAdc
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)	I_{GES}	—	—	50	µAdc
ON CHARACTERISTICS (1)					
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc) (V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 10 Adc)	$V_{CE(on)}$	 — — —	 1.4 1.3 1.7	 1.7 — 2.0	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	$V_{GE(th)}$	 3.0 —	 5.0 10	 7.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)	g_{fe}	—	7.0	—	Mhos

DYNAMIC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1060	—	pF
Output Capacitance		C_{oes}	—	99	—	
Transfer Capacitance		C_{res}	—	15	—	

SWITCHING CHARACTERISTICS (1)

Characteristic		Symbol	Min	Typ	Max	Unit
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 µH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	43	—	ns
Rise Time		t_r	—	45	—	
Turn–Off Delay Time		$t_{d(off)}$	—	144	—	
Fall Time		t_f	—	175	—	
Turn–Off Switching Loss		E_{off}	—	340	—	µJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 µH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	43	—	ns
Rise Time		t_r	—	56	—	
Turn–Off Delay Time		$t_{d(off)}$	—	235	—	
Fall Time		t_f	—	220	—	
Turn–Off Switching Loss		E_{off}	—	625	—	µJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	57	—	nC
		Q_1	—	12	—	
		Q_2	—	25	—	

INTERNAL PACKAGE INDUCTANCE

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)	L_E	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

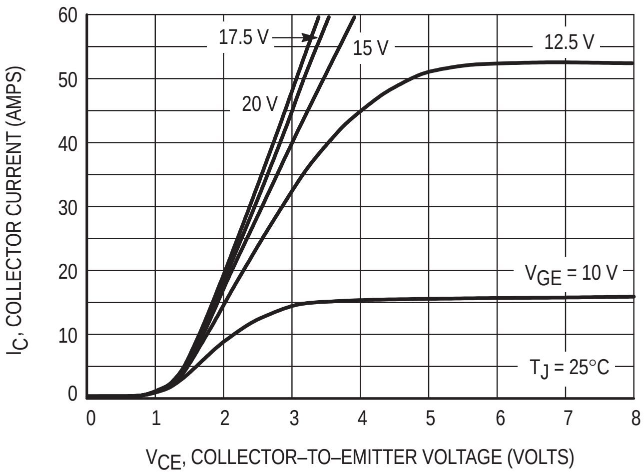


Figure 1. Output Characteristics

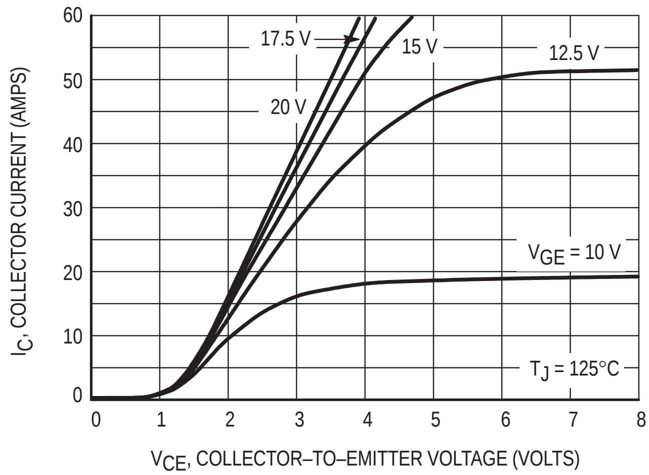


Figure 2. Output Characteristics

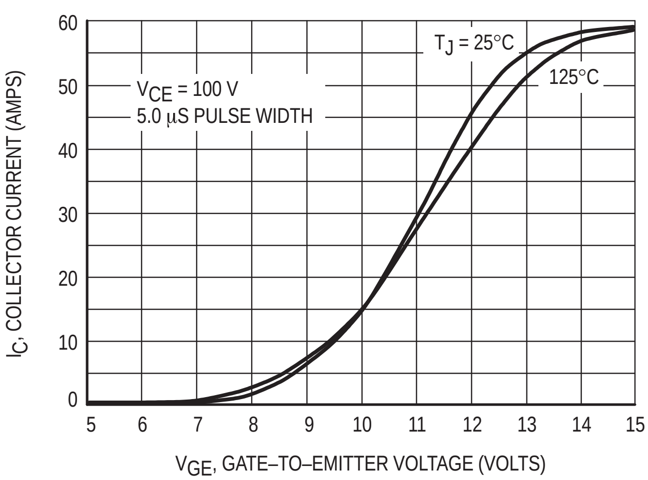


Figure 3. Transfer Characteristics

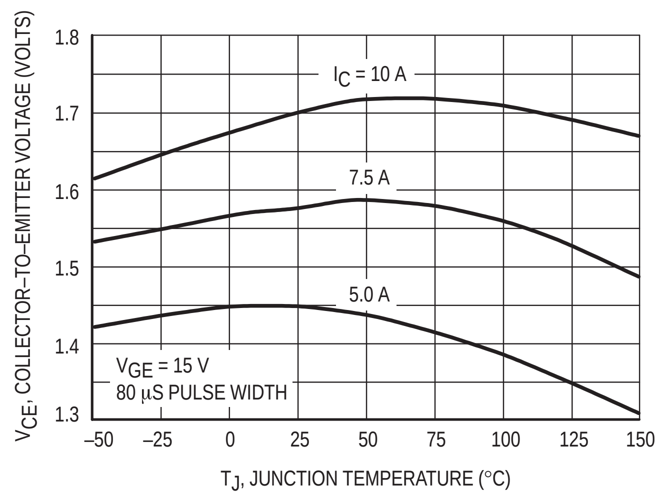


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

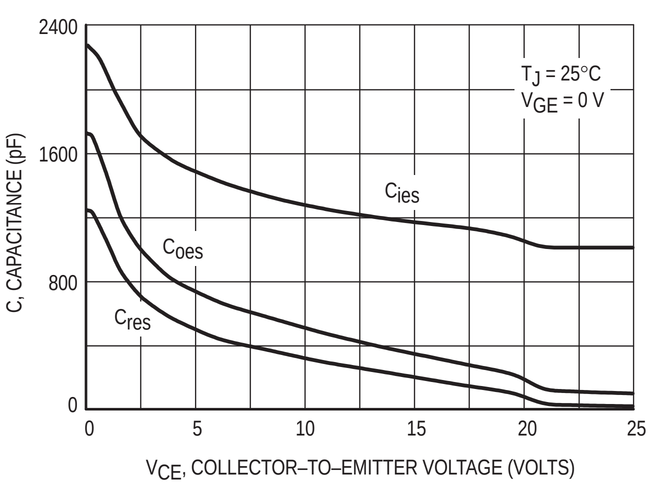


Figure 5. Capacitance Variation

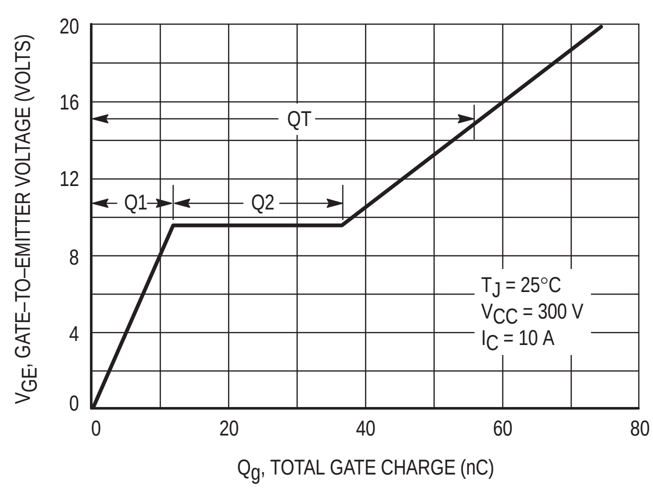


Figure 6. Gate–To–Emitter Voltage versus Total Charge

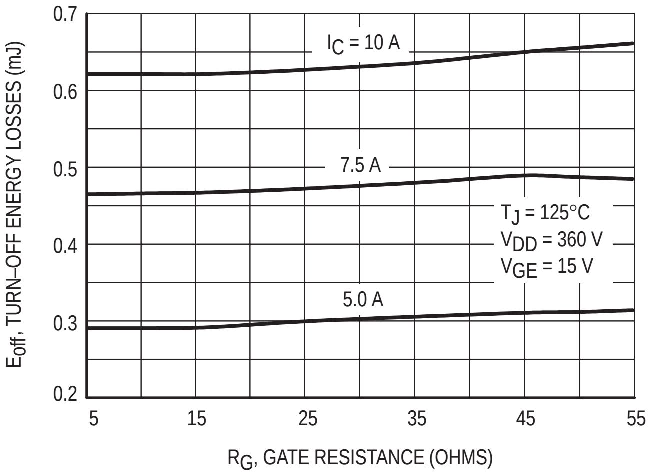


Figure 7. Turn–Off Energy Losses versus Gate Resistance

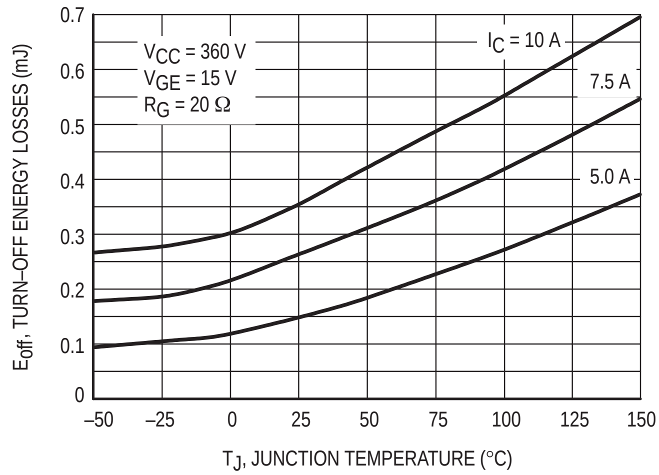


Figure 8. Turn–Off Energy Losses versus Junction Temperature

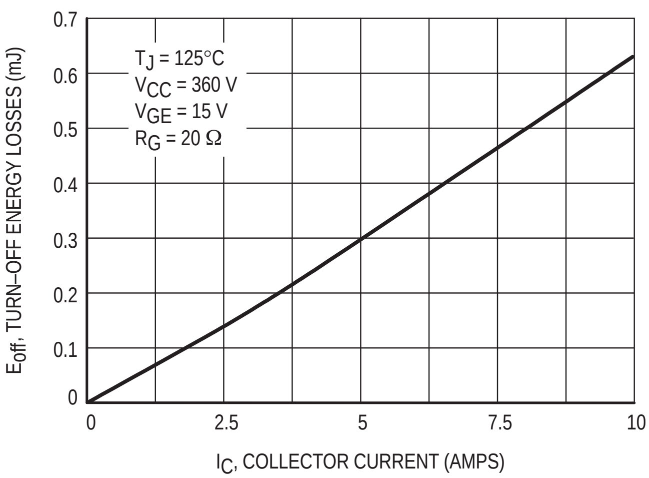


Figure 9. Turn–Off Energy Losses versus Collector Current

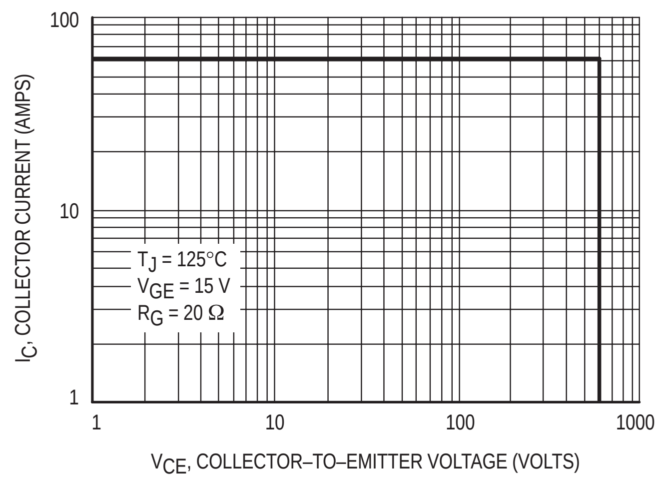


Figure 10. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

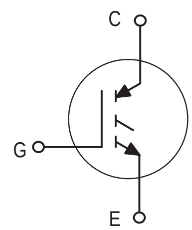
MGW12N120

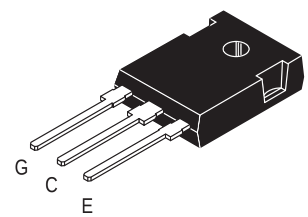
Motorola Preferred Device

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 150 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination

IGBT IN TO–247
12 A @ 90°C
20 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED





CASE 340K–01
STYLE 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	20 12 40	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.98	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)	$V_{(BR)CES}$	1200	—	—	Vdc
Temperature Coefficient (Positive)		—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)	$V_{(BR)ECS}$	25	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)	I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)	I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)					
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc)	$V_{CE(on)}$	—	2.51	3.37	Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)		—	2.36	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)		—	3.5	4.42	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)	$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)		—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)	g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	930	—	pF
Output Capacitance	C_{oes}	—	126	—	
Transfer Capacitance	C_{res}	—	16	—	
SWITCHING CHARACTERISTICS (1)					
Turn–On Delay Time (V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	74	—	ns
Rise Time	t_r	—	83	—	
Turn–Off Delay Time	$t_{d(off)}$	—	76	—	
Fall Time	t_f	—	231	—	
Turn–Off Switching Loss	E_{off}	—	0.55	1.33	mJ
Turn–On Delay Time (V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	66	—	ns
Rise Time	t_r	—	87	—	
Turn–Off Delay Time	$t_{d(off)}$	—	120	—	
Fall Time	t_f	—	575	—	
Turn–Off Switching Loss	E_{off}	—	1.49	—	mJ
Gate Charge (V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	31	—	nC
	Q_1	—	13	—	
	Q_2	—	14	—	
INTERNAL PACKAGE INDUCTANCE					
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)	L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

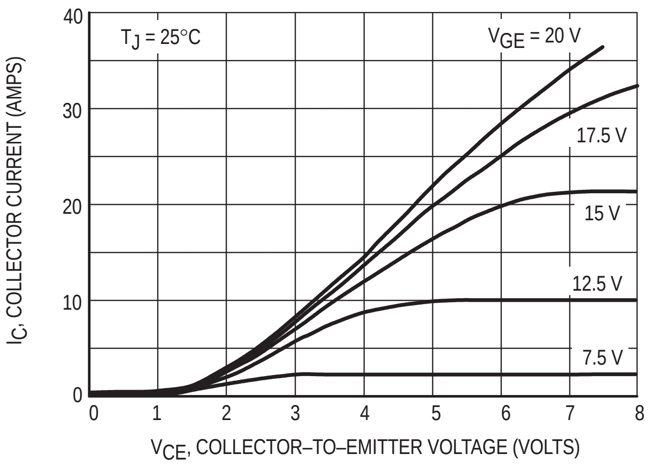


Figure 1. Output Characteristics

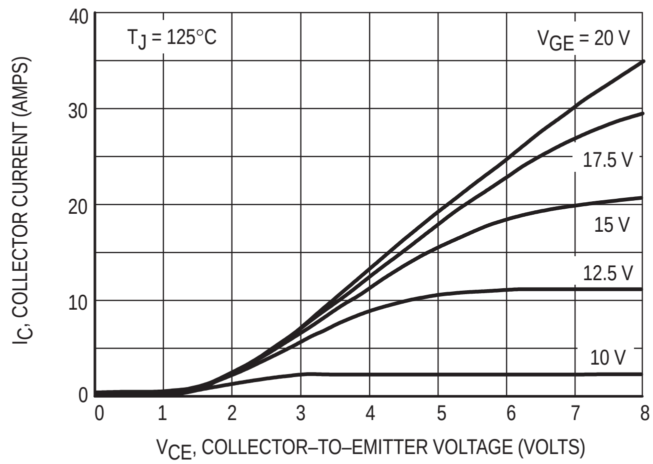


Figure 2. Output Characteristics

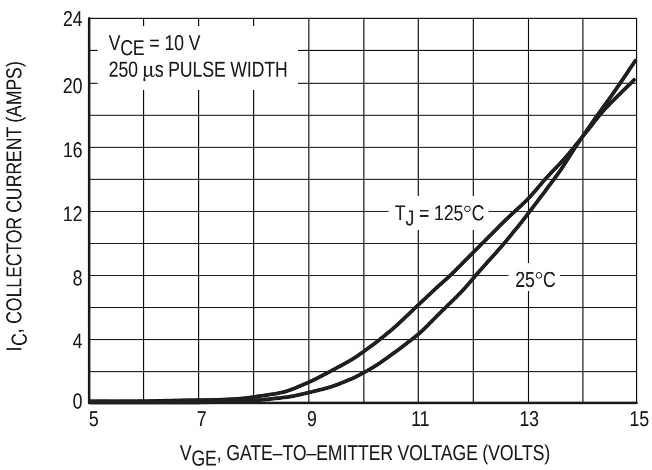


Figure 3. Transfer Characteristics

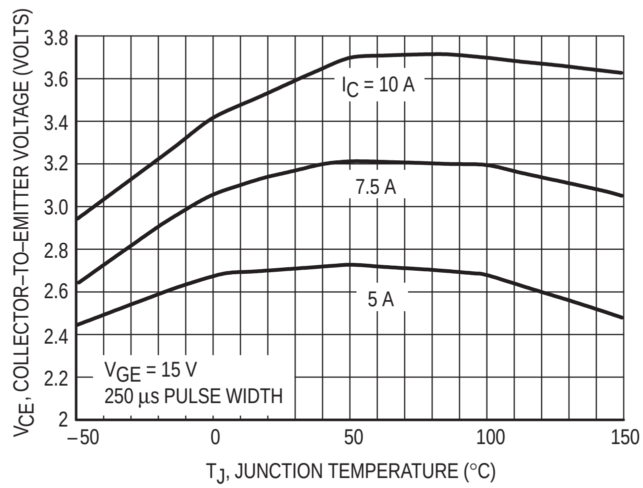


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

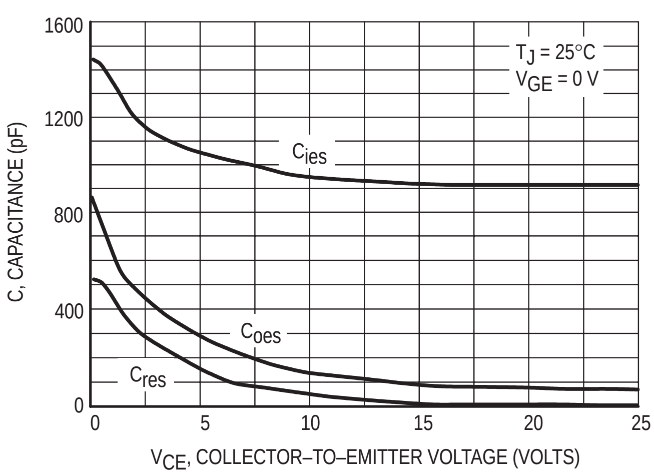


Figure 5. Capacitance Variation

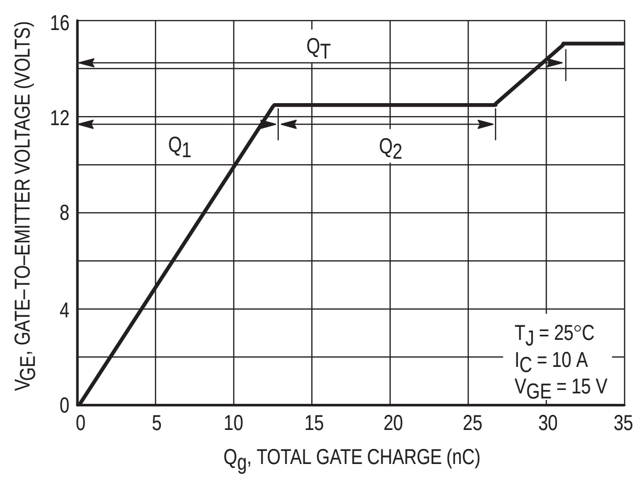


Figure 6. Gate–to–Emitter Voltage versus Total Charge

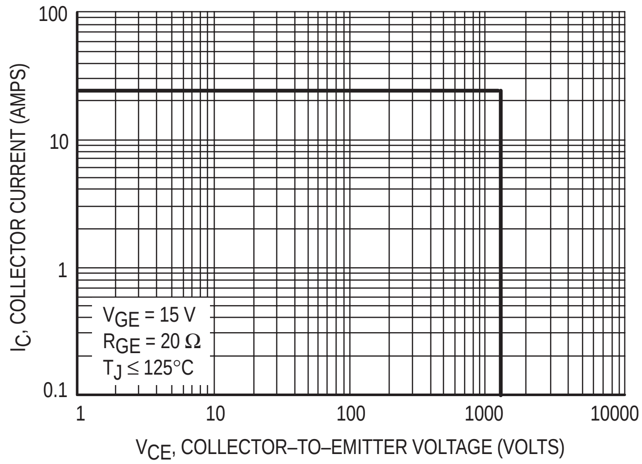


Figure 7. Reverse Biased Safe Operating Area

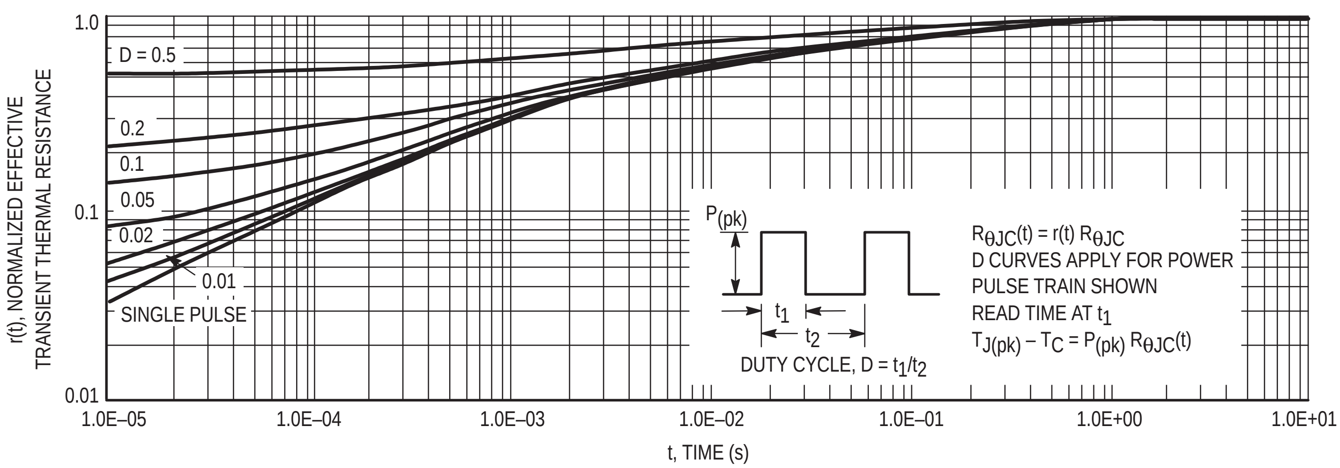


Figure 8. Thermal Response

Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N–Channel Enhancement–Mode Silicon Gate

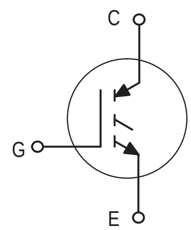
MGW20N120

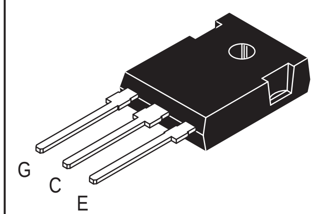
Motorola Preferred Device

IGBT IN TO–247
20 A @ 90°C
28 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 160 µJ/A typical at 125°C
- High Short Circuit Capability – 10 µs minimum
- Robust High Voltage Termination





CASE 340K–01
STYLE 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	28 20 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	174 1.39	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	µs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc) Temperature Coefficient (Positive)		$V_{(BR)CES}$	1200 —	— 870	— —	Vdc mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	25	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		I_{CES}	— —	— —	100 2500	μAdc
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 10 Adc) (V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 20 Adc)		$V_{CE(on)}$	— — —	2.42 2.36 2.90	3.54 — 4.99	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1860	—	pF
Output Capacitance		C_{oes}	—	122	—	
Transfer Capacitance		C_{res}	—	29	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	103	—	
Turn–Off Delay Time		$t_{d(off)}$	—	190	—	
Fall Time		t_f	—	284	—	
Turn–Off Switching Loss		E_{off}	—	1.65	2.75	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	83	—	ns
Rise Time		t_r	—	107	—	
Turn–Off Delay Time		$t_{d(off)}$	—	216	—	
Fall Time		t_f	—	494	—	
Turn–Off Switching Loss		E_{off}	—	3.19	—	mJ
Gate Charge	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	62	—	nC
		Q_1	—	21	—	
		Q_2	—	25	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

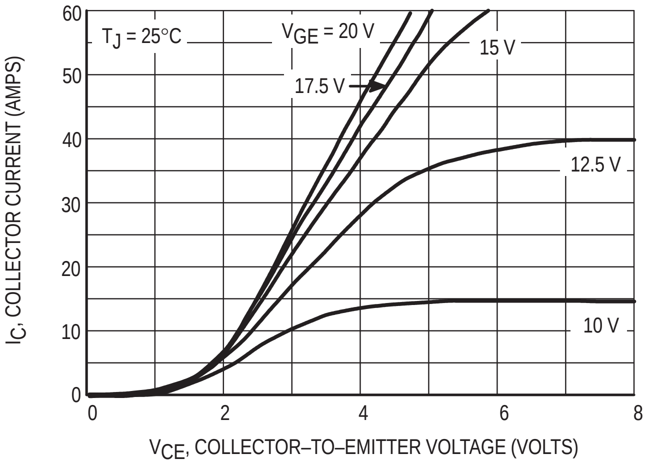


Figure 1. Output Characteristics

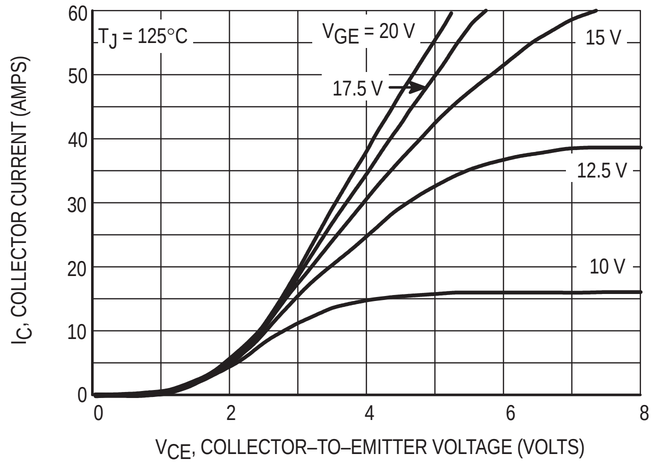


Figure 2. Output Characteristics

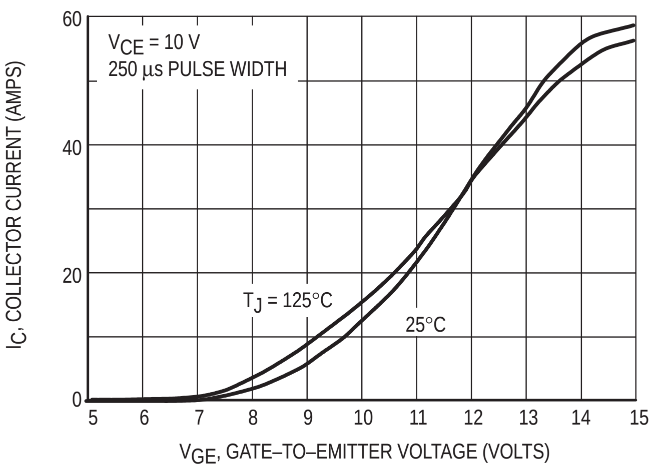


Figure 3. Transfer Characteristics

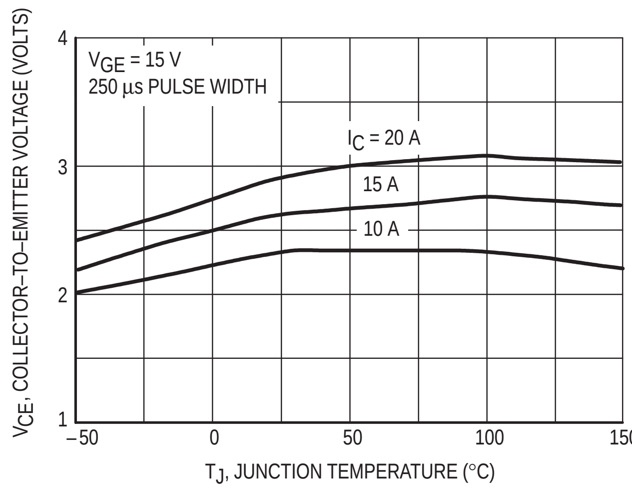


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

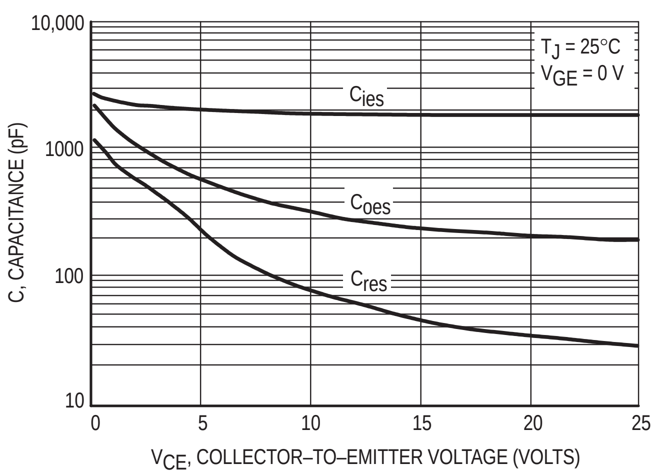


Figure 5. Capacitance Variation

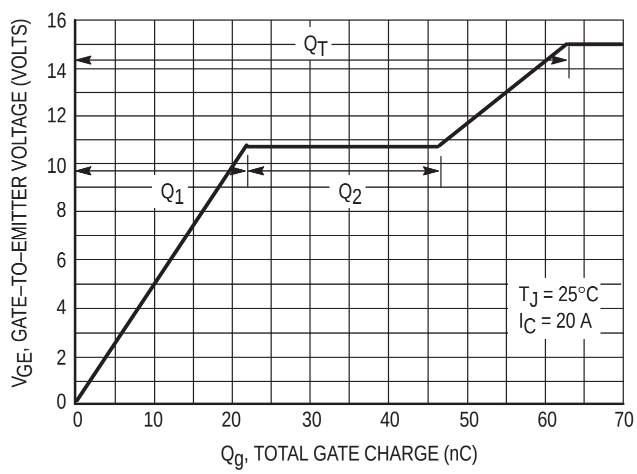


Figure 6. Gate–to–Emitter Voltage versus Total Charge

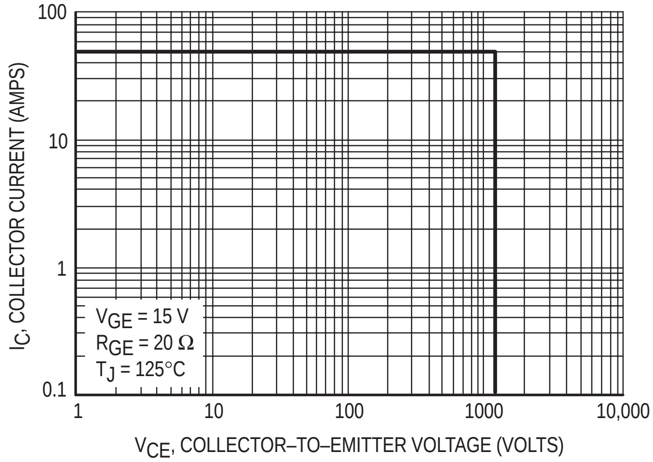


Figure 7. Reverse Biased Safe Operating Area

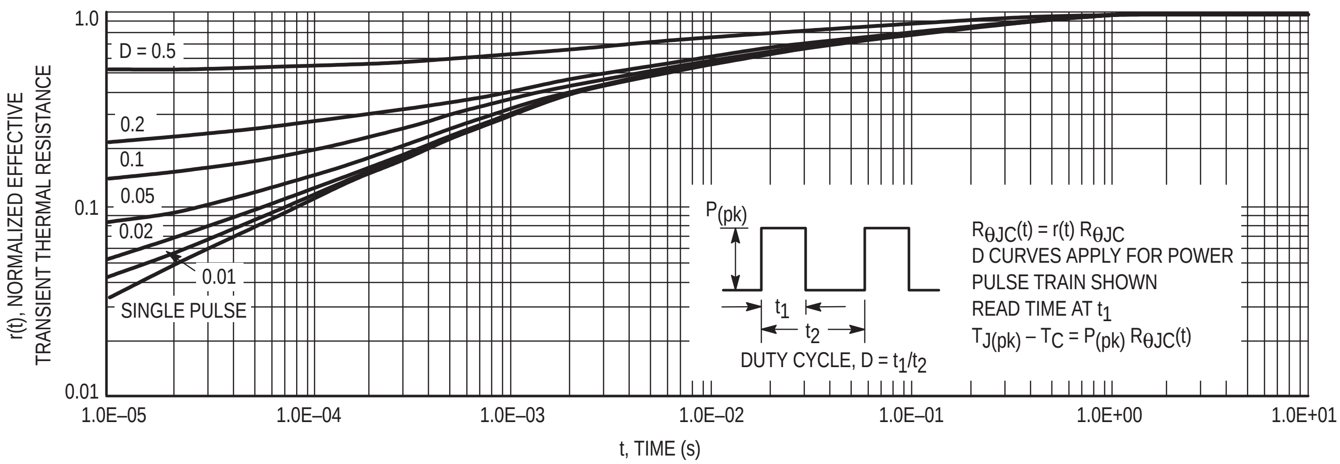


Figure 8. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

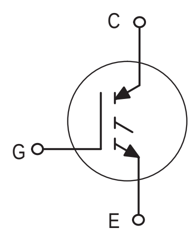
MGY25N120

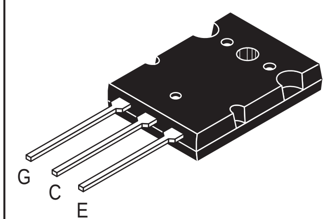
Motorola Preferred Device

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 216 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination

IGBT IN TO–264
25 A @ 90°C
38 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED





CASE 340G–02
STYLE 5
TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	38 25 76	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	212 1.69	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.6 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 µAdc) Temperature Coefficient (Positive)		$V_{(BR)CES}$	1200 —	— 960	— —	Vdc mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	25	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		I_{CES}	— —	— —	100 2500	µAdc
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 12.5 Adc) (V_{GE} = 15 Vdc, I_C = 12.5 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 25 Adc)		$V_{CE(on)}$	— — —	2.37 2.15 2.98	3.24 — 4.19	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 25 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	2795	—	pF
Output Capacitance		C_{oes}	—	181	—	
Transfer Capacitance		C_{res}	—	45	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 µH R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	91	—	ns
Rise Time		t_r	—	124	—	
Turn–Off Delay Time		$t_{d(off)}$	—	196	—	
Fall Time		t_f	—	310	—	
Turn–Off Switching Loss		E_{off}	—	2.44	4.69	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 µH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	126	—	
Turn–Off Delay Time		$t_{d(off)}$	—	236	—	
Fall Time		t_f	—	640	—	
Turn–Off Switching Loss		E_{off}	—	5.40	—	mJ
Gate Charge	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc)	Q_T	—	97	—	nC
		Q_1	—	31	—	
		Q_2	—	40	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

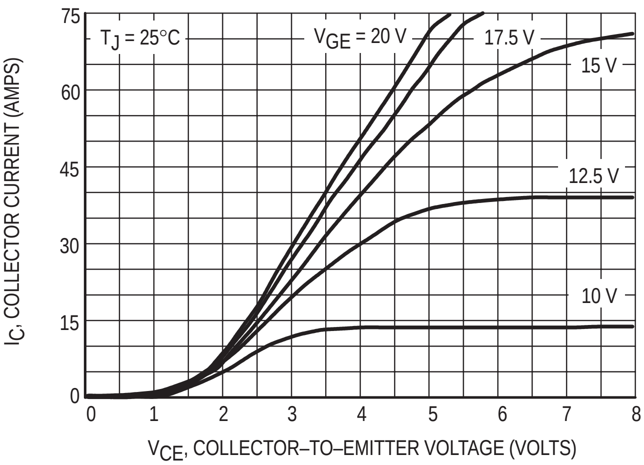


Figure 1. Output Characteristics

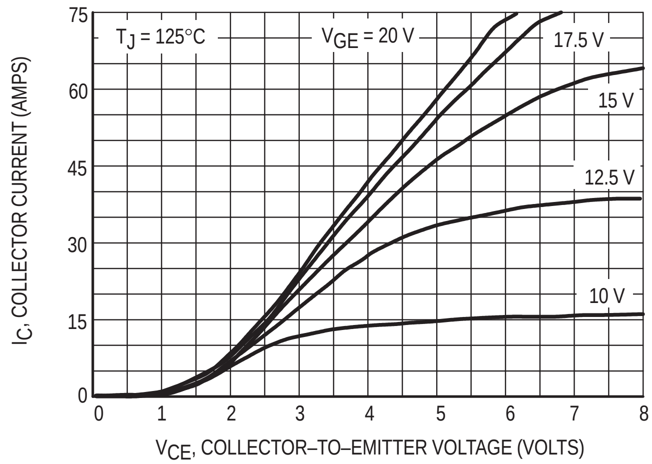


Figure 2. Output Characteristics

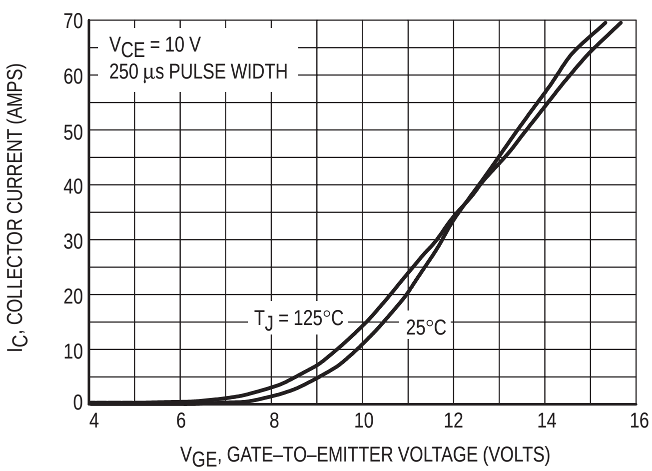


Figure 3. Transfer Characteristics

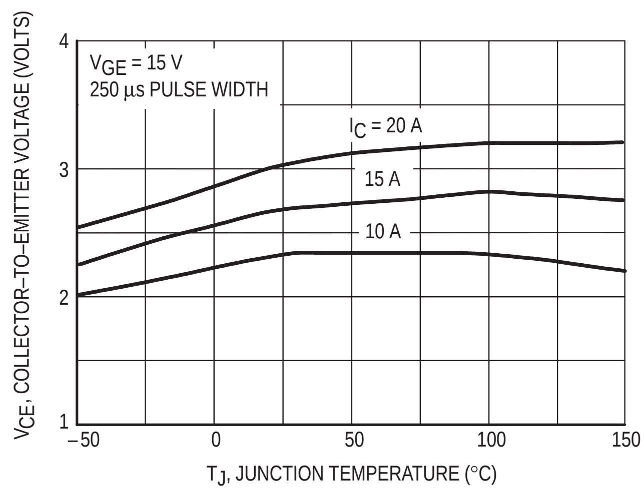


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

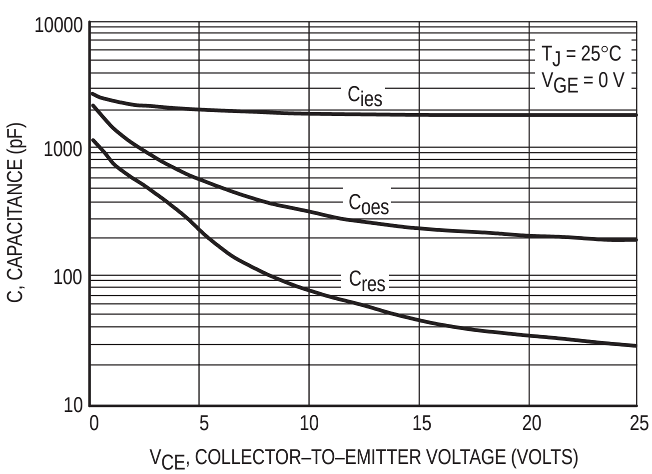


Figure 5. Capacitance Variation

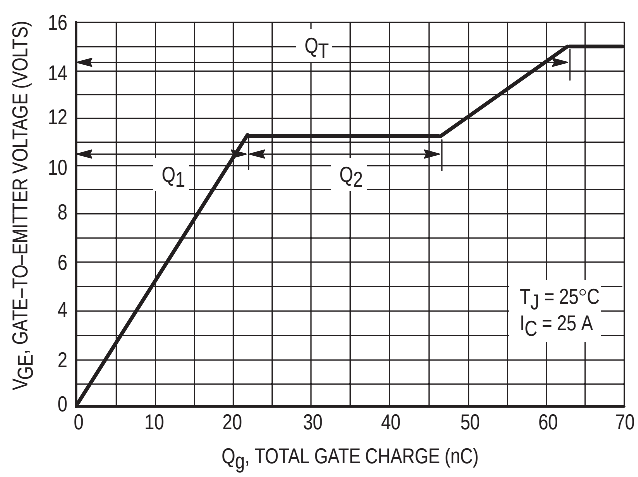


Figure 6. Gate–to–Emitter Voltage versus Total Charge

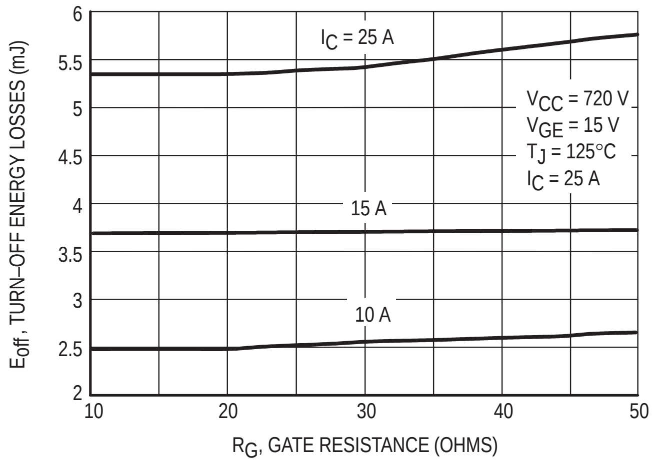


Figure 7. Turn–Off Losses versus Gate Resistance

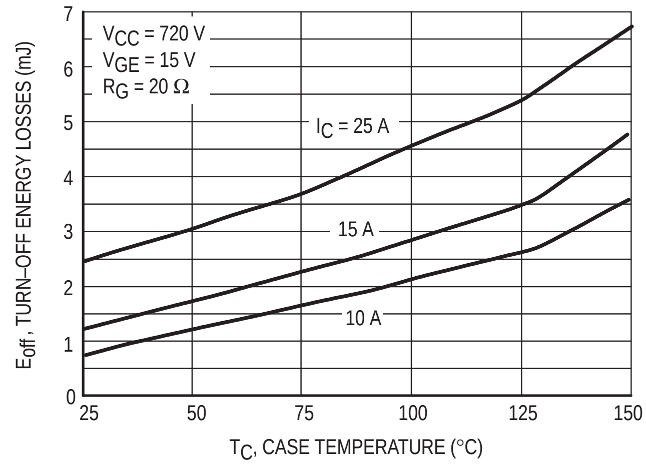


Figure 8. Turn–Off Losses versus Case Temperature

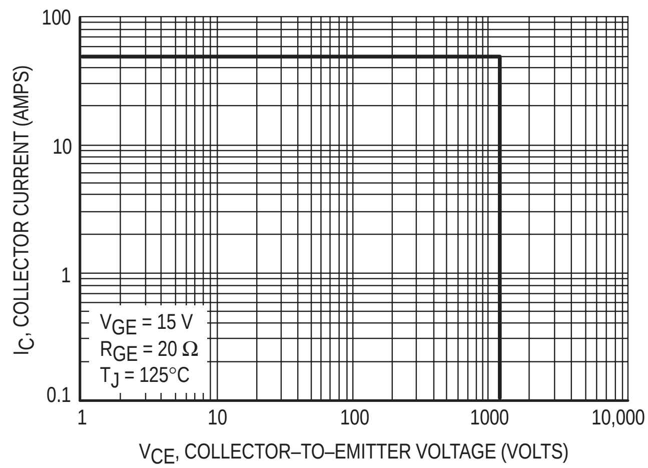


Figure 9. Reverse Biased Safe Operating Area

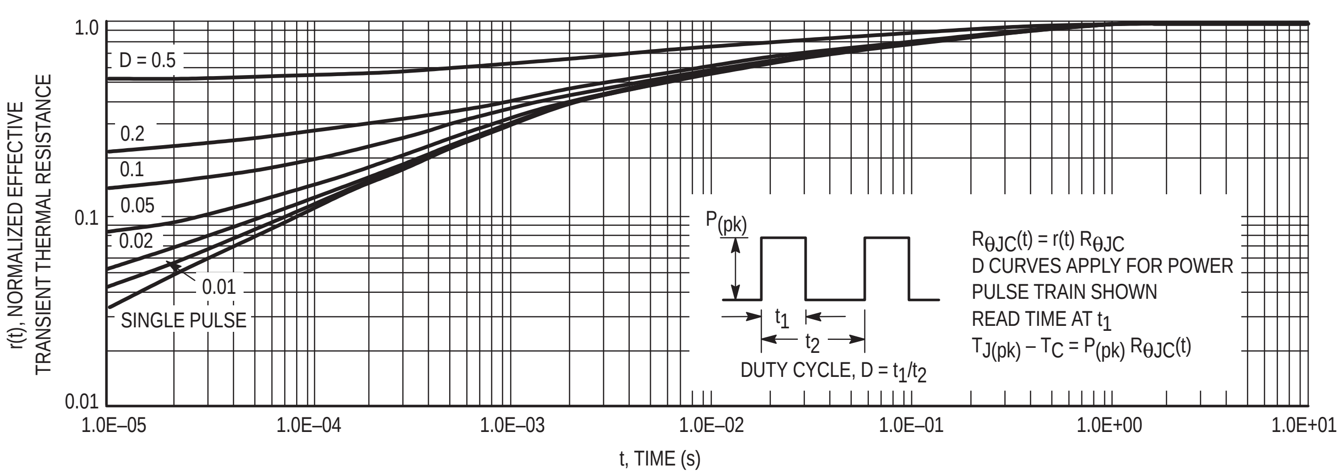


Figure 10. Thermal Response

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Preliminary Information

Insulated Gate Bipolar Transistor

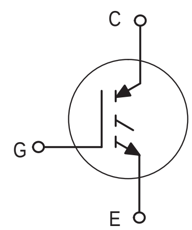
N–Channel Enhancement–Mode Silicon Gate

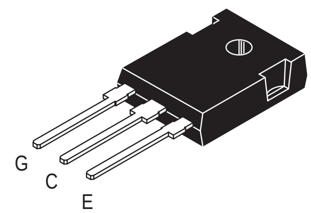
MGW12N120E

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. The new generation provides lower On–voltage without sacrificing switching performance. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed: E_{off} = 167 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 720 V
- Low On–Voltage — 2.6 V typical at 10 A, 125°C
- Robust High Voltage Termination

IGBT IN TO–247
12 A @ 90°C
20 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED
LOW ON–VOLTAGE





CASE 340K–01
STYLE 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	20 12 24	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	123 0.98	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 µAdc)		$V_{(BR)CES}$	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	25	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	µAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	300	
Gate–Body Leakage Current (V_{GE} = ±20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc)		$V_{CE(on)}$	—	2.0	3.0	Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)			—	2.1	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	2.6	3.5	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)		g_{fe}	—	5.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1033	—	pF
Output Capacitance		C_{oes}	—	131	—	
Transfer Capacitance		C_{res}	—	64	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 µH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	39	—	ns
Rise Time		t_r	—	36	—	
Turn–Off Delay Time		$t_{d(off)}$	—	129	—	
Fall Time		t_f	—	400	—	
Turn–Off Switching Loss		E_{off}	—	0.96	1.5	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 µH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	155	—	ns
Rise Time		t_r	—	36	—	
Turn–Off Delay Time		$t_{d(off)}$	—	164	—	
Fall Time		t_f	—	625	—	
Turn–Off Switching Loss		E_{off}	—	1.67	—	mJ
Gate Charge	(V_{CC} = 600 V, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	62	—	nC
		Q_1	—	15.6	—	
		Q_2	—	37	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

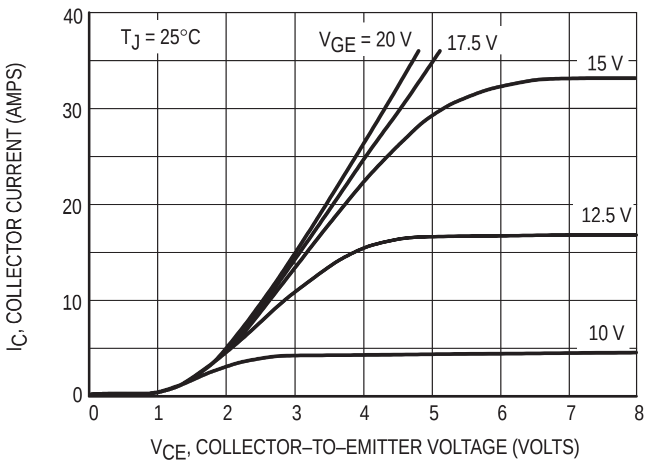


Figure 1. Output Characteristics

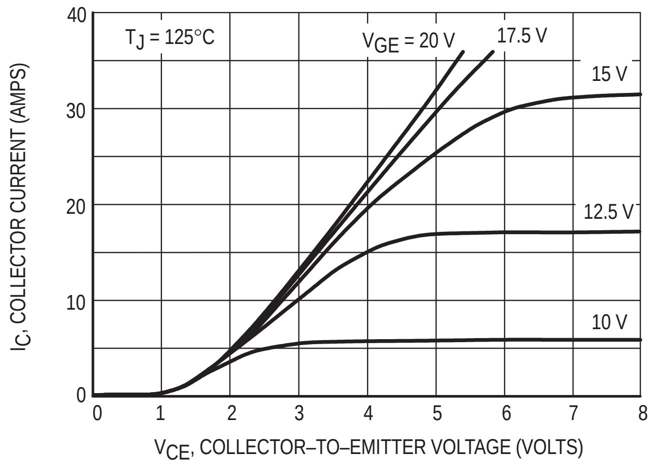


Figure 2. Output Characteristics

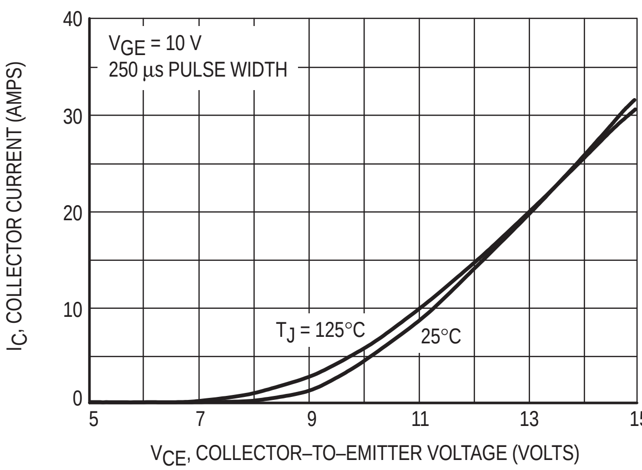


Figure 3. Transfer Characteristics

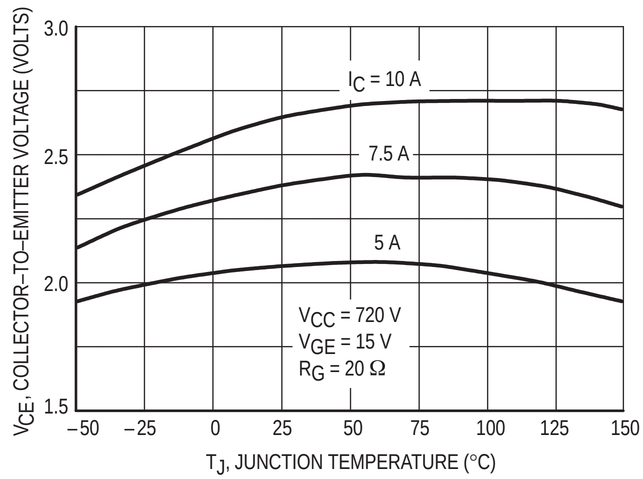


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

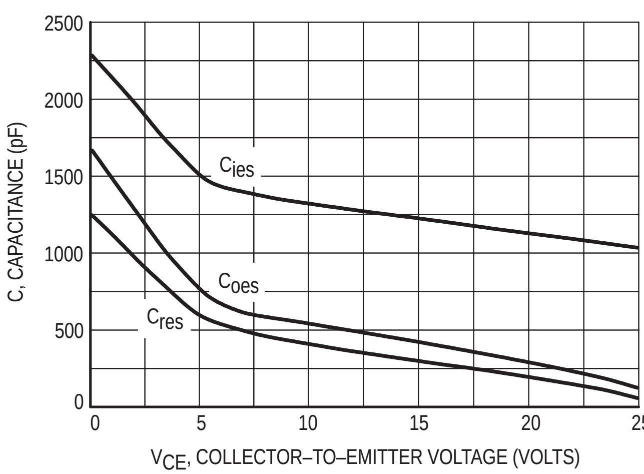


Figure 5. Capacitance Variation

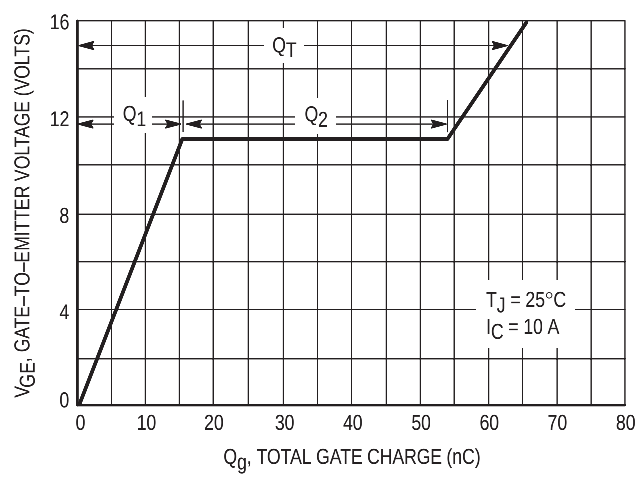


Figure 6. Gate–to–Emitter Voltage versus Total Charge

TYPICAL ELECTRICAL CHARACTERISTICS

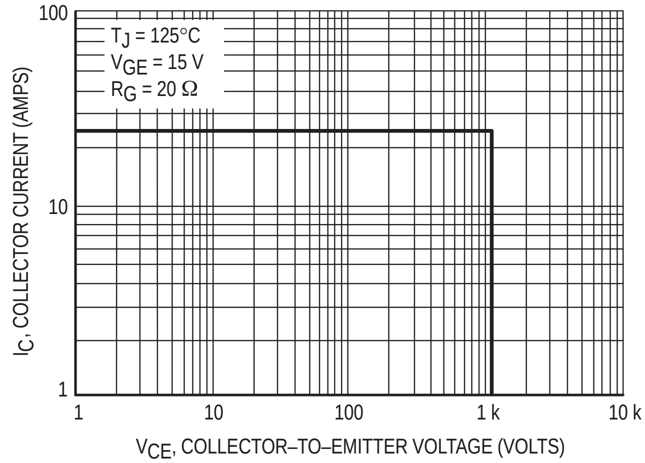


Figure 7. Forward Characteristics versus Current

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

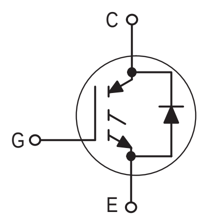
MGW12N120D

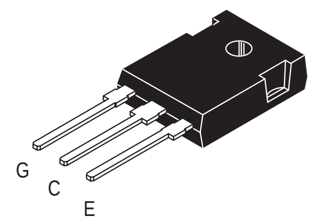
Motorola Preferred Device

IGBT & DIODE IN TO–247
12 A @ 90°C
20 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 150 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340K–01
STYLE 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	20 12 40	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.98	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.0 1.4 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc)		$V_{CE(on)}$	—	2.71	3.37	Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)			—	3.78	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	3.5	4.42	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1003	—	pF
Output Capacitance		C_{oes}	—	126	—	
Transfer Capacitance		C_{res}	—	106	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	74	—	ns
Rise Time		t_r	—	83	—	
Turn–Off Delay Time		$t_{d(off)}$	—	76	—	
Fall Time		t_f	—	231	—	
Turn–Off Switching Loss		E_{off}	—	0.55	1.33	mJ
Turn–On Switching Loss		E_{on}	—	1.21	1.88	
Total Switching Loss		E_{ts}	—	1.76	3.21	
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	66	—	ns
Rise Time		t_r	—	87	—	
Turn–Off Delay Time		$t_{d(off)}$	—	120	—	
Fall Time		t_f	—	575	—	
Turn–Off Switching Loss		E_{off}	—	1.49	—	mJ
Turn–On Switching Loss		E_{on}	—	2.37	—	
Total Switching Loss		E_{ts}	—	3.86	—	
Gate Charge	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	29	—	nC
		Q_1	—	13	—	
		Q_2	—	12	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 5.0 Adc)		V_{FEC}	—	2.26	3.32	Vdc
(I_{EC} = 5.0 Adc, T_J = 125°C)			—	1.37	—	
(I_{EC} = 10 Adc)			—	2.86	4.18	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 10 Adc, V_R = 720 Vdc, dI_F/dt = 100 A/μs)	t_{rr}	—	116	—	ns
		t_a	—	69	—	
		t_b	—	47	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.36	—	μC
Reverse Recovery Time	(I_F = 10 Adc, V_R = 720 Vdc, dI_F/dt = 100 A/μs, T_J = 125°C)	t_{rr}	—	234	—	ns
		t_a	—	149	—	
		t_b	—	85	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.40	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

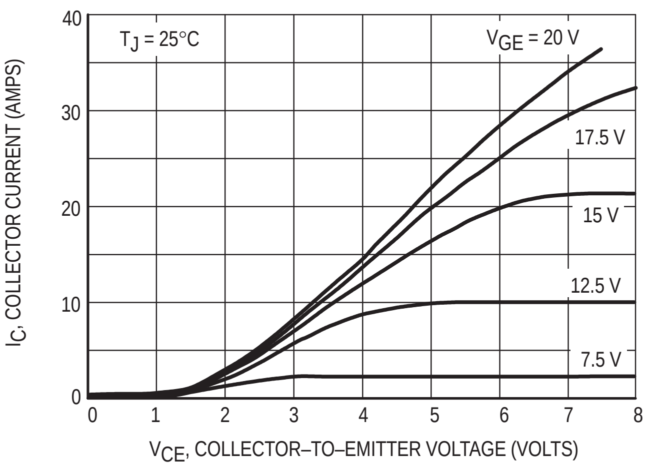


Figure 1. Output Characteristics

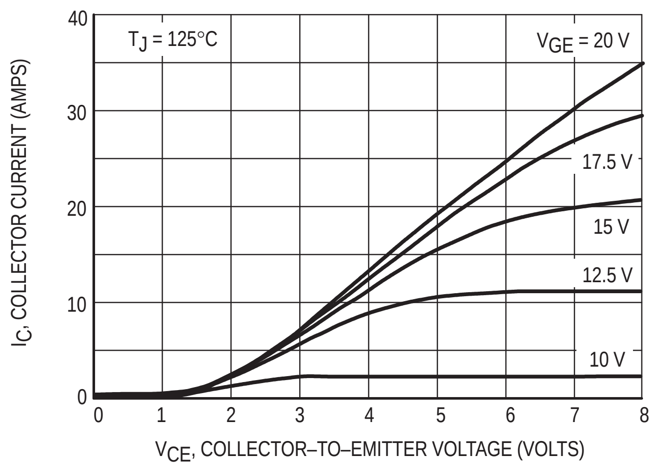


Figure 2. Output Characteristics

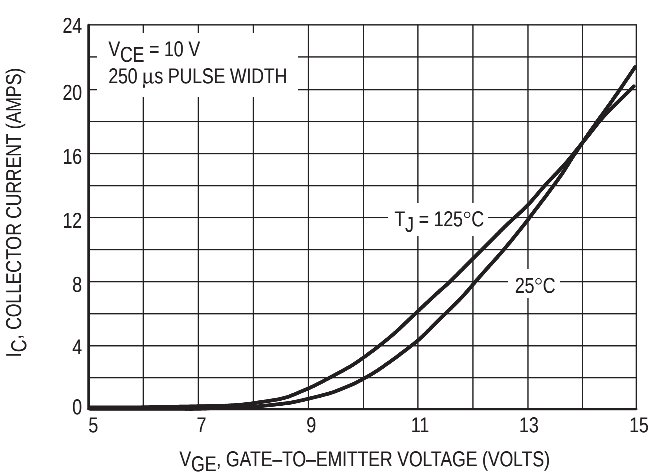


Figure 3. Transfer Characteristics

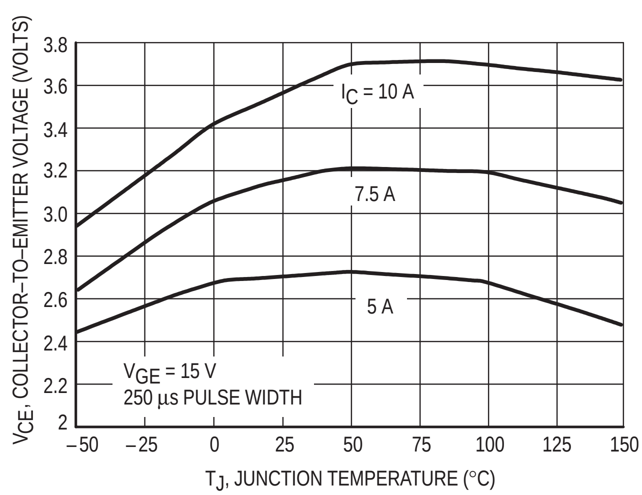


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

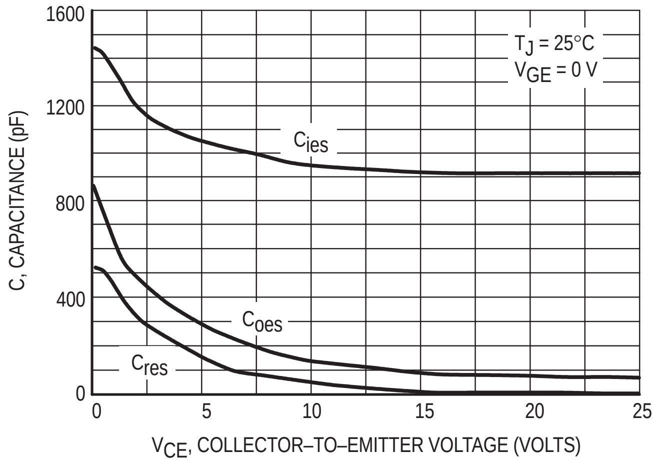


Figure 5. Capacitance Variation

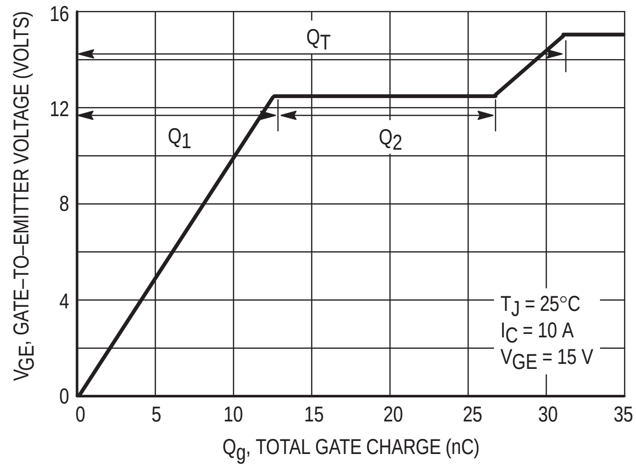


Figure 6. Gate–to–Emitter Voltage versus Total Charge

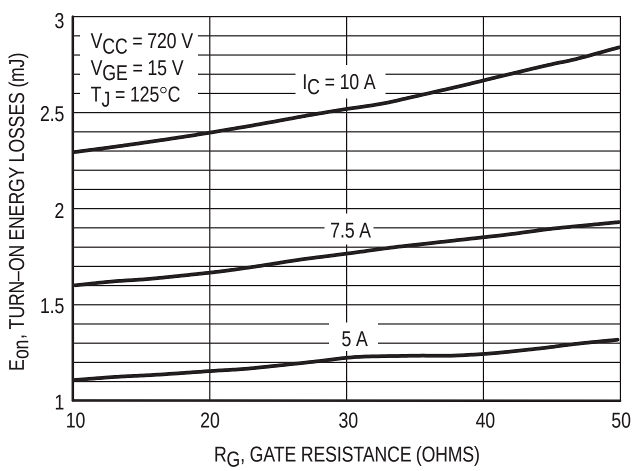


Figure 7. Turn–On Losses versus Gate Resistance

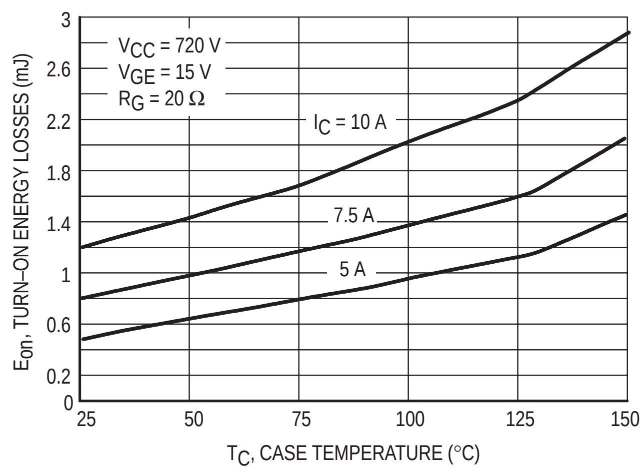


Figure 8. Turn–On Losses versus Case Temperature

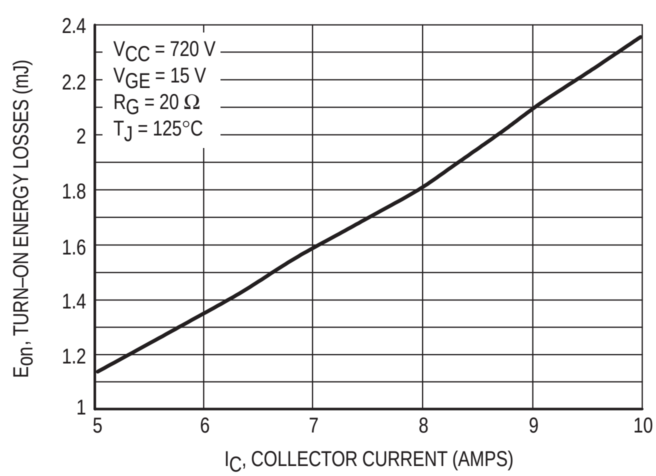


Figure 9. Turn–On Losses versus Collector Current

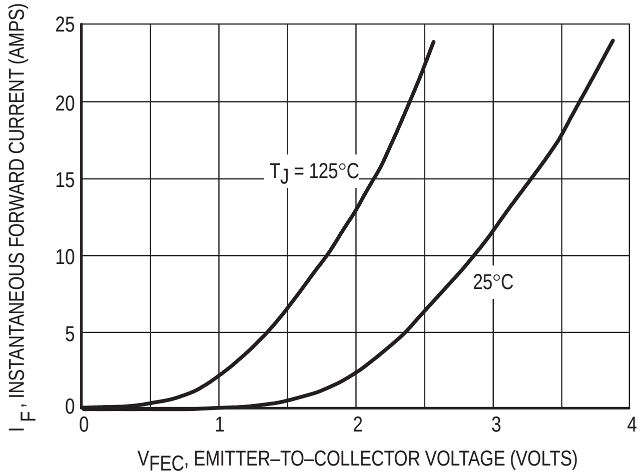


Figure 10. Diode Forward Voltage Drop

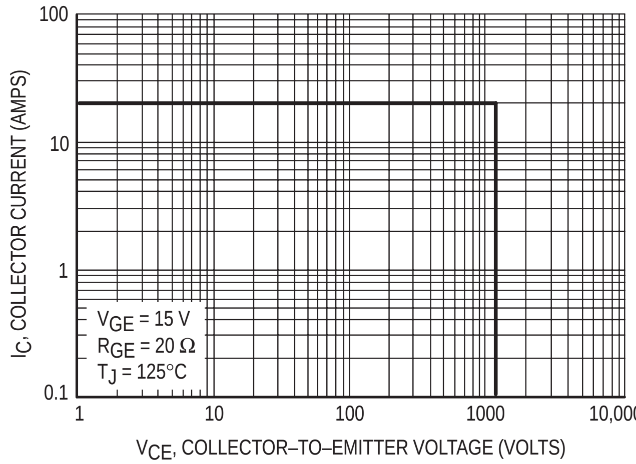


Figure 11. Reverse Biased Safe Operating Area

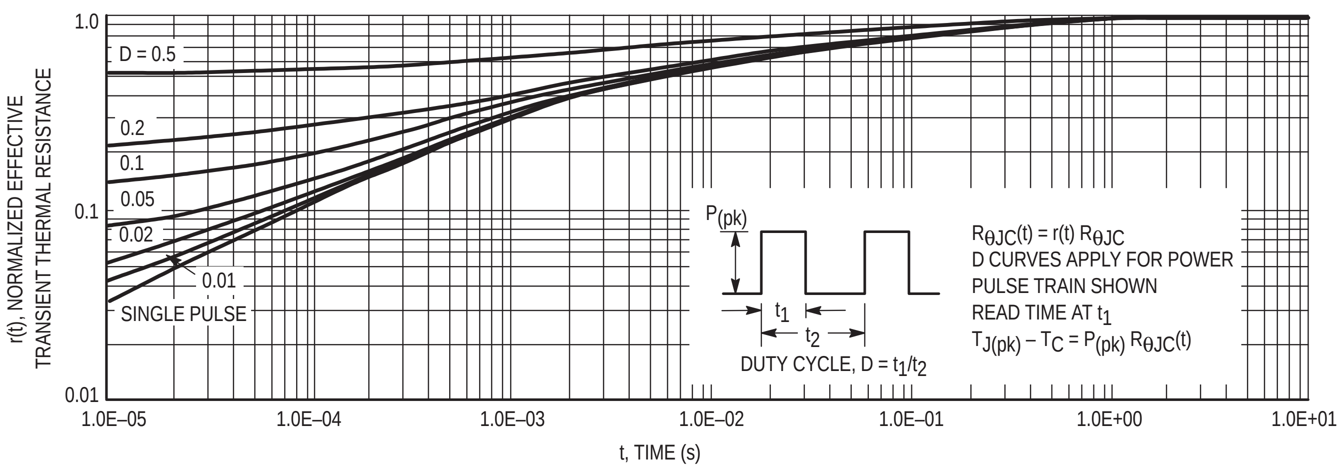


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

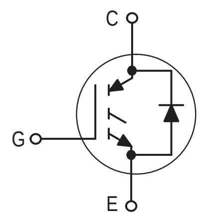
MGY20N120D

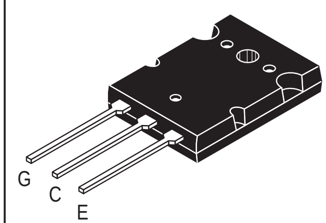
Motorola Preferred Device

IGBT & DIODE IN TO–264
20 A @ 90°C
28 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 160 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02
STYLE 5
TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	28 20 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	174 1.39	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.7 1.1 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 10 Adc)		$V_{CE(on)}$	—	2.42	3.54	Vdc
(V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C)			—	2.36	—	
(V_{GE} = 15 Vdc, I_C = 20 Adc)			—	2.90	4.99	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1876	—	pF
Output Capacitance		C_{oes}	—	208	—	
Transfer Capacitance		C_{res}	—	31	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	103	—	
Turn–Off Delay Time		$t_{d(off)}$	—	190	—	
Fall Time		t_f	—	284	—	
Turn–Off Switching Loss		E_{off}	—	1.65	2.75	mJ
Turn–On Switching Loss		E_{on}	—	2.42	3.75	
Total Switching Loss		E_{ts}	—	4.07	6.50	
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	83	—	ns
Rise Time		t_r	—	107	—	
Turn–Off Delay Time		$t_{d(off)}$	—	216	—	
Fall Time		t_f	—	494	—	
Turn–Off Switching Loss		E_{off}	—	3.19	—	mJ
Turn–On Switching Loss		E_{on}	—	4.26	—	
Total Switching Loss		E_{ts}	—	7.45	—	
Gate Charge	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	63	—	nC
		Q_1	—	20	—	
		Q_2	—	27	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 10 Adc)		V_{FEC}	—	2.92	3.59	Vdc
(I_{EC} = 10 Adc, T_J = 125°C)			—	1.73	—	
(I_{EC} = 20 Adc)			—	3.67	4.57	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 20 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/µs)	t_{rr}	—	114	—	ns
		t_a	—	74	—	
		t_b	—	40	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.68	—	µC
Reverse Recovery Time	(I_F = 20 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/µs, T_J = 125°C)	t_{rr}	—	224	—	ns
		t_a	—	149	—	
		t_b	—	75	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.40	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

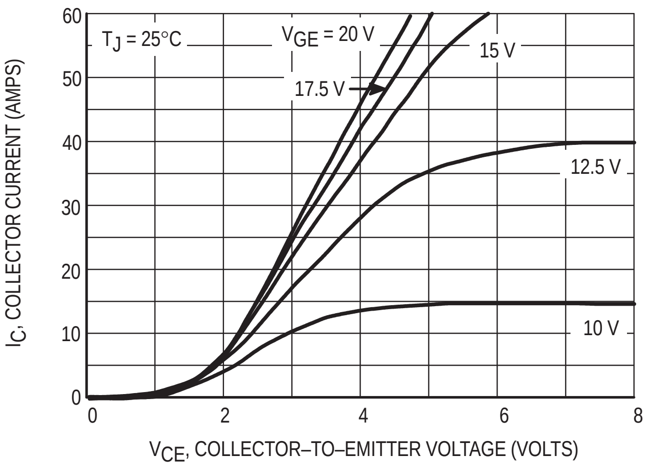


Figure 1. Output Characteristics

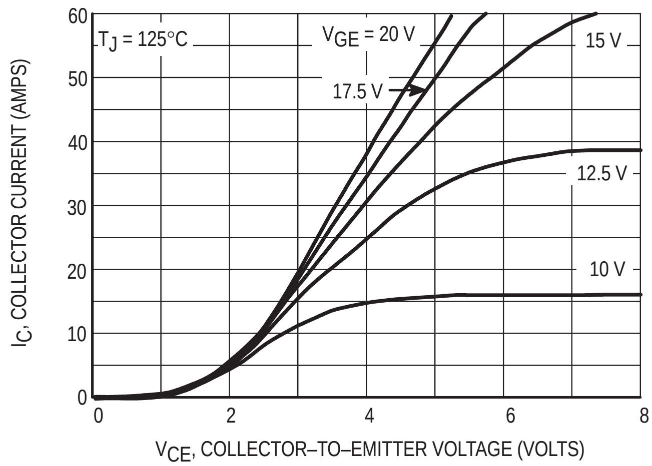


Figure 2. Output Characteristics

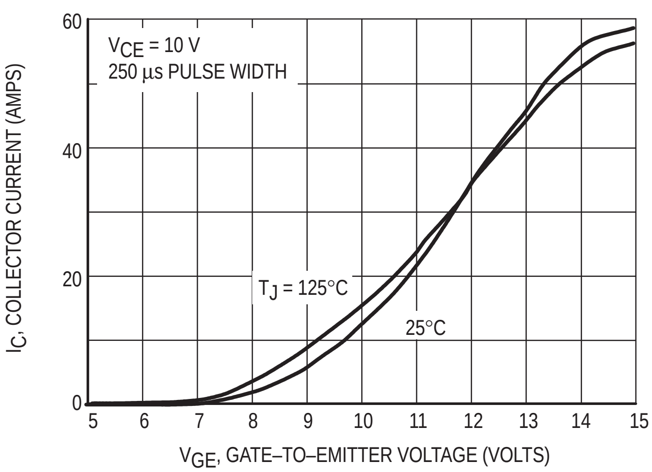


Figure 3. Transfer Characteristics

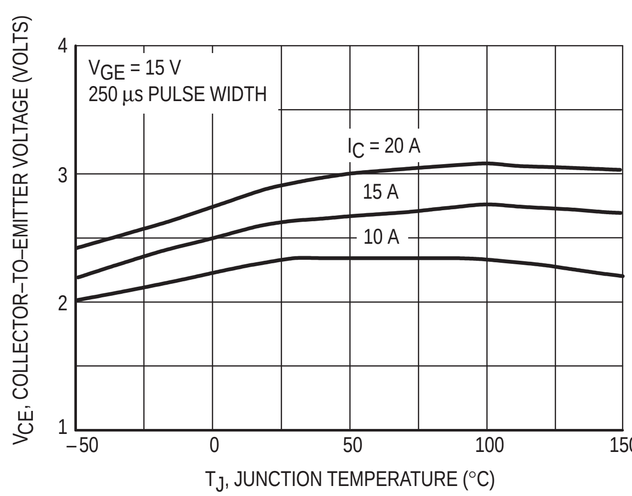


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

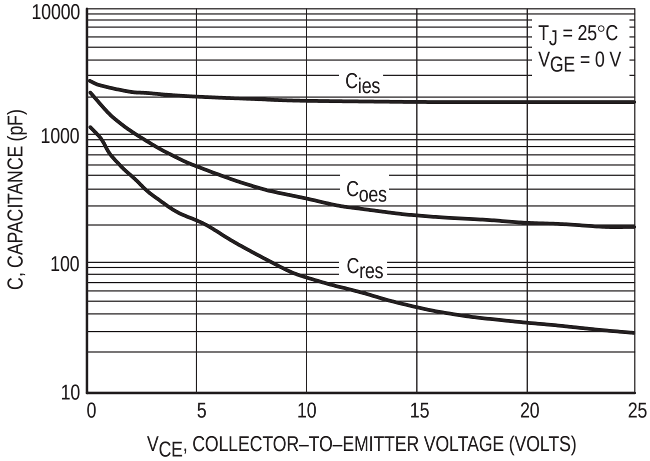


Figure 5. Capacitance Variation

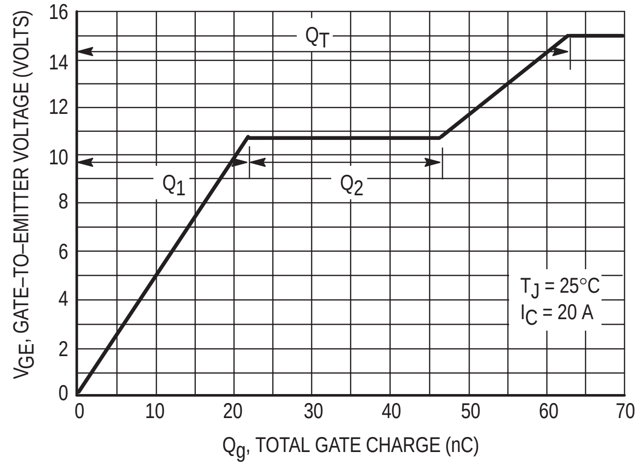


Figure 6. Gate–to–Emitter Voltage versus Total Charge

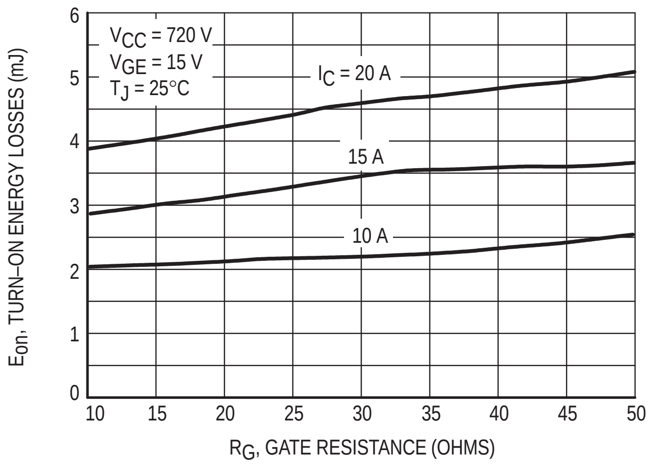


Figure 7. Turn–On Losses versus Gate Resistance

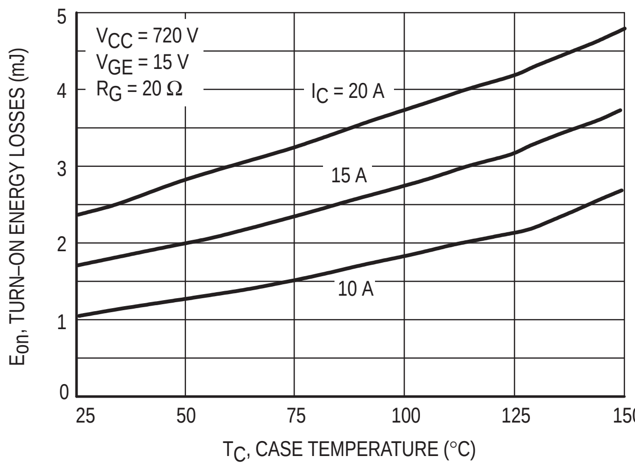


Figure 8. Turn–On Losses versus Case Temperature

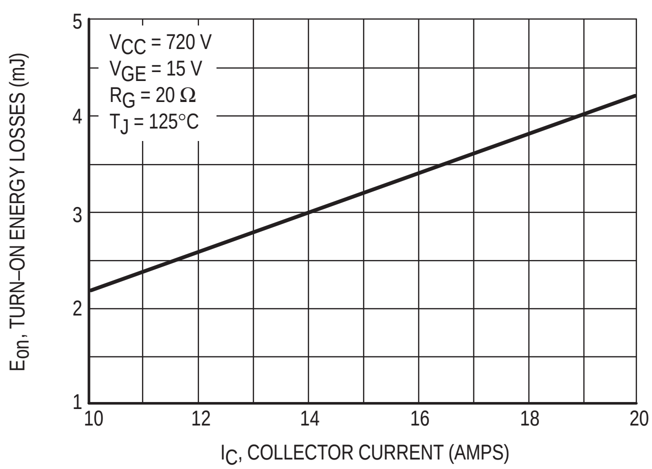


Figure 9. Turn–On Losses versus Collector Current

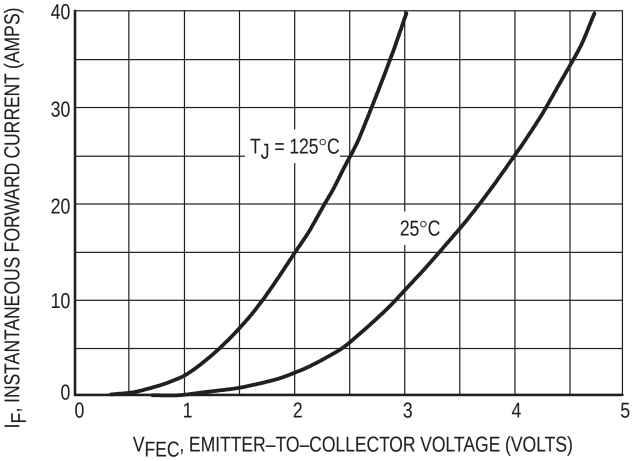


Figure 10. Diode Forward Voltage Drop

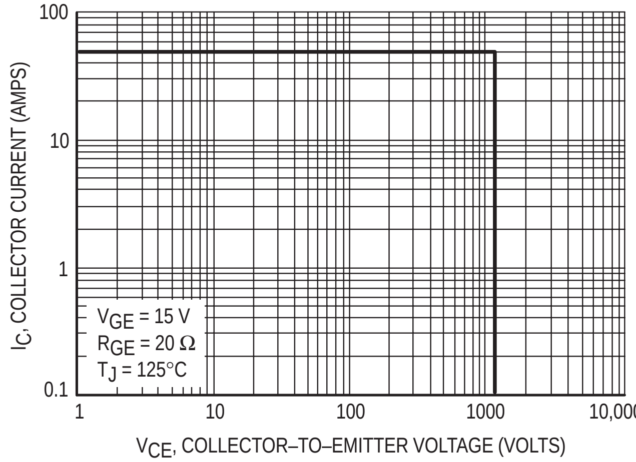


Figure 11. Reverse Biased Safe Operating Area

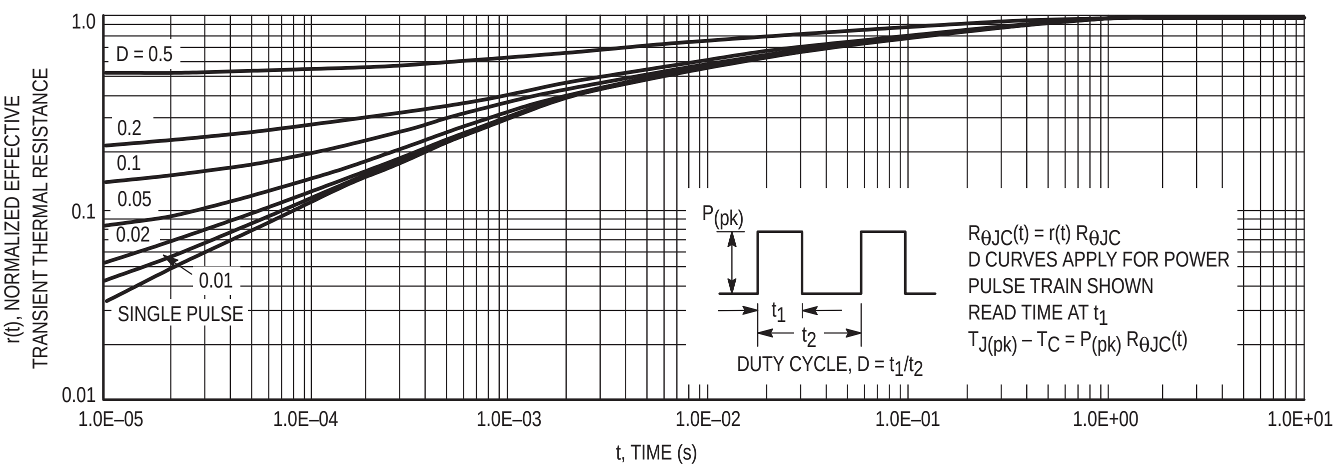


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

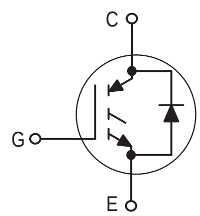
MGY25N120D

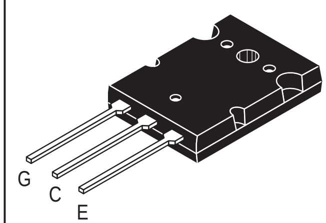
Motorola Preferred Device

IGBT & DIODE IN TO–264
25 A @ 90°C
38 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 216 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02
STYLE 5
TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	38 25 76	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	212 1.69	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.6 0.9 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	960	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 12.5 Adc)		$V_{CE(on)}$	—	2.37	3.24	Vdc
(V_{GE} = 15 Vdc, I_C = 12.5 Adc, T_J = 125°C)			—	2.15	—	
(V_{GE} = 15 Vdc, I_C = 25 Adc)			—	2.98	4.19	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1859	—	pF
Output Capacitance		C_{oes}	—	198	—	
Transfer Capacitance		C_{res}	—	30	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	91	—	ns
Rise Time		t_r	—	124	—	
Turn–Off Delay Time		$t_{d(off)}$	—	196	—	
Fall Time		t_f	—	310	—	
Turn–Off Switching Loss		E_{off}	—	2.44	4.69	mJ
Turn–On Switching Loss		E_{on}	—	3.14	5.22	
Total Switching Loss		E_{ts}	—	5.58	9.91	
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	126	—	
Turn–Off Delay Time		$t_{d(off)}$	—	236	—	
Fall Time		t_f	—	640	—	
Turn–Off Switching Loss		E_{off}	—	5.40	—	mJ
Turn–On Switching Loss		E_{on}	—	5.03	—	
Total Switching Loss		E_{ts}	—	10.43	—	
Gate Charge	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc)	Q_T	—	62	—	nC
		Q_1	—	22	—	
		Q_2	—	25	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 12.5 Adc)		V_{FEC}	—	2.89	3.50	Vdc
(I_{EC} = 12.5 Adc, T_J = 125°C)			—	1.75	—	
(I_{EC} = 25 Adc)			—	3.65	4.45	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 25 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/µs)	t_{rr}	—	114	—	ns
		t_a	—	71	—	
		t_b	—	43	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.65	—	µC
Reverse Recovery Time	(I_F = 25 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/µs, T_J = 125°C)	t_{rr}	—	226	—	ns
		t_a	—	165	—	
		t_b	—	61	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.90	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

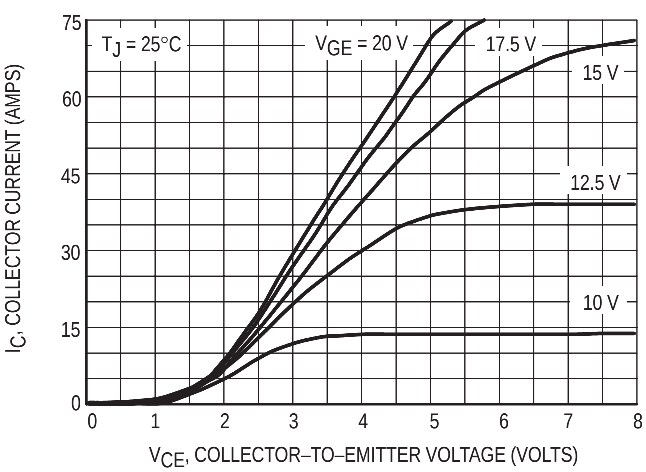


Figure 1. Output Characteristics

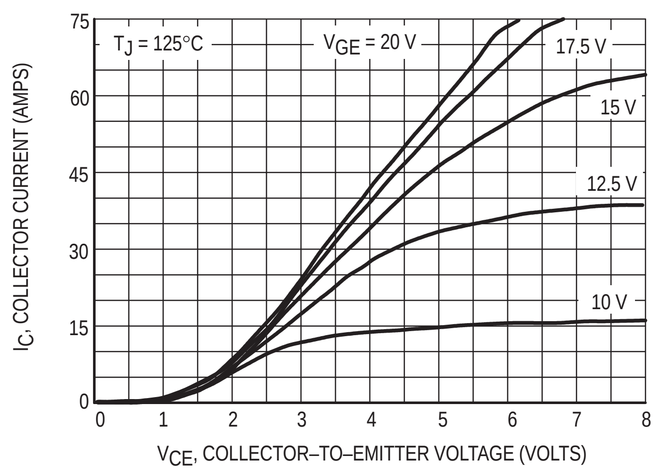


Figure 2. Output Characteristics

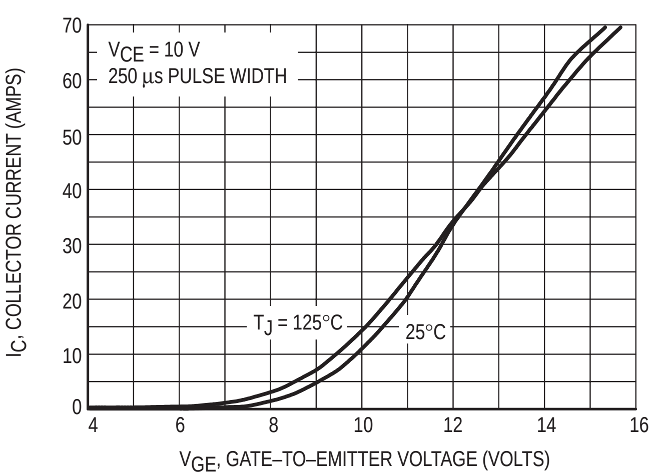


Figure 3. Transfer Characteristics

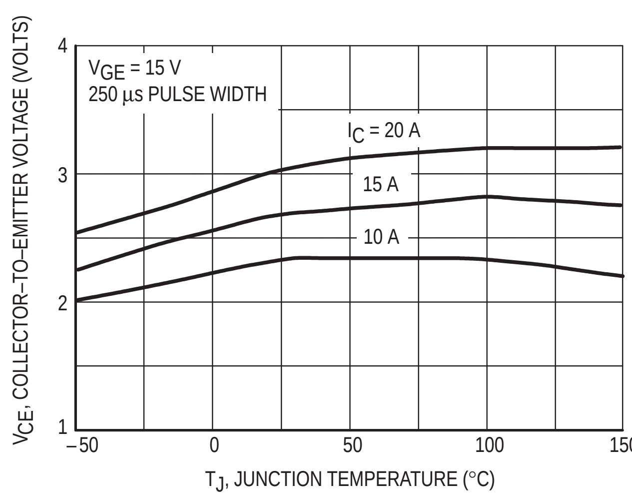


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

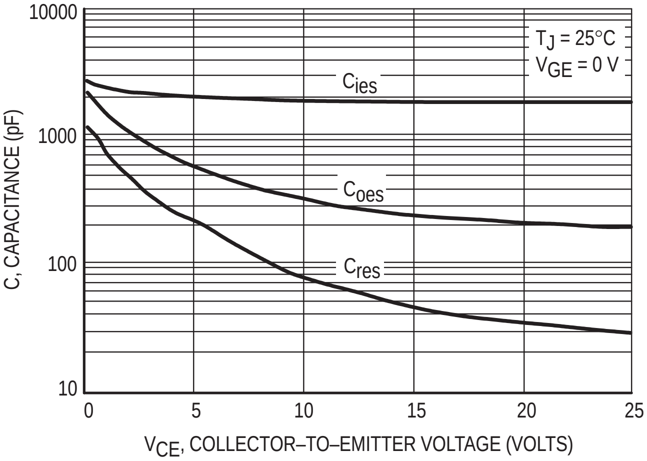


Figure 5. Capacitance Variation

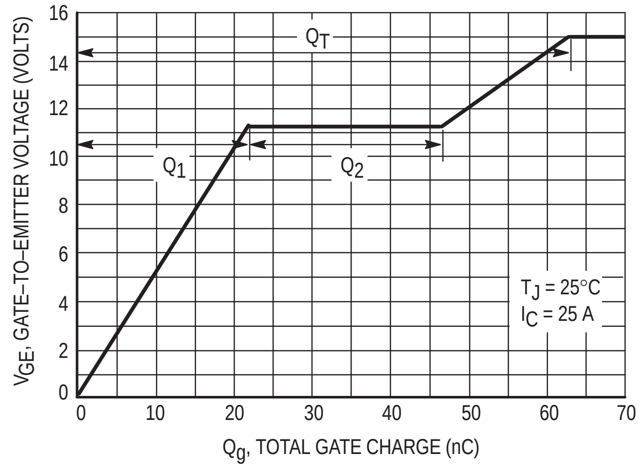


Figure 6. Gate–to–Emitter Voltage versus Total Charge

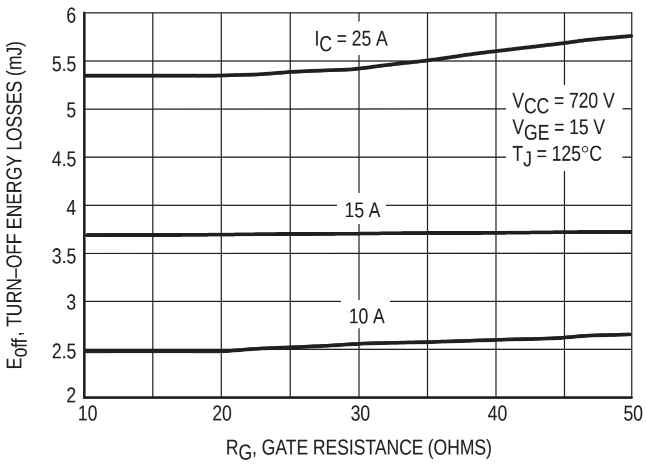


Figure 7. Turn–Off Losses versus Gate Resistance

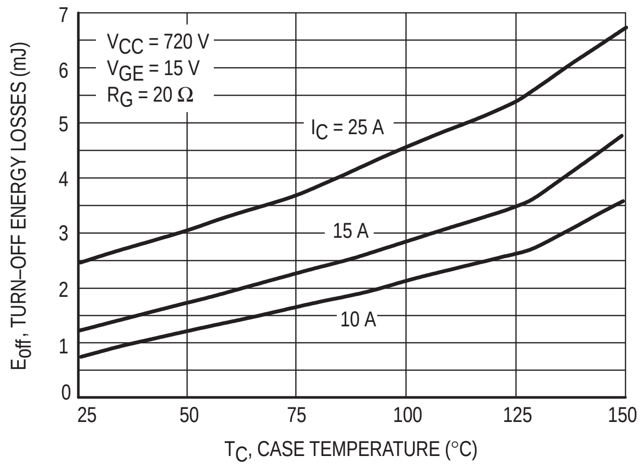


Figure 8. Turn–Off Losses versus Case Temperature

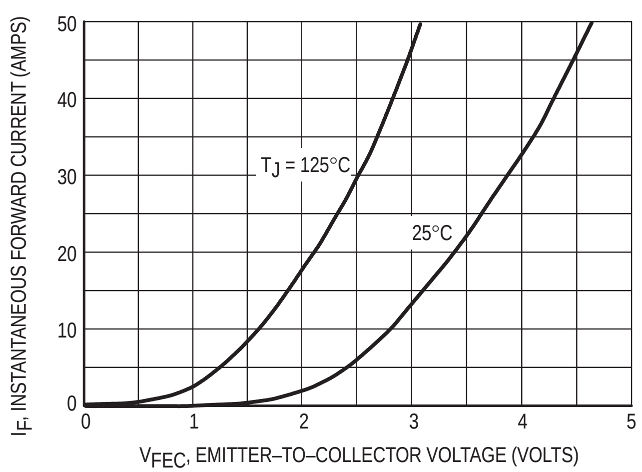


Figure 9. Diode Forward Voltage Drop

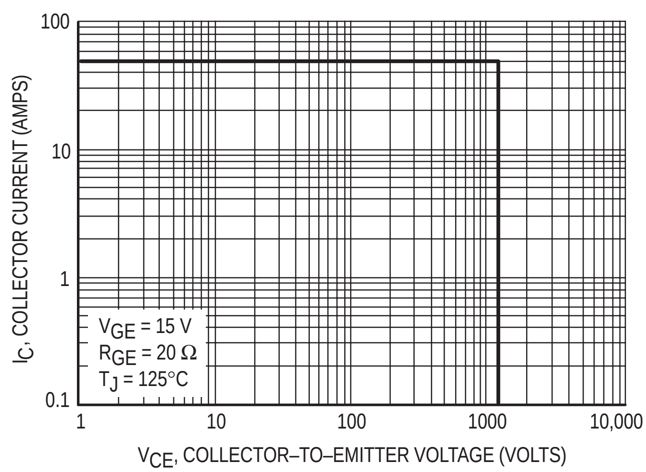


Figure 10. Reverse Biased Safe Operating Area

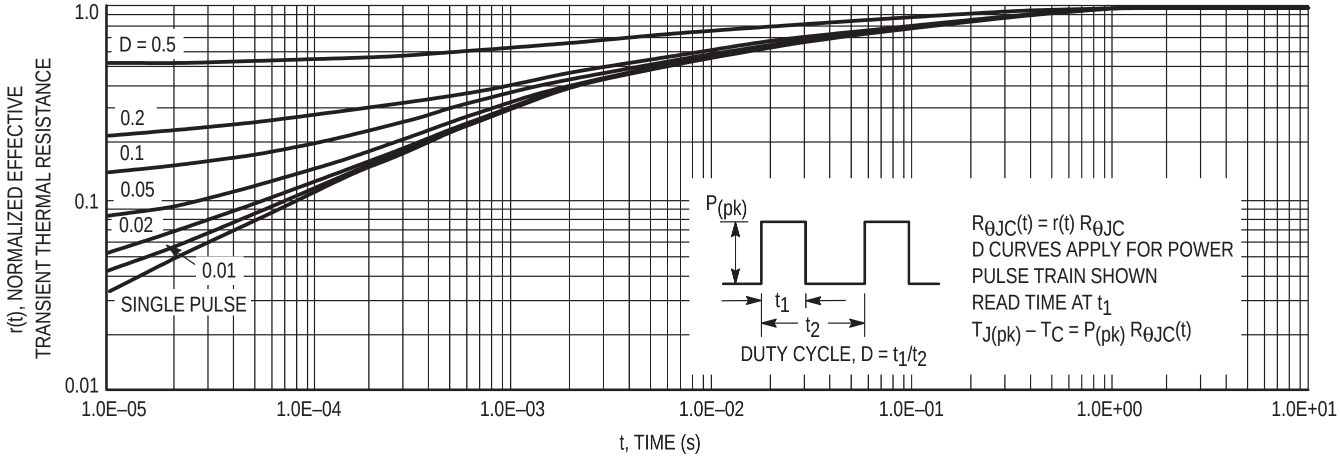


Figure 11. Thermal Response

Product Preview

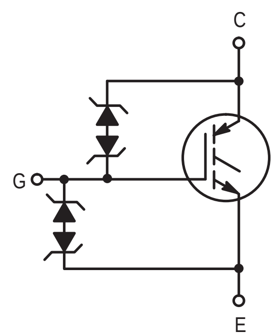
Internally Clamped N-Channel IGBT

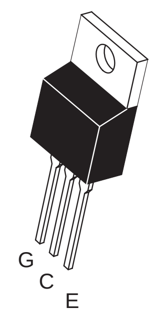
MGP15N38CL

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate Collector Over–Voltage Protection from monolithic circuitry for usage as an Ignition Coil Driver.

- Temperature Compensated Gate – Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability

15 AMPERES
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.8 V
380 VOLTS
CLAMPED





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CER}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Power Dissipation Derate above 25°C	P_D	136 0.91	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 14.2 A, L = 3.0 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 10 A, L = 3.0 mH, Starting T_J = 150°C	E_{AS}	 300 150	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Case — Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Clamp Voltage (I_C = 1.0 mA, T_J = –40°C to 175°C)		$V_{(BR)CES}$	350	380	410	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 300 V, V_{GE} = 0 V) (V_{CE} = 300 V, V_{GE} = 0 V, T_J = 150°C)		I_{CES}	— —	— —	10 150	μAdc
Gate–Emitter Clamp Voltage (I_G = 5.0 mA)		$V_{(BR)GES}$	17	—	22	Vdc
Gate–Emitter Leakage Current (V_{GE} = 10 V)		I_{GES}	—	—	10	μAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{GE} = V_{CE}, I_C = 1.0 mA) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	1.3 —	1.8 4.4	2.1 —	Vdc mV/°C
Collector–to–Emitter On–Voltage (V_{GE} = 3.5 V, I_C = 6.0 A) (V_{GE} = 4.0 V, I_C = 10 A, T_J = 150°C)		$V_{CE(on)}$	— —	— —	2.0 1.8	Volts
Forward Transconductance (V_{CE} = 5.0 V, I_C = 10 A)		g_{fe}	8.0	19	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CC} = 15 V, V_{GE} = 0 V, f = 1.0 MHz)	C_{ies}	—	TBD	—	pF
Output Capacitance		C_{oes}	—	TBD	—	
Transfer Capacitance		C_{res}	—	TBD	—	
SWITCHING CHARACTERISTICS (1)						
Turn–Off Delay Time	(V_{CC} = 300 V, I_C = 6.5 A, R_G = 1.0 kΩ, L = 300 μH)	$t_{d(off)}$	—	TBD	—	μSec
Fall Time		t_f	—	TBD	—	
Turn–On Delay Time	(V_{CC} = 10 V, I_C = 6.5 A, R_G = 1.0 kΩ, R_L = 1.0 Ω)	$t_{d(on)}$	—	TBD	—	μSec
Rise Time		t_r	—	TBD	—	
Gate Charge	(V_{CC} = 300 V, I_C = 15 A, V_{GE} = 5.0 V)	Q_T	—	TBD	—	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	

(1) Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

Product Preview

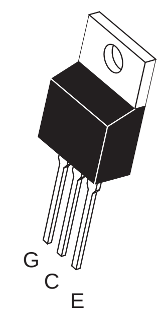
Internally Clamped N-Channel IGBT

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate Collector Over–Voltage Protection from monolithic circuitry for usage as an Ignition Coil Driver.

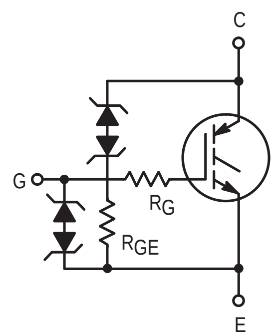
- Temperature Compensated Gate – Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability

MGP15N40CL

15 AMPERES
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.9 V
400 VOLTS
CLAMPED



CASE 221A–09
STYLE 9
TO–220AB



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CER}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Power Dissipation Derate above 25°C	P_D	136 0.91	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 14.2 A, L = 3.0 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 10 A, L = 3.0 mH, Starting T_J = 150°C	E_{AS}	 300 150	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Case — Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Clamp Voltage (I_C = 2.0 mA, T_J = –40°C to 175°C)		$V_{(BR)CES}$	380	410	440	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 350 V, V_{GE} = 0 V)		I_{CES}	—	—	40	μAdc
(V_{CE} = 350 V, V_{GE} = 0 V, T_J = 150°C)			—	—	200	
Gate–Emitter Clamp Voltage (I_G = 5.0 mA)		$V_{(BR)GES}$	17	—	22	Vdc
Gate–Emitter Leakage Current (V_{GE} = 10 V)		I_{GES}	384	—	1000	μAdc
Gate Resistor (optional)		R_G	—	70	—	Ω
Gate Emitter Resistor (optional)		R_{GE}	10	—	26	kΩ
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{GE} = V_{CE}, I_C = 1.0 mA)		$V_{GE(th)}$	1.0	1.8	2.1	Vdc
Threshold Temperature Coefficient (Negative)			—	4.4	—	mV/°C
Collector–to–Emitter On–Voltage (V_{GE} = 4.0 V, I_C = 6.0 A)		$V_{CE(on)}$	—	—	1.8	Volts
(V_{GE} = 4.5 V, I_C = 10 A, T_J = 150°C)			—	—	1.8	
Forward Transconductance (V_{CE} = 5.0 V, I_C = 6.0 A)		g_{fe}	8.0	15	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CC} = 15 V, V_{GE} = 0 V, f = 1.0 MHz)	C_{ies}	—	750	—	pF
Output Capacitance		C_{oes}	—	600	—	
Transfer Capacitance		C_{res}	—	130	—	
SWITCHING CHARACTERISTICS (1)						
Turn–Off Delay Time	(V_{CC} = 380 V, I_C = 6.5 A, R_G = 1.0 kΩ, L = 300 μH)	$t_{d(off)}$	—	4.0	—	μSec
Fall Time		t_f	—	6.0	—	
Turn–On Delay Time	(V_{CC} = 10 V, I_C = 6.5 A, R_G = 1.0 kΩ, R_L = 1.0 Ω)	$t_{d(on)}$	—	2.0	—	μSec
Rise Time		t_r	—	4.0	—	
Gate Charge	(V_{CC} = 350 V, I_C = 15 A, V_{GE} = 5.0 V)	Q_T	—	19	—	nC
		Q_1	—	4.0	—	
		Q_2	—	13	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

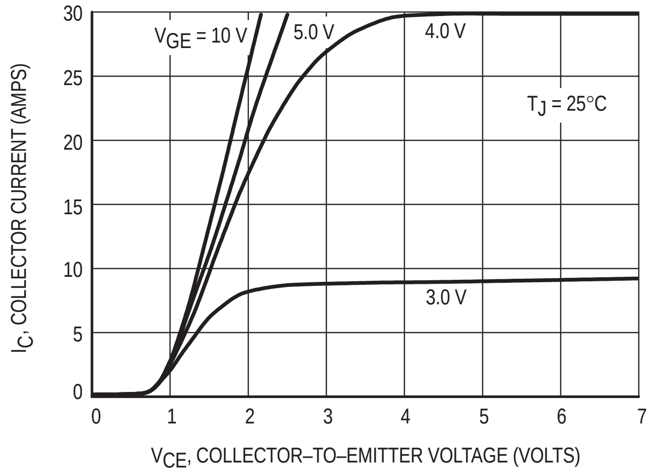


Figure 1. Output Characteristics

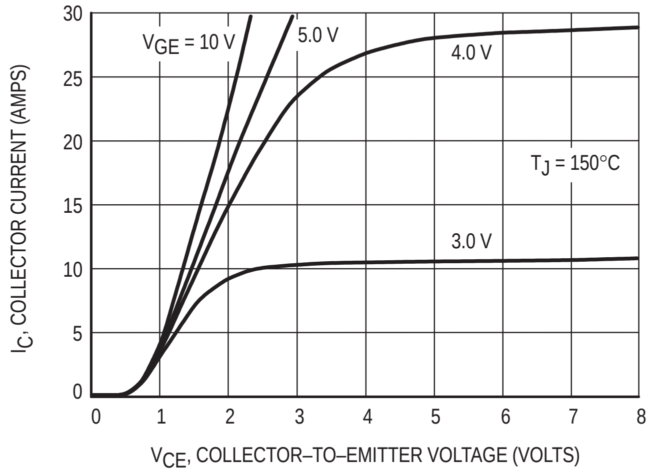


Figure 2. Output Characteristics

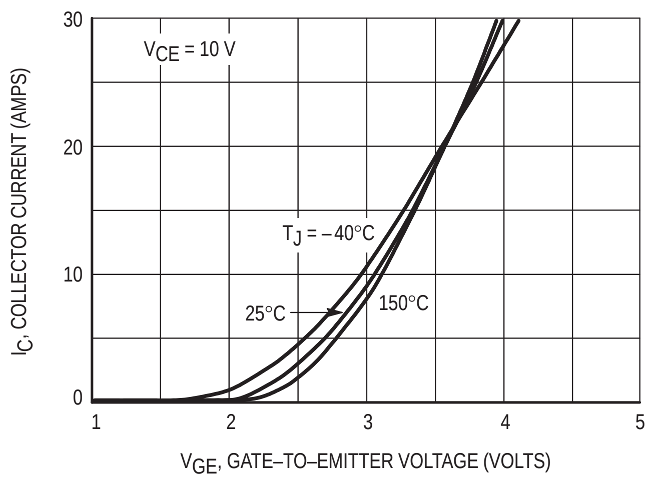


Figure 3. Transfer Characteristics

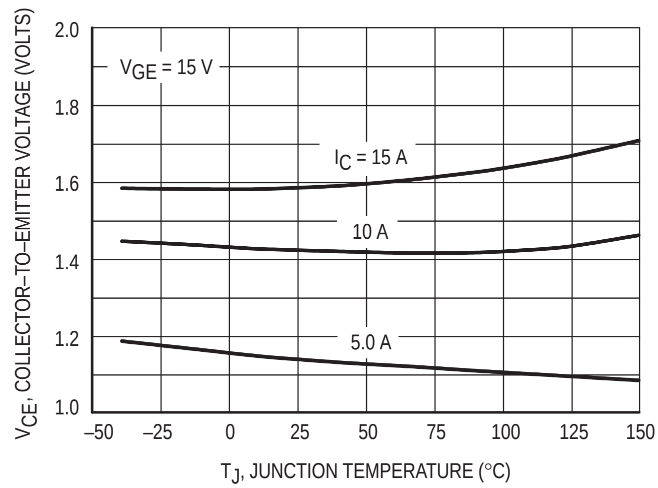


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

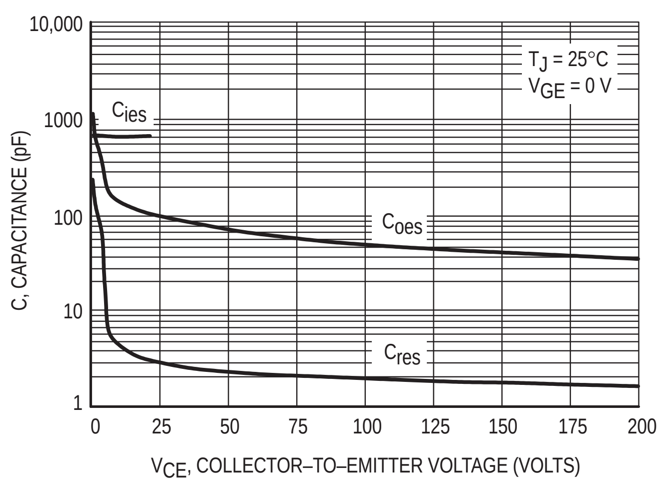


Figure 5. Capacitance Variation

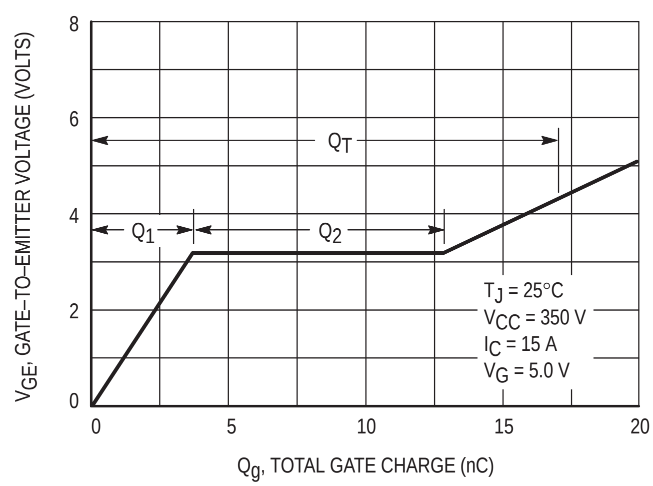


Figure 6. Gate–To–Emitter Voltage versus Total Charge

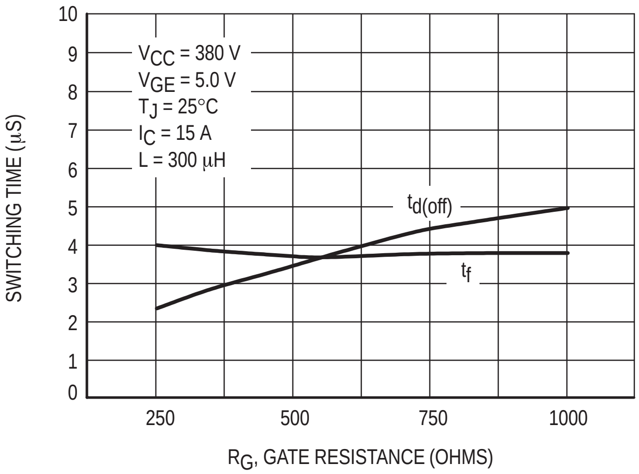


Figure 7. Switching Speed versus Gate Resistance

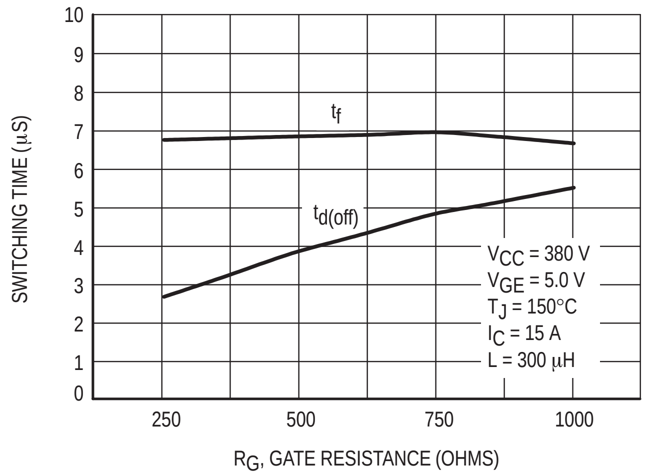


Figure 8. Switching Speed versus Gate Resistance

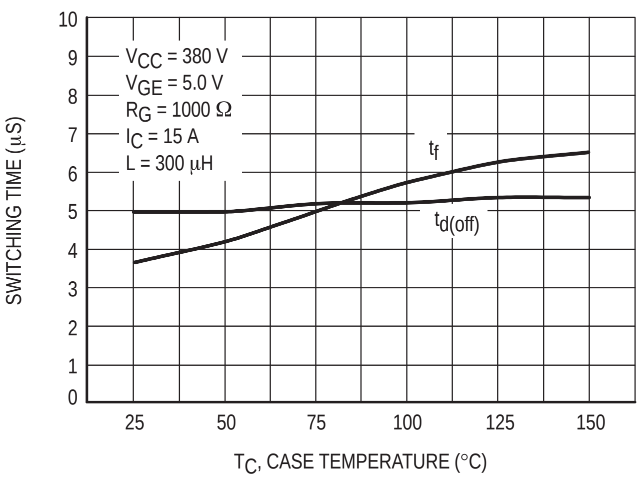


Figure 9. Switching Speed versus Case Temperature

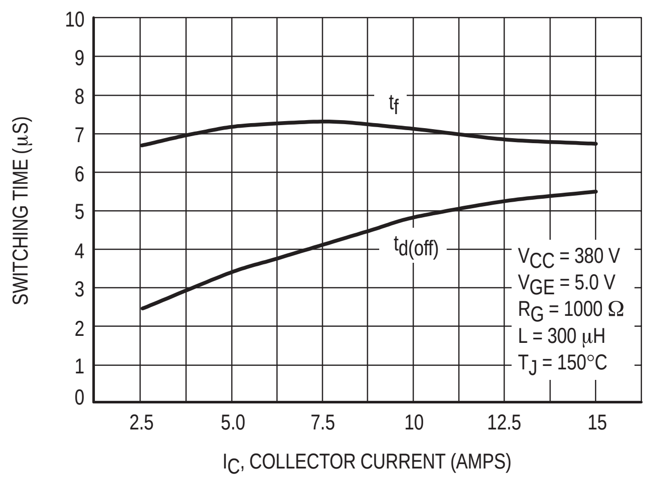


Figure 10. Total Switching Losses versus Collector Current

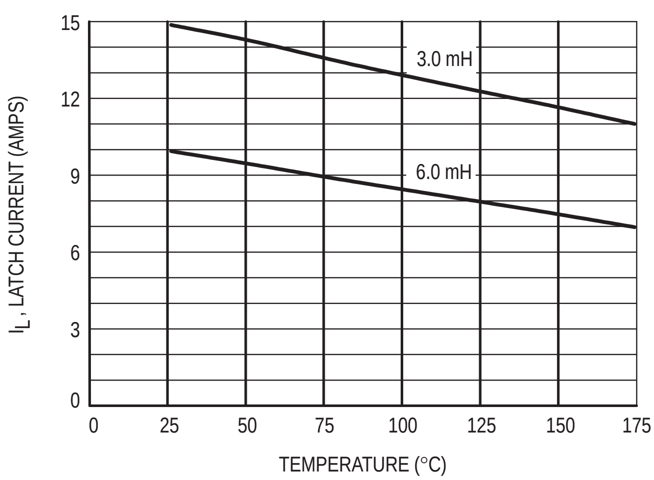


Figure 11. Latch Current versus Temperature

Product Preview

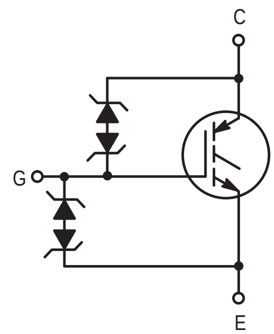
Internally Clamped N-Channel IGBT

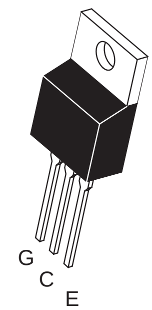
MGP15N43CL

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate Collector Over–Voltage Protection from monolithic circuitry for usage as an Ignition Coil Driver.

- Temperature Compensated Gate – Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability

15 AMPERES
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.8 V
430 VOLTS
CLAMPED





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CER}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Power Dissipation Derate above 25°C	P_D	136 0.91	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 14.2 A, L = 3.0 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 10 A, L = 3.0 mH, Starting T_J = 150°C	E_{AS}	 300 150	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Case — Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Clamp Voltage (I_C = 1.0 mA, T_J = –40°C to 175°C)		$V_{(BR)CES}$	—	430	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 360 V, V_{GE} = 0 V)		I_{CES}	—	—	10	µAdc
(V_{CE} = 360 V, V_{GE} = 0 V, T_J = 150°C)			—	—	150	
Gate–Emitter Clamp Voltage (I_G = 5.0 mA)		$V_{(BR)GES}$	17	—	22	Vdc
Gate–Emitter Leakage Current (V_{GE} = 10 V)		I_{GES}	—	—	10	µAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{GE} = V_{CE}, I_C = 1.0 mA)		$V_{GE(th)}$	1.3	1.8	2.1	Vdc
Threshold Temperature Coefficient (Negative)			—	4.4	—	mV/°C
Collector–to–Emitter On–Voltage (V_{GE} = 3.5 V, I_C = 6.0 A)		$V_{CE(on)}$	—	—	2.0	Volts
(V_{GE} = 4.0 V, I_C = 10 A, T_J = 150°C)			—	—	1.8	
Forward Transconductance (V_{CE} = 5.0 V, I_C = 10 A)		g_{fe}	8.0	20	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CC} = 15 V, V_{GE} = 0 V, f = 1.0 MHz)	C_{ies}	—	TBD	—	pF
Output Capacitance		C_{oes}	—	TBD	—	
Transfer Capacitance		C_{res}	—	TBD	—	
SWITCHING CHARACTERISTICS (1)						
Turn–Off Delay Time	(V_{CC} = 400 V, I_C = 6.5 A, R_G = 1.0 kΩ, L = 300 µH)	$t_{d(off)}$	—	TBD	—	µSec
Fall Time		t_f	—	TBD	—	
Turn–On Delay Time	(V_{CC} = 10 V, I_C = 6.5 A, R_G = 1.0 kΩ, R_L = 1.0 Ω)	$t_{d(on)}$	—	TBD	—	µSec
Rise Time		t_r	—	TBD	—	
Gate Charge	(V_{CC} = 350 V, I_C = 15 A, V_{GE} = 5.0 V)	Q_T	—	TBD	—	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	

(1) Pulse Test: Pulse Width ≤ 300 µS, Duty Cycle ≤ 2%.

Product Preview

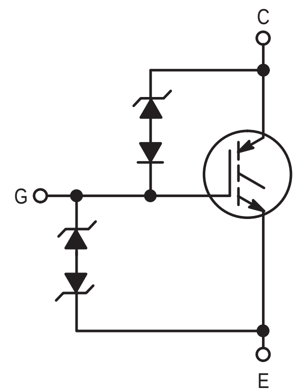
SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

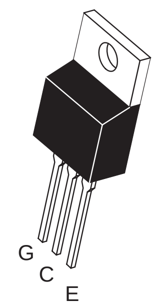
MGP20N14CL

20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.9 VOLTS
135 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous — Single Pulsed (t_p = ± 10 µs)	I_C I_{CM}	20 60	Adc Apk
Total Power Dissipation (TO–220) Derate Above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C (V_{CC} = 80 V, V_{GE} = 5 V, Peak I_L = 10 A, L = 10 mH)	E_{AS}	500	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Clamp Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)		$V_{(BR)CES}$	135			Vdc
Zero Gate Voltage Collector Current (V_{CE} = 100 V, V_{GE} = 0 V)		I_{CES}	—	—	10	μA
(V_{CE} = 100 V, V_{GE} = 0 V, T_J = 150°C)			—	—	100	
Gate–Emitter Clamp Voltage (I_G = 1 mA)		$V_{(BR)GES}$	10			Vdc
Gate–Emitter Leakage Current (V_{GE} = ± 5 V, V_{CE} = 0 V)		I_{GES}	—	—	1.0	μA
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA)		$V_{GE(th)}$	1.0	1.5	2.0	V
Threshold Temperature Coefficient (Negative)				4.4		mV/°C
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 10 A)		$V_{CE(on)}$	—		1.9	V
(V_{GE} = 5 V, I_C = 10 Adc, T_J = 175°C)			—		1.8	
Forward Transconductance (V_{CE} > 15 V, I_C = 10 A)		g_{fe}	8.0	15	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	430	600	pF
Output Capacitance		C_{oes}	—	182	250	
Transfer Capacitance		C_{res}	—	48	100	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 68 V, I_C = 20 A, V_{GE} = 5 V, R_G = 9.1 Ω)	$t_{d(on)}$	—	TBD	TBD	ns
Rise Time		t_r	—	TBD	TBD	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	TBD	
Fall Time		t_f	—	TBD	TBD	
Total Gate Charge	(V_{CC} = 108 V, I_C = 20 A, V_{GE} = 5 V)	Q_T	—	14	20	nC
Gate–Emitter Charge		Q_{ge}	—	3.0	—	
Gate–Collector Charge		Q_{gc}	—	6.0	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Advanced Information

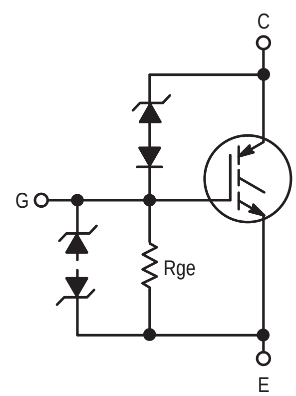
SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

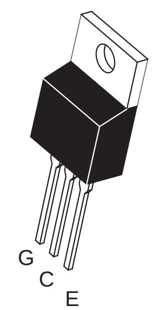
MGP20N35CL

20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.8 VOLTS
350 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C	I_C	20	Adc
Reversed Collector Current – pulse width $<$ 100 μs	I_{CR}	12	Apk
Total Power Dissipation @ T_C = 25°C (TO–220)	P_D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C @ Starting T_J = 150°C	E_{AS}	 550 150	mJ

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)		$V_{(BR)CES}$	320	350	380	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 250 V, V_{GE} = 0 V, T_J = 125°C) (V_{CE} = 15 V, V_{GE} = 0 V, T_J = 125°C)		I_{CES}	— —	— —	1.0 200	mA µA
Resistance Gate–Emitter (T_J = –40 to 150°C)		R_{GE}	10k	16k	30k	Ω
Gate–Emitter Breakdown Voltage (I_G = 2 mA)		$V_{(BR)GES}$	11	13	15	± V
Collector–Emitter Reverse Leakage (V_{CE} = –15 V, T_J = –40 to 150°C)		I_{ECS}	—	8	100	mA
Collector–Emitter Reversed Breakdown Voltage (I_E = 75 mA)		$V_{(BR)ECS}$	26	40	120	V
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA) (V_{CE} = V_{GE}, I_C = 1 mA, T_J = 150°C)		$V_{GE(th)}$	1.0 0.75	1.7 —	2.4 1.8	V
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 5 A) (V_{GE} = 5 V, I_C = 10 A) (V_{GE} = 5 V, I_C = 10 Adc, T_J = 150°C)		$V_{CE(on)}$	— — —	1.1 1.4 1.4	1.4 1.9 1.8	V
Forward Transconductance (V_{CE} > 50 V, I_C = 10 A)		g_{fe}	10	16	—	S
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	2800	—	pF
Output Capacitance		C_{oes}	—	200	—	
Transfer Capacitance		C_{res}	—	25	—	
SWITCHING CHARACTERISTICS (1)						
Total Gate Charge	(V_{CC} = 280 V, I_C = 20 A, V_{GE} = 5 V)	Q_g	—	45	80	nC
Gate–Emitter Charge		Q_{ge}	—	8.0	—	
Gate–Collector Charge		Q_{gc}	—	20	—	
Turn–Off Delay Time	(V_{CC} = 320 V, I_C = 20 A, L = 200 µH, R_G = 1 KΩ)	$t_{d(off)}$	—	TBD	TBD	µs
Fall Time		t_f	—	TBD	TBD	
Turn–On Delay Time	(V_{CC} = 14 V, I_C = 20 A, L = 200 µH, R_G = 1 KΩ)	$t_{d(on)}$	—	TBD	TBD	µs
Rise Time		t_r	—	TBD	TBD	

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

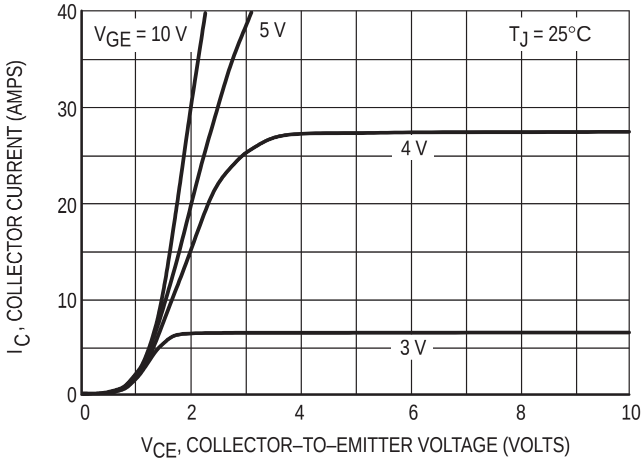


Figure 1. Output Characteristics

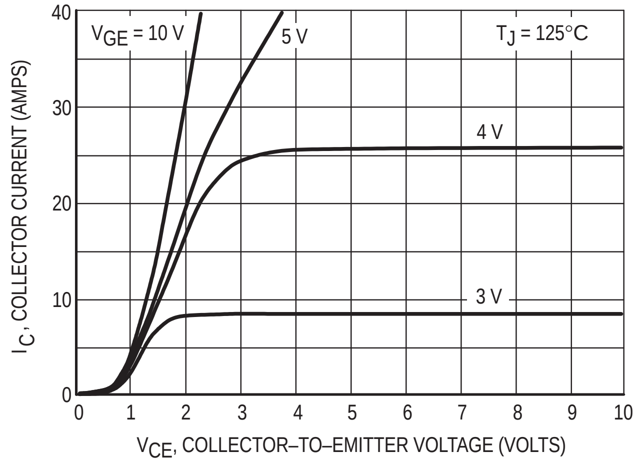


Figure 2. Output Characteristics

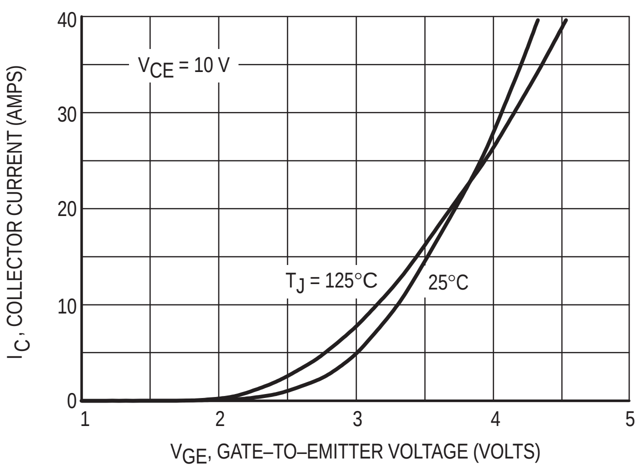


Figure 3. Transfer Characteristics

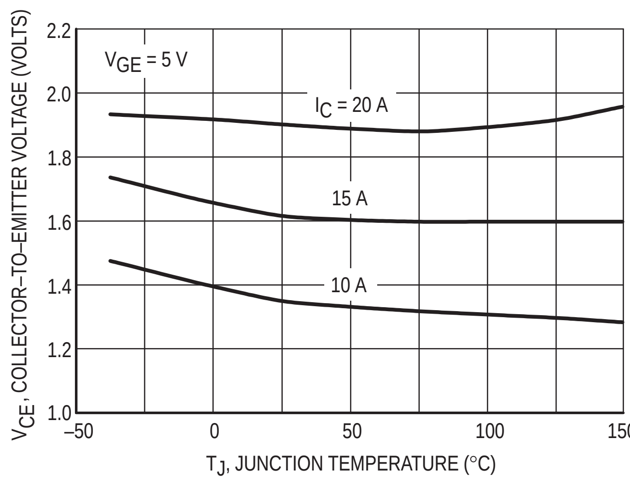


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

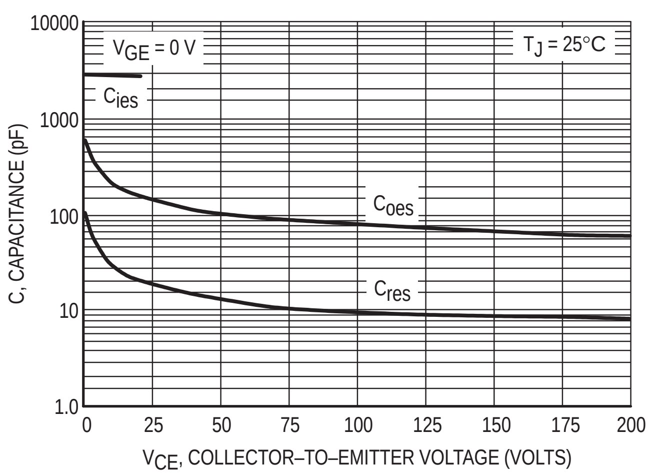


Figure 5. Capacitance Variation

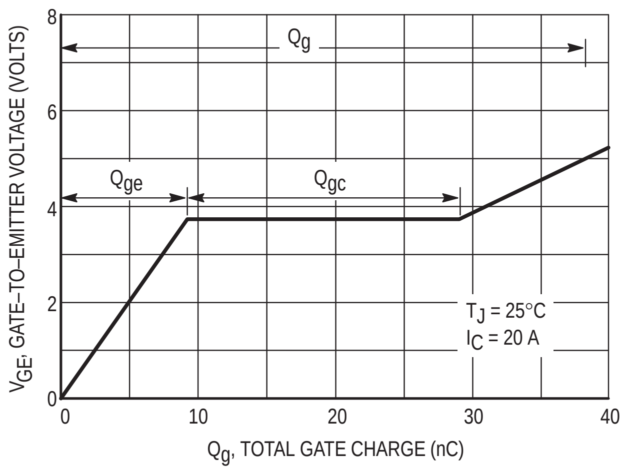


Figure 6. Gate–to–Emitter Voltage versus Total Charge

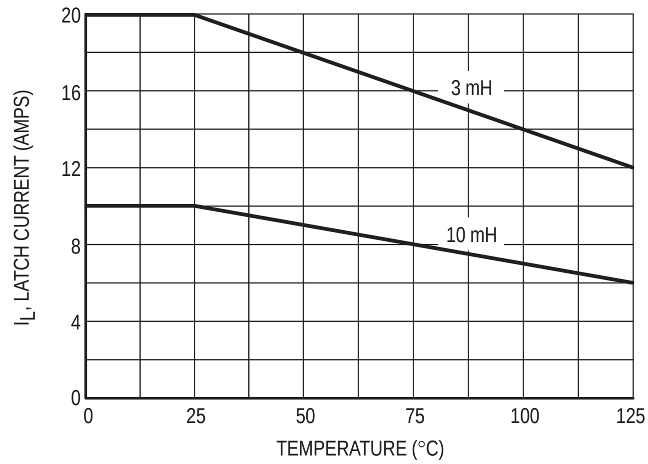


Figure 7. Latch Current versus Temperature

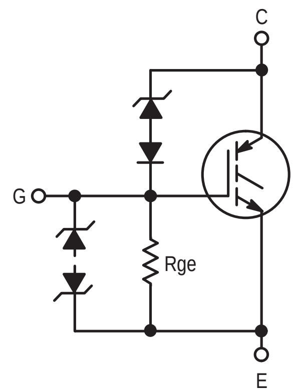
Advanced Information
SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

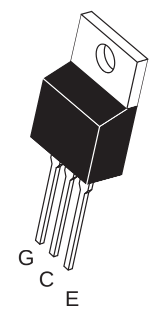
MGP20N40CL

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability

20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.8 VOLTS
400 VOLTS (CLAMPED)





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C	I_C	20	Adc
Reversed Collector Current – pulse width $<$ 100 μs	I_{CR}	12	Apk
Total Power Dissipation @ T_C = 25°C (TO–220)	P_D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C @ Starting T_J = 150°C	E_{AS}	 550 150	mJ

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)		$V_{(BR)CES}$	370	405	430	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 350 V, V_{GE} = 0 V, T_J = 150°C)		I_{CES}	—	—	500	μA
(V_{CE} = 15 V, V_{GE} = 0 V, T_J = 150°C)			—	—	100	
Resistance Gate–Emitter (T_J = –40 to 150°C)		R_{GE}	10k	16k	30k	Ω
Gate–Emitter Breakdown Voltage (I_G = 2 mA)		$V_{(BR)GES}$	11	13	15	± V
Collector–Emitter Reverse Leakage (V_{CE} = –15 V, T_J = 150°C)		I_{ECS}	—	—	50	mA
Collector–Emitter Reversed Breakdown Voltage (I_E = 75 mA)		$V_{(BR)ECS}$	26	40	120	V
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA)		$V_{GE(th)}$	1.0	1.7	2.2	V
(V_{CE} = V_{GE}, I_C = 1 mA, T_J = 150°C)			0.75	—	1.8	
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 5 A)		$V_{CE(on)}$	—	1.1	1.4	V
(V_{GE} = 5 V, I_C = 10 A)			—	1.4	1.9	
(V_{GE} = 5 V, I_C = 10 Adc, T_J = 150°C)			—	1.4	1.8	
Forward Transconductance (V_{CE} > 5.0 V, I_C = 10 A)		g_{fe}	10	18	—	S
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	2800	—	pF
Output Capacitance		C_{oes}	—	200	—	
Transfer Capacitance		C_{res}	—	25	—	
SWITCHING CHARACTERISTICS (1)						
Total Gate Charge	(V_{CC} = 280 V, I_C = 20 A, V_{GE} = 5 V)	Q_g	—	45	80	nC
Gate–Emitter Charge		Q_{ge}	—	8.0	—	
Gate–Collector Charge		Q_{gc}	—	20	—	
Turn–Off Delay Time	(V_{CC} = 320 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)	$t_{d(off)}$	—	14	—	μs
Fall Time		t_f	—	4.0	—	
Turn–On Delay Time	(V_{CC} = 14 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)	$t_{d(on)}$	—	2.0	—	μs
Rise Time		t_r	—	6.0	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

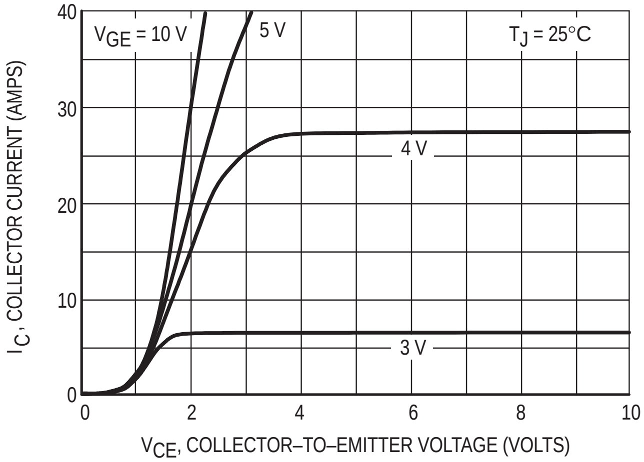


Figure 1. Output Characteristics

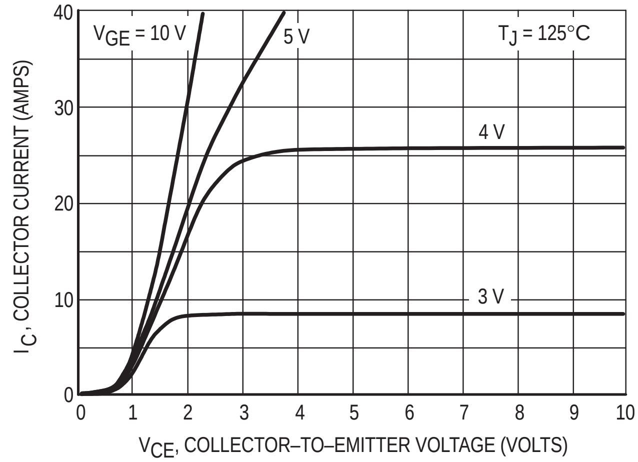


Figure 2. Output Characteristics

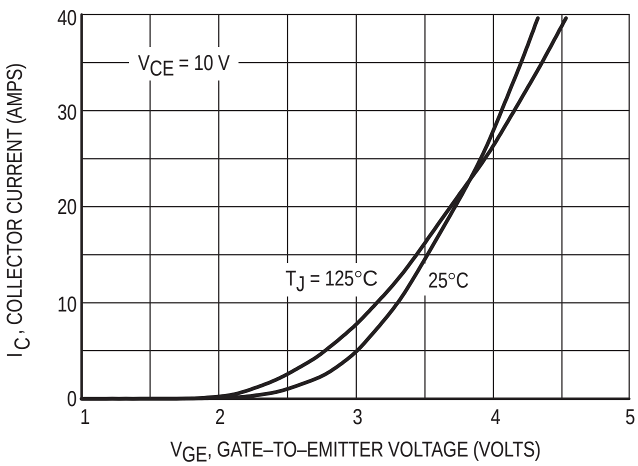


Figure 3. Transfer Characteristics

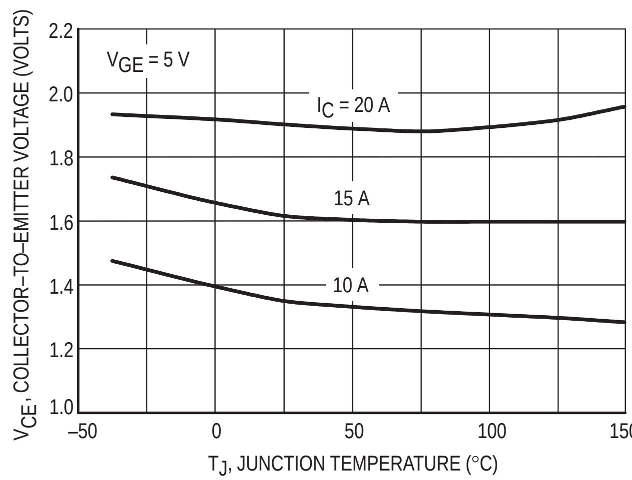


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

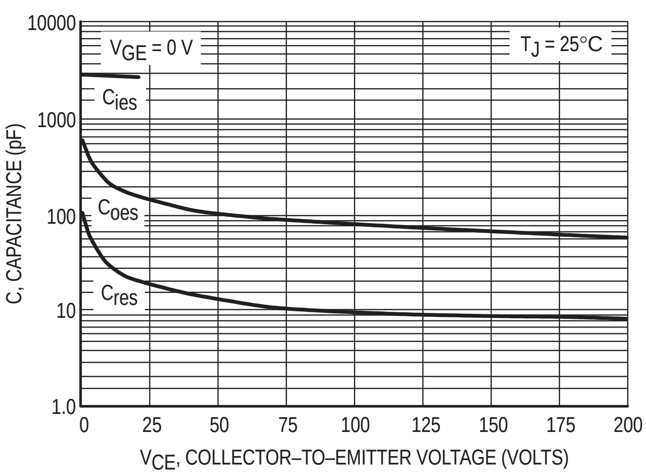


Figure 5. Capacitance Variation

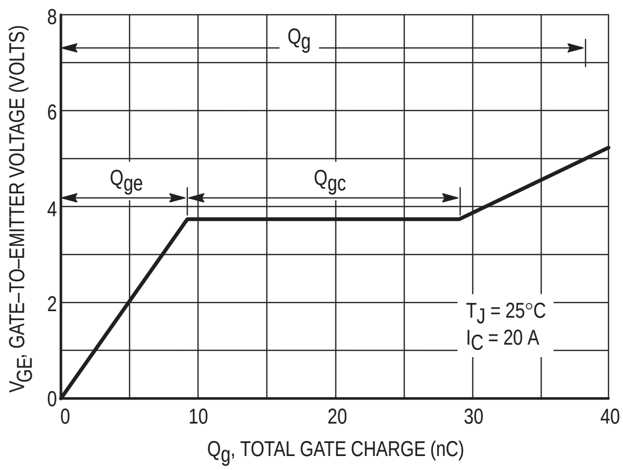


Figure 6. Gate–to–Emitter Voltage versus Total Charge

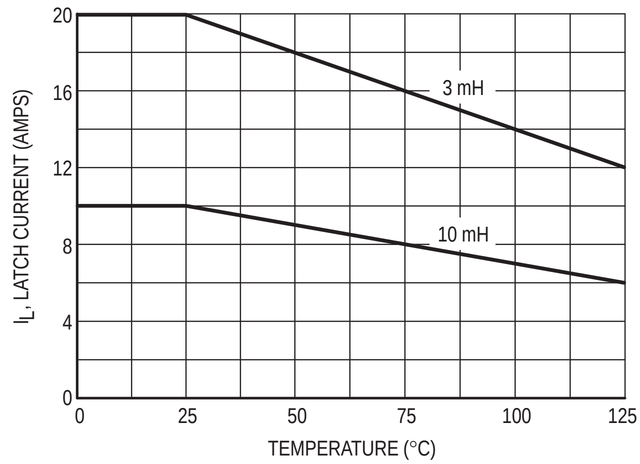


Figure 7. Latch Current versus Temperature

Product Preview

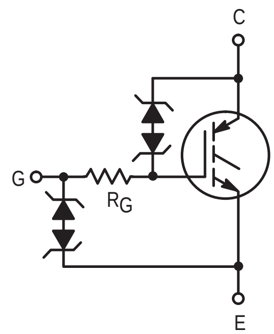
Internally Clamped N-Channel IGBT

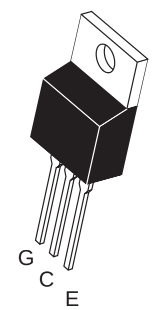
MGP20N63CL

**20 AMPERES
N–CHANNEL IGBT
$V_{CE(on)}$ = 1.7 V
630 VOLTS
CLAMPED**

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate Collector Over–Voltage Protection from monolithic circuitry for usage as an Ignition Coil Driver.

- Temperature Compensated Gate – Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability





**CASE 221A–09
STYLE 9
TO–220AB**

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CER}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous	I_C	20	Adc
Total Power Dissipation Derate above 25°C	P_D	180 1.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS (T_J < 150°C)			
Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 14.2 A, L = 3.0 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, PEAK I_L = 10 A, L = 3.0 mH, Starting T_J = 150°C	E_{AS}	 650 350	mJ
THERMAL CHARACTERISTICS			
Thermal Resistance — Junction–to–Case — Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.8 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Clamp Voltage (I_C = 1.0 mA, T_J = –40°C to 175°C)		$V_{(BR)CES}$	—	630	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 500 V, V_{GE} = 0 V) (V_{CE} = 500 V, V_{GE} = 0 V, T_J = 150°C)		I_{CES}	— —	— —	100 2000	μAdc
Gate–Emitter Clamp Voltage (I_G = 5.0 mA)		$V_{(BR)GES}$	17	—	22	Vdc
Gate–Emitter Leakage Current (V_{GE} = 10 V)		I_{GES}	—	—	20	μAdc
Gate–Resistor		R_G	—	400	—	Ω
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{GE} = V_{CE}, I_C = 1.0 mA) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	— —	1.7 4.4	— —	Vdc mV/°C
Collector–to–Emitter On–Voltage (V_{GE} = 3.5 V, I_C = 6.0 A) (V_{GE} = 4.0 V, I_C = 10 A, T_J = 150°C)		$V_{CE(on)}$	— —	1.6 1.7	— —	Volts
Forward Transconductance (V_{CE} = 5.0 V, I_C = 10 A)		g_{fe}	—	20	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CC} = 15 V, V_{GE} = 0 V, f = 1.0 MHz)	C_{ies}	—	TBD	—	pF
Output Capacitance		C_{oes}	—	TBD	—	
Transfer Capacitance		C_{res}	—	TBD	—	
SWITCHING CHARACTERISTICS (1)						
Turn–Off Delay Time	(V_{CC} = 600 V, I_C = 10 A, R_G = 1.0 kΩ, L = 300 μH)	$t_{d(off)}$	—	TBD	—	μSec
Fall Time		t_f	—	TBD	—	
Turn–On Delay Time	(V_{CC} = 10 V, I_C = 10 A, R_G = 1.0 kΩ, R_L = 1.0 Ω)	$t_{d(on)}$	—	TBD	—	μSec
Rise Time		t_r	—	TBD	—	
Gate Charge		Q_T	—	TBD	—	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	

(1) Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

Preliminary Data Sheet

Insulated Gate Bipolar Transistor

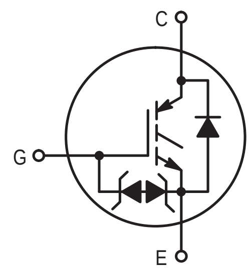
N–Channel Enhancement–Mode Silicon Gate

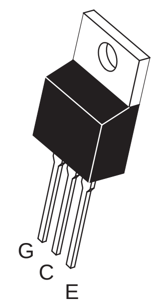
MGP2N60D

POWERLUX IGBT
1.5 AMPS
600 VOLTS

This Insulated Gate Bipolar Transistor (IGBT) contains a built–in free wheeling diode and a gate protection zener. Fast switching characteristics result in efficient operation at higher frequencies.

- Built In Free Wheeling Diode
- Built In Gate Protection Zener Diode
- Industry Standard Package TO220
- High Speed: E_{off} = 35 μJ/A Typical at 125°C
- Robust High Voltage Termination





CASE 221A–09
STYLE 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameters	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±15	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	1.5 0.9 6.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	75	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.67 TBD 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C/W

(1) Pulse width limited by maximum junction temperature repetitive rating.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 750 μAdc)		$V_{(BR)CES}$	600	680	—	Vdc
Temperature Coefficient (Positive)			—	670	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	0.3	15	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	15	150	
Gate–Body Leakage Current (V_{GE} = ±15 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	30	300	μAdc
ON CHARACTERISTICS						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 0.9 Adc, T_C = 25°C)		$V_{CE(on)}$	—	1.6	2.0	Vdc
(V_{GE} = 15 Vdc, I_C = 0.9 Adc, T_C = 125°C)			—	1.5	—	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 750 μAdc)		$V_{GE(th)}$	4.0	—	6.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.0	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 1.5 Adc)		g_{fe}	0.3	0.42	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 20 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	300	TBD	pF
Output Capacitance		C_{oes}	—	75	TBD	
Transfer Capacitance		C_{res}	—	30	TBD	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 0.9 Adc)		V_{FEC}	—	5.3	6.0	Vdc
(I_{EC} = 0.9 Adc, T_J = 125°C)			—	5.7	—	
(I_{EC} = 0.3 Adc)			—	2.7	TBD	
(I_{EC} = 0.3 Adc, T_J = 125°C)			—	2.6	—	
Reverse Recovery Time	(I_F = 0.3 Adc, V_R = 300 Vdc, dI_F/dt = 10 A/μs)	t_{rr}	—	TBD	—	ns
	(I_F = 0.9 Adc, V_R = 300 Vdc, dI_F/dt = 10 A/μs)		—	TBD	—	
Reverse Recovery Stored Charge	(I_F = 0.3 Adc, V_R = 300 Vdc, dI_F/dt = 10 A/μs)	Q_{RR}	—	TBD	—	μC
Forward Recovery Time, (I_F = 0.3 Adc, dI_F/dt = 10 A/μs)		t_{fr}	—	TBD	—	ns
(I_F = 0.9 Adc, dI_F/dt = 10 A/μs)			—	TBD	—	
(I_F = 1.5 Adc, dI_F/dt = 10 A/μs)			—	TBD	—	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 300 Vdc, I_C = 1.2 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 10 Ω) Energy losses include "tail" Power Supply, Z_O = 50 Ω	$t_{d(on)}$	—	TBD	—	ns
Rise Time		t_r	—	TBD	—	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	—	
Fall Time		t_f	—	130	—	
Turn–Off Switching Loss		E_{off}	—	TBD	—	μJ
Turn–On Switching Loss		E_{on}	—	TBD	—	
Total Switching Loss		E_{ts}	—	TBD	—	
Turn–On Delay Time	(V_{CC} = 300 Vdc, I_C = 1.2 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 10 Ω, T_J = 125°C) Energy losses include "tail" Power Supply, Z_O = 50 Ω	$t_{d(on)}$	—	TBD	—	ns
Rise Time		t_r	—	TBD	—	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	—	
Fall Time		t_f	—	270	—	
Turn–Off Switching Loss		E_{off}	—	TBD	—	μJ
Turn–On Switching Loss		E_{on}	—	TBD	—	
Total Switching Loss		E_{ts}	—	TBD	—	
Gate Charge	(V_{CC} = 300 Vdc, I_C = 0.9 Adc, V_{GE} = 15 V)	Q_T	—	TBD	—	nC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

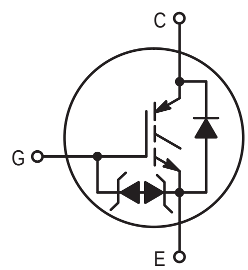
N–Channel Enhancement–Mode Silicon Gate

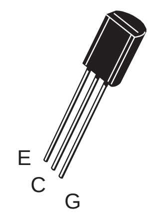
MGS05N60D

POWERLUX IGBT
0.5 A @ 25°C
600 V

This IGBT contains a built–in free wheeling diode and a gate protection zener diodes. Fast switching characteristics result in efficient operation at higher frequencies. This device is ideally suited for high frequency electronic ballasts.

- Built–In Free Wheeling Diodes
- Built–In Gate Protection Zener Diode
- Industry Standard Package (TO92 — 1.0 Watt)
- High Speed E_{off}: Typical 6.5 µJ @ I_C = 0.3 A; T_C = 125°C and dV/dt = 1000 V/µs
- Robust High Voltage Termination
- Robust Turn–Off SOA





CASE 029–05
STYLE 35
TO–226AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameters	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GES}	±15	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	0.5 0.3 2.0	Adc
Total Power Dissipation	P_D	1.0	Watt
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Parameters	Symbol	Value	Unit
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	25 125	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_C ≤ 150°C)

Parameters	Symbol	Value	Unit
Single Pulse Drain–to–Source Avalanche Energy – Starting @ T_C = 25°C @ T_C = 125°C V_{CE} = 100 V, V_{GE} = 15 V, Peak I_L = 2.0 A, L = 3.0 mH, R_G = 25 Ω	E_{AS}	 125 40	mJ

(1) Pulse width is limited by maximum junction temperature repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		$V_{(BR)CES}$	600	680	—	Vdc
Temperature Coefficient (Positive)			—	0.7	—	V/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	0.1	5.0	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_C = 125°C)		I_{CES}	—	5.0	50	
Gate–Body Leakage Current (V_{GE} = ±15 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	10	100	μAdc
ON CHARACTERISTICS						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 0.3 Adc)		$V_{CE(on)}$	—	1.6	2.0	Vdc
(V_{GE} = 15 Vdc, I_C = 0.3 Adc, T_C = 125°C)			—	1.5	—	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 250 μAdc)		$V_{GE(th)}$	3.5	—	6.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 0.5 Adc)		g_{fe}	0.3	0.42	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 20 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	75	100	pF
Output Capacitance		C_{oes}	—	11	20	
Transfer Capacitance		C_{res}	—	1.6	5.0	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 0.3 Adc)		V_{FEC}	—	5.0	6.0	Vdc
(I_{EC} = 0.3 Adc, T_C = 125°C)			—	5.2	—	
(I_{EC} = 0.1 Adc)			—	2.3	3.0	
(I_{EC} = 0.1 Adc, T_C = 125°C)			—	2.3	—	
Reverse Recovery Time	(I_F = 0.4 Adc, V_R = 300 Vdc, dIF/dt = 10 A/μs)	t_{rr}	—	150	—	ns
Reverse Recovery Stored Charge		Q_{RR}	—	35	—	μC
SWITCHING CHARACTERISTICS (1)						
Turn–Off Delay Time	(V_{CC} = 300 Vdc, I_C = 0.4 Adc, V_{GE} = 15 Vdc, L = 3.0 mH, R_G = 25 Ω, dV/dt = 1000 V/μs) Energy losses include “tail”	$t_{d(off)}$	—	28	—	ns
Fall Time		t_f	—	150	—	
Turn–Off Switching Loss		E_{off}	—	3.25	4.25	μJ
Turn–Off Delay Time	(V_{CC} = 300 Vdc, I_C = 0.4 Adc, V_{GE} = 15 Vdc, L = 3.0 mH, R_G = 25 Ω, T_C = 125°C, dV/dt = 1000 V/μs) Energy losses include “tail”	$t_{d(off)}$	—	21	—	ns
Fall Time		t_f	—	280	—	
Turn–Off Switching Loss		E_{off}	—	8.0	10	μJ
Gate Charge	(V_{CC} = 300 Vdc, I_C = 0.3 Adc, V_{GE} = 15 Vdc)	Q_T	—	6.4	—	nC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

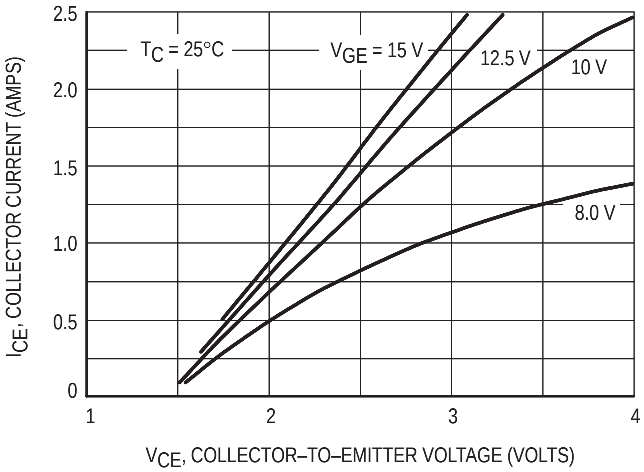


Figure 1. Saturation Characteristics

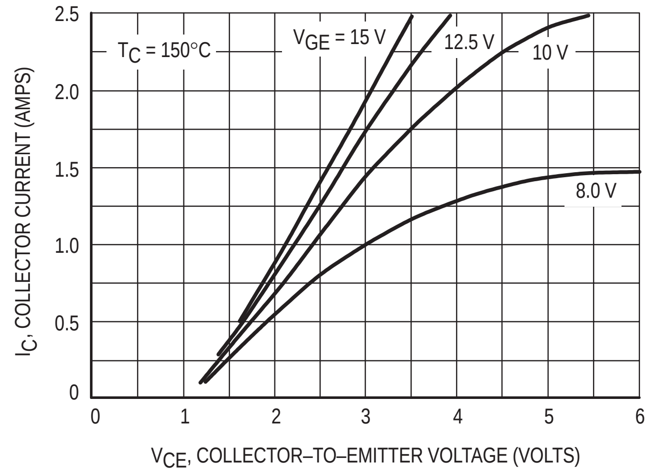


Figure 2. Saturation Characteristics

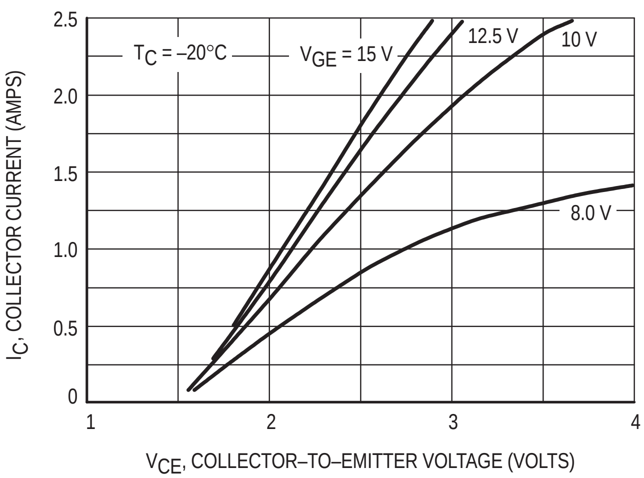


Figure 3. Saturation Characteristics

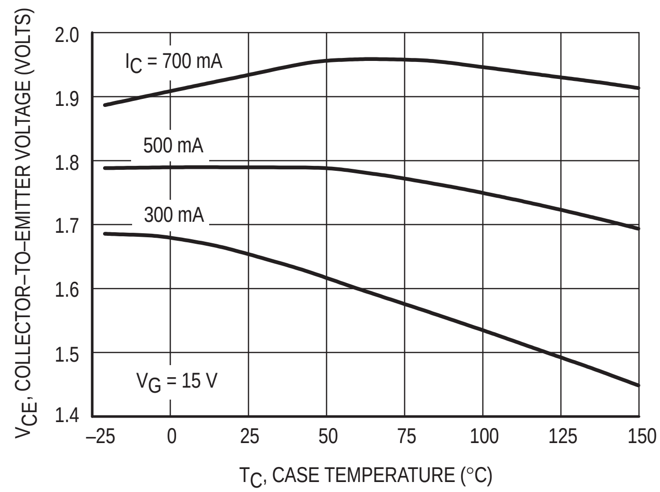


Figure 4. Collector–To–Emitter Saturation Voltage versus Case Temperature

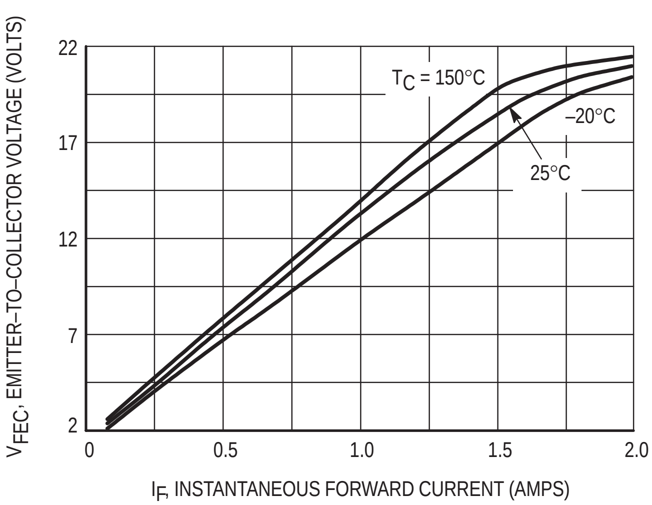


Figure 5. Diode Forward Voltage Drop

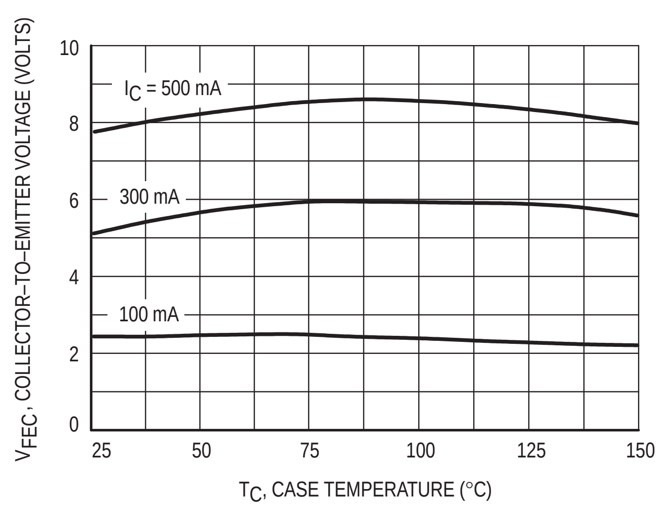


Figure 6. Diode Forward Voltage versus Case Temperature

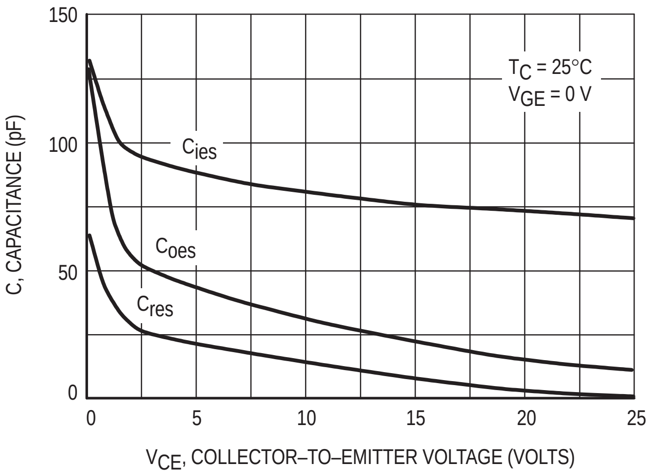


Figure 7. Capacitance Variation

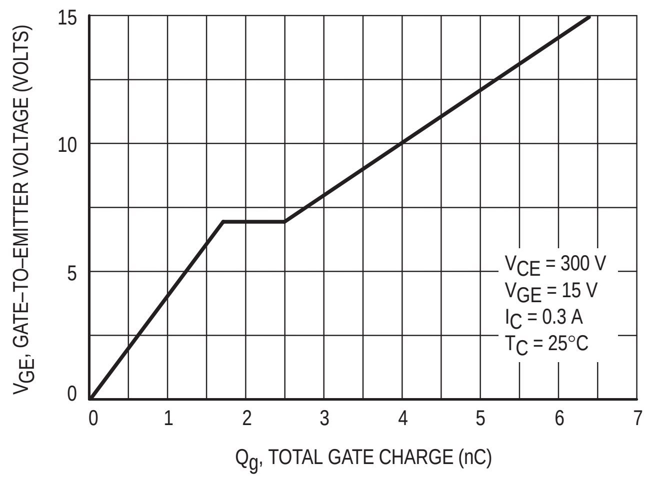


Figure 8. Gate–To–Emitter Voltage versus Total Charge

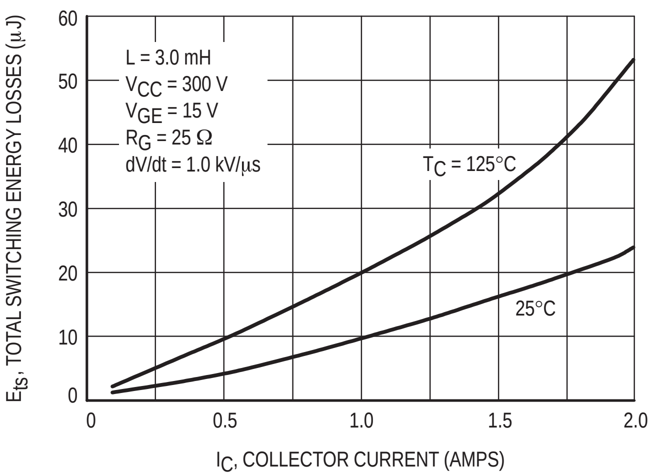


Figure 9. Total Switching Losses versus Collector Current

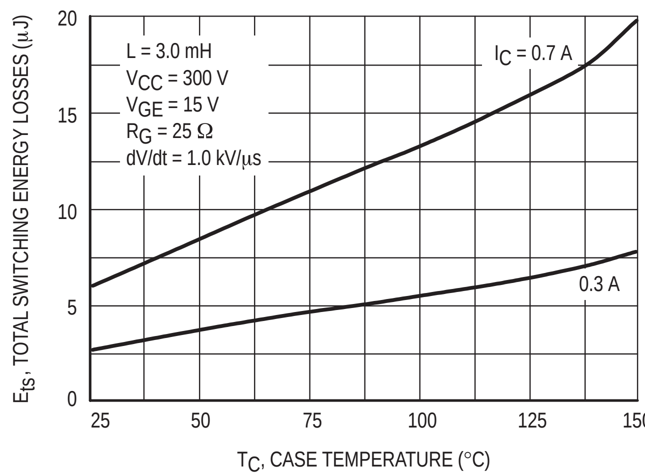


Figure 10. Total Switching Losses versus Case Temperature

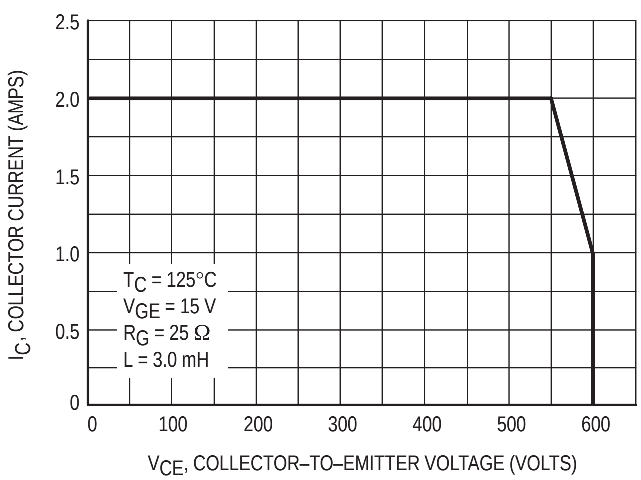


Figure 11. Minimum Turn–Off Safe Operating Area

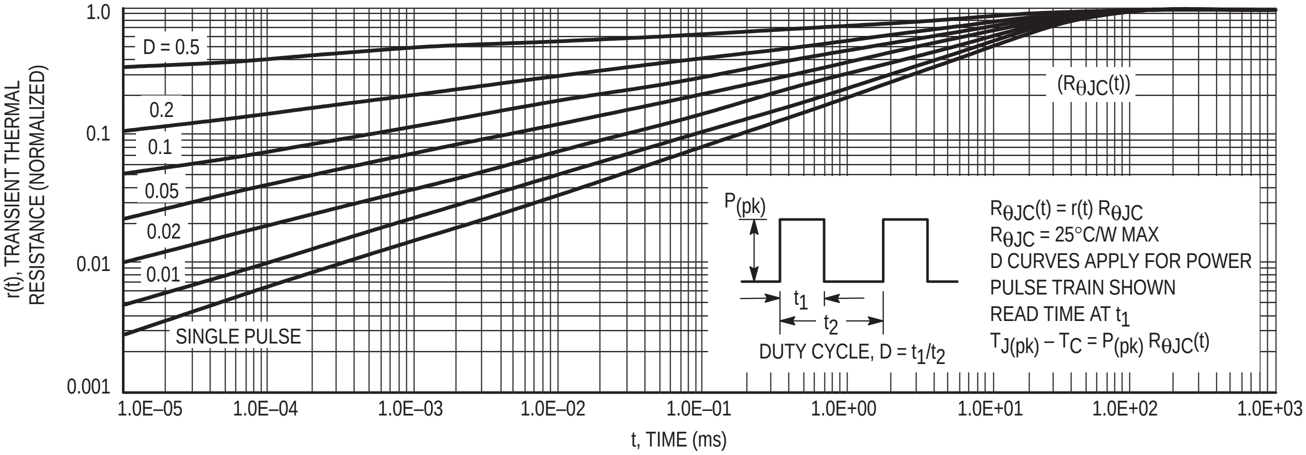


Figure 12. Typical Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

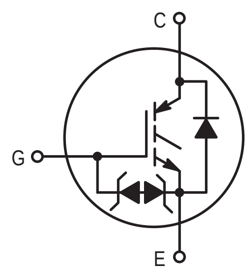
N–Channel Enhancement–Mode Silicon Gate

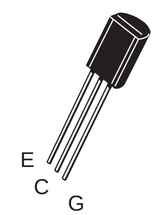
MGS13002D

This IGBT contains a built–in free wheeling diode and a gate protection zener diodes. Fast switching characteristics result in efficient operation at higher frequencies. This device is ideally suited for high frequency electronic ballasts.

- Built–In Free Wheeling Diodes
- Built–In Gate Protection Zener Diode
- Industry Standard Package (TO92 — 1.0 Watt)
- High Speed E_{off}: Typical 6.5 µJ @ I_C = 0.3 A; T_C = 125°C and dV/dt = 1000 V/µs
- Robust High Voltage Termination
- Robust Turn–Off SOA

**POWERLUX
IGBT
0.5 A @ 25°C
600 V**





**CASE 029–05
STYLE 35
TO–226AE**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameters	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GES}	±15	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	0.5 0.3 2.0	Adc
Total Power Dissipation @ T_C = 25°C	P_D	1.0	Watt
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – IGBT Thermal Resistance — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	25 125	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_C ≤ 150°C)

Single Pulse Drain–to–Source Avalanche Energy – Starting @ T_C = 25°C @ T_C = 125°C V_{CE} = 100 V, V_{GE} = 15 V, Peak I_L = 2.0 A, L = 3.0 mH, R_G = 25 Ω	E_{AS}	 125 40	mJ

(1) Pulse width is limited by maximum junction temperature repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		$V_{(BR)CES}$	600	680	—	Vdc
Temperature Coefficient (Positive)			—	0.7	—	V/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	0.1	5.0	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_C = 125°C)			—	5.0	50	
Gate–Body Leakage Current (V_{GE} = ±15 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	10	100	μAdc
ON CHARACTERISTICS						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 0.3 Adc)		$V_{CE(on)}$	—	1.6	2.0	Vdc
(V_{GE} = 15 Vdc, I_C = 0.3 Adc, T_C = 125°C)			—	1.5	—	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 250 μAdc)		$V_{GE(th)}$	3.5	—	6.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 0.5 Adc)		g_{fe}	0.3	0.42	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 20 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	75	100	pF
Output Capacitance		C_{oes}	—	11	20	
Transfer Capacitance		C_{res}	—	1.6	5.0	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 0.3 Adc)		V_{FEC}	—	5.0	6.0	Vdc
(I_{EC} = 0.3 Adc, T_C = 125°C)			—	5.2	—	
(I_{EC} = 0.1 Adc)			—	2.3	3.0	
(I_{EC} = 0.1 Adc, T_C = 125°C)			—	2.3	—	
Reverse Recovery Time	(I_F = 0.4 Adc, V_R = 300 Vdc, dIF/dt = 10 A/μs)	t_{rr}	—	150	—	ns
Reverse Recovery Stored Charge		Q_{RR}	—	35	—	μC
SWITCHING CHARACTERISTICS(1)						
Turn–Off Delay Time	(V_{CC} = 300 Vdc, I_C = 0.4 Adc, V_{GE} = 15 Vdc, L = 3.0 mH, R_G = 25 Ω, T_C = 25°C, dV/dt = 1000 V/μs) Energy losses include "tail"	$t_{d(off)}$	—	28	—	ns
Fall Time		t_f	—	150	—	
Turn–Off Switching Loss		E_{off}	—	3.25	—	μJ
Turn–Off Delay Time	(V_{CC} = 300 Vdc, I_C = 0.4 Adc, V_{GE} = 15 Vdc, L = 3.0 mH, R_G = 25 Ω, T_C = 125°C, dV/dt = 1000 V/μs) Energy losses include "tail"	$t_{d(off)}$	—	21	—	ns
Fall Time		t_f	—	280	—	
Turn–Off Switching Loss		E_{off}	—	8.0	—	μJ
Gate Charge	(V_{CC} = 300 Vdc, I_C = 0.3 Adc, V_{GE} = 15 Vdc)	Q_T	—	6.4	—	nC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

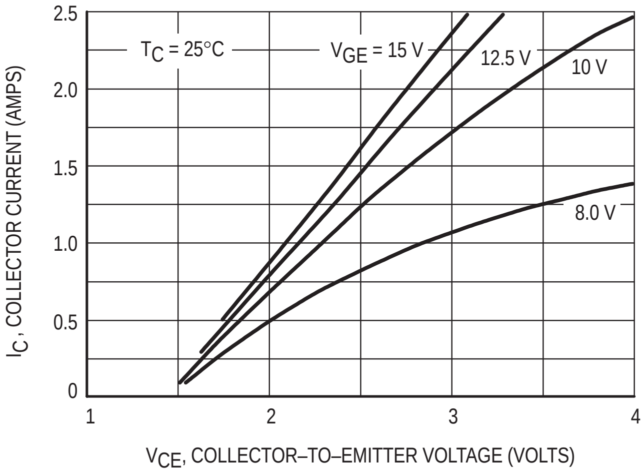


Figure 1. Saturation Characteristics

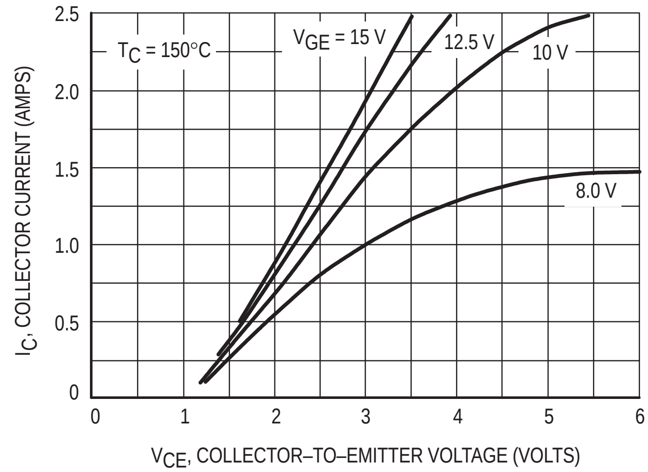


Figure 2. Saturation Characteristics

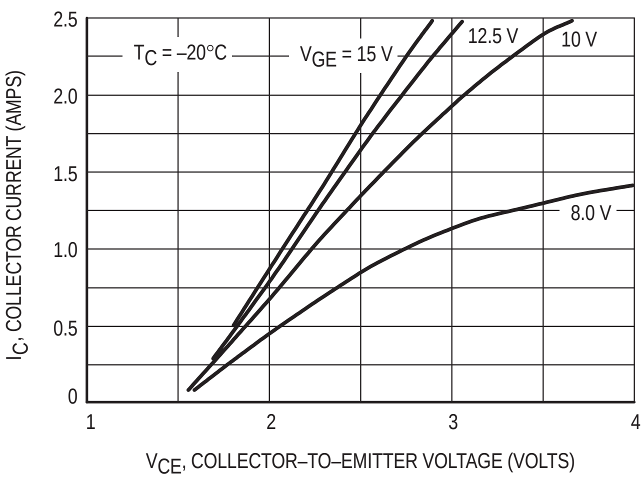


Figure 3. Saturation Characteristics

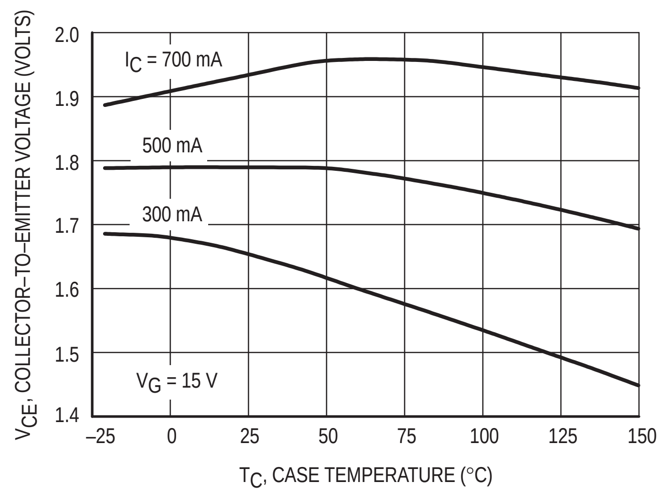


Figure 4. Collector–To–Emitter Saturation Voltage versus Case Temperature

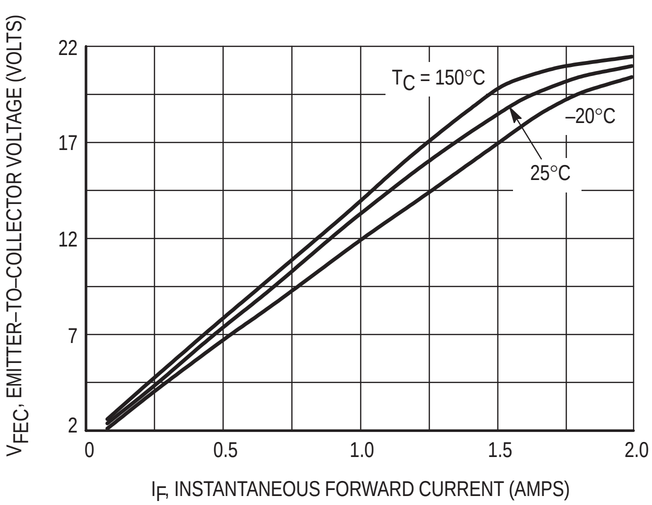


Figure 5. Diode Forward Voltage Drop

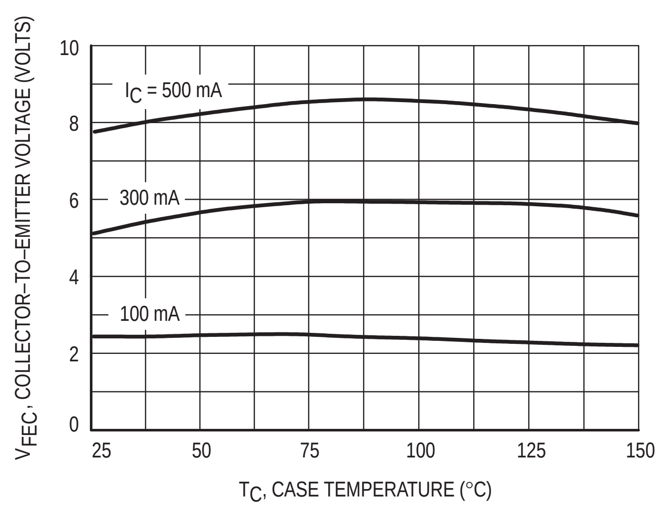


Figure 6. Diode Forward Voltage versus Case Temperature

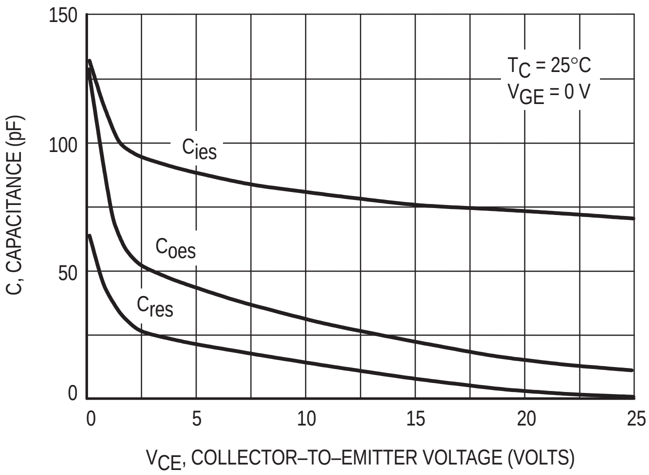


Figure 7. Capacitance Variation

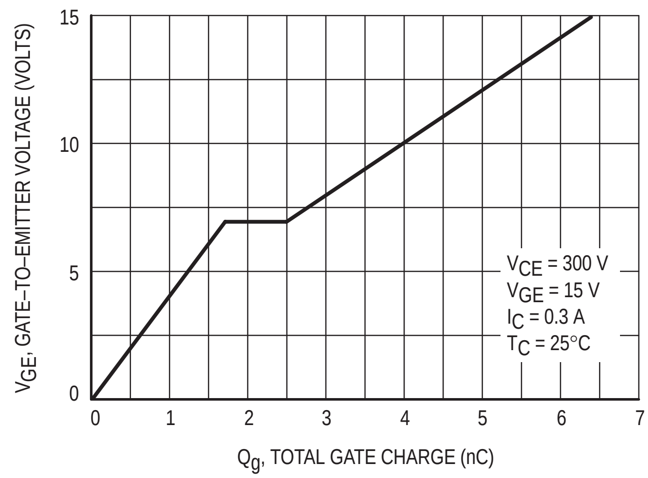


Figure 8. Gate–To–Emitter Voltage versus Total Charge

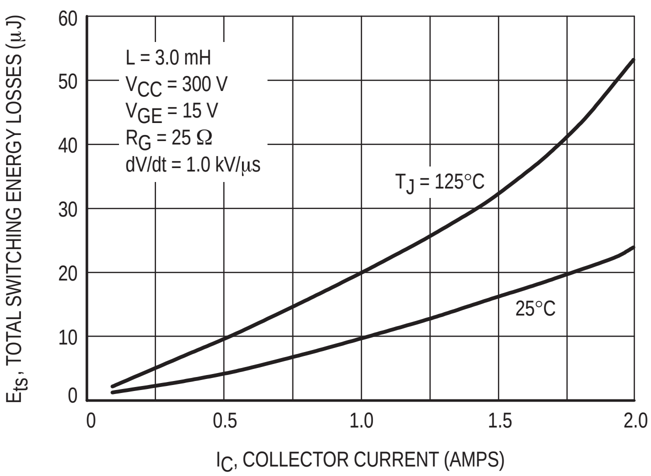


Figure 9. Total Switching Losses versus Collector Current

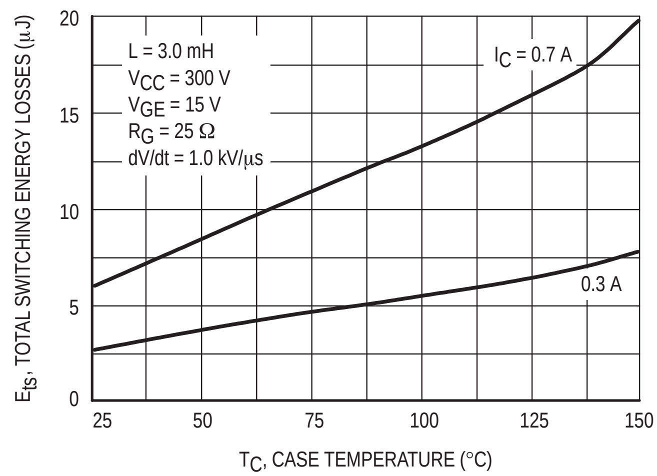


Figure 10. Total Switching Losses versus Case Temperature

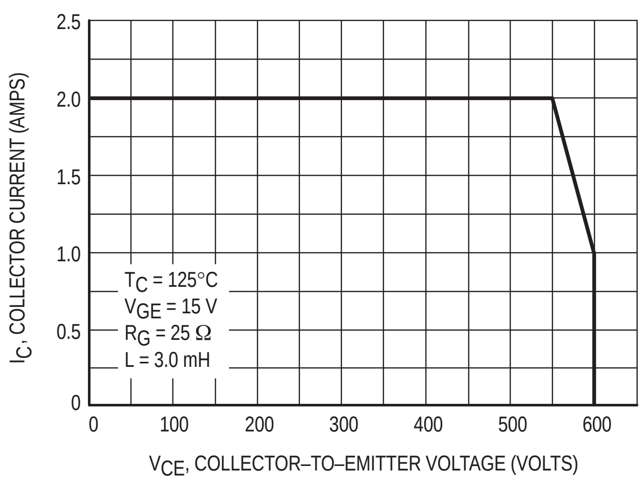


Figure 11. Minimum Turn–Off Safe Operating Area

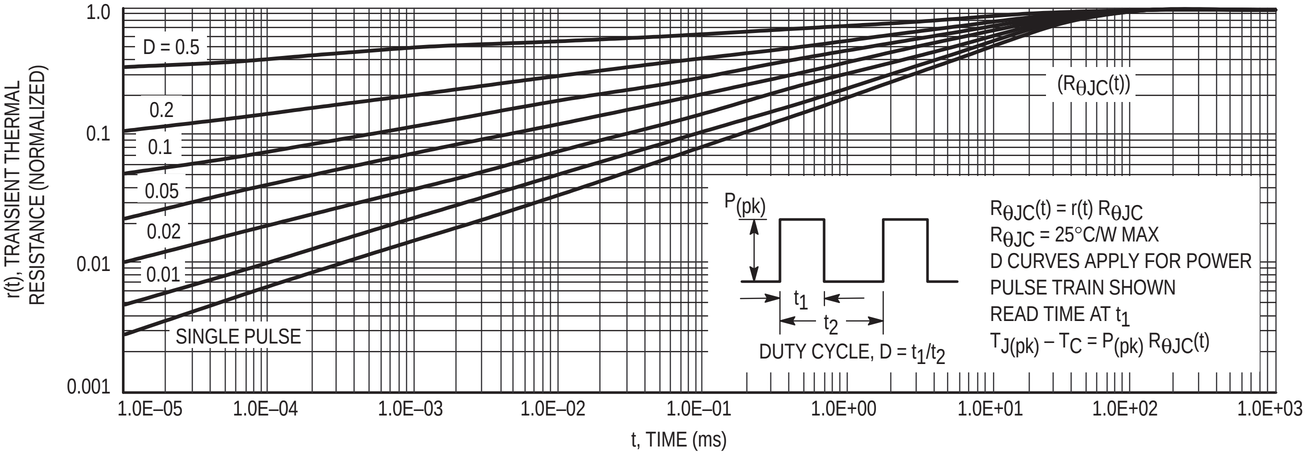


Figure 12. Typical Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

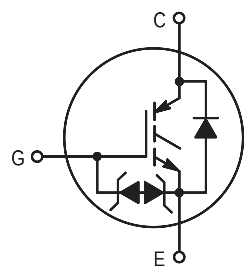
N–Channel Enhancement–Mode Silicon Gate

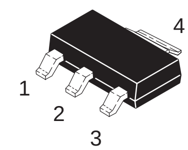
MMG05N60D

POWERLUX
IGBT
0.5 A @ 25°C
600 V

This IGBT contains a built–in free wheeling diode and a gate protection zener diodes. Fast switching characteristics result in efficient operation at higher frequencies. This device is ideally suited for high frequency electronic ballasts.

- Built–In Free Wheeling Diode
- Built–In Gate Protection Zener Diodes
- Industry Standard Package (SOT223)
- High Speed E_{off}: Typical 6.5 μJ @ I_C = 0.3 A; T_C = 125°C and dV/dt = 1000 V/μs
- Robust High Voltage Termination
- Robust Turn–Off SOA





1 = G
2 = 4 = C
3 = E

CASE 318E–04
STYLE 13
TO–261A

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameters	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{CGR}	±15	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	0.5 0.3 2.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	1.0	Watt
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	30 150	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_C ≤ 150°C)

Single Pulse Drain–to–Source Avalanche Energy – Starting @ T_C = 25°C @ T_C = 125°C V_{CE} = 100 V, V_{GE} = 15 V, Peak I_L = 2.0 A, L = 3.0 mH, R_G = 25 Ω	E_{AS}	 125 40	mJ

(1) Pulse width is limited by maximum junction temperature repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		$V_{(BR)CES}$	600	680	—	Vdc
Temperature Coefficient (Positive)			—	0.7	—	V/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_C = 25°C)		I_{CES}	—	0.1	5.0	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_C = 125°C)		I_{CES}	—	5.0	50	
Gate–Body Leakage Current (V_{GE} = ±15 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	10	100	μAdc
ON CHARACTERISTICS						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 0.3 Adc, T_C = 25°C)		$V_{CE(on)}$	—	1.6	2.0	Vdc
(V_{GE} = 15 Vdc, I_C = 0.3 Adc, T_C = 125°C)			—	1.5	—	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 250 μAdc)		$V_{GE(th)}$	3.5	—	6.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 0.5 Adc)		g_{fe}	0.3	0.42	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 20 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	75	100	pF
Output Capacitance		C_{oes}	—	11	20	
Transfer Capacitance		C_{res}	—	1.6	5.0	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 0.3 Adc, T_C = 25°C)		V_{FEC}	—	5.0	6.0	Vdc
(I_{EC} = 0.3 Adc, T_C = 125°C)			—	5.2	—	
(I_{EC} = 0.1 Adc, T_C = 25°C)			—	2.3	3.0	
(I_{EC} = 0.1 Adc, T_C = 125°C)			—	2.3	—	
Reverse Recovery Time @ T_C = 25°C I_F = 0.4 Adc, V_R = 300 Vdc, dIF/dt = 10 A/μs		t_{rr}	—	150	—	ns
Reverse Recovery Stored Charge I_F = 0.4 Adc, V_R = 300 Vdc, dIF/dt = 10 A/μs		Q_{RR}	—	35	—	μC
SWITCHING CHARACTERISTICS (1)						
Turn–Off Delay Time	(V_{CC} = 300 Vdc, I_C = 0.4 Adc, V_{GE} = 15 Vdc, L = 3.0 mH, R_G = 25 Ω, T_C = 25°C, dV/dt = 1000 V/μs) Energy losses include “tail”	$t_{d(off)}$	—	28	—	ns
Fall Time		t_f	—	150	—	
Turn–Off Switching Loss		E_{off}	—	3.25	4.25	μJ
Turn–Off Delay Time	(V_{CC} = 300 Vdc, I_C = 0.4 Adc, V_{GE} = 15 Vdc, L = 3.0 mH, R_G = 25 Ω, T_C = 125°C, dV/dt = 1000 V/μs) Energy losses include “tail”	$t_{d(off)}$	—	21	—	ns
Fall Time		t_f	—	280	—	
Turn–Off Switching Loss		E_{off}	—	8.0	10	μJ
Gate Charge	(V_{CC} = 300 Vdc, I_C = 0.3 Adc, V_{GE} = 15 Vdc)	Q_T	—	6.4	—	nC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

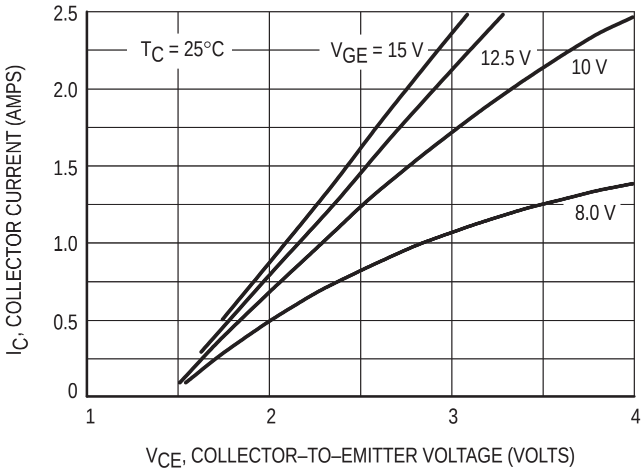


Figure 1. Saturation Characteristics

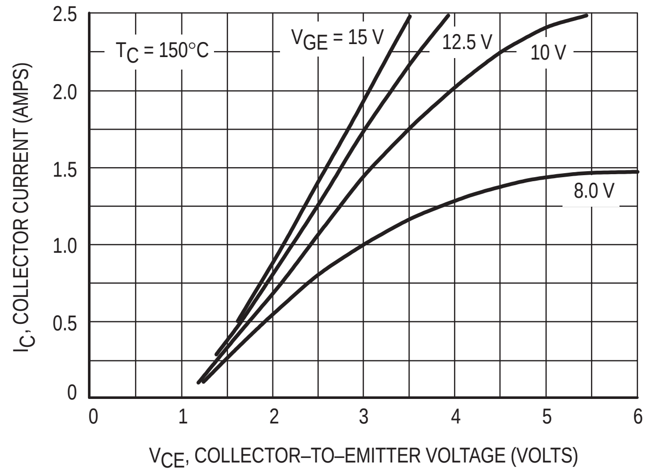


Figure 2. Saturation Characteristics

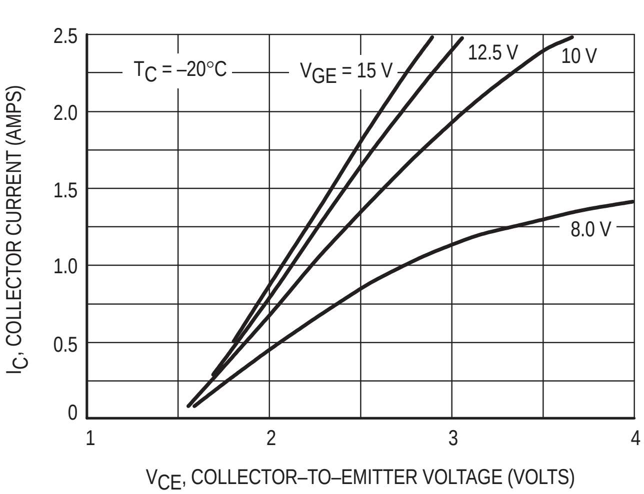


Figure 3. Saturation Characteristics

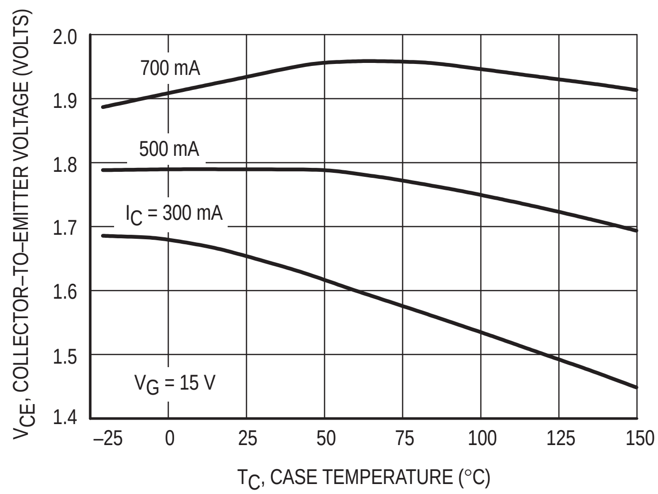


Figure 4. Collector–To–Emitter Saturation Voltage versus Case Temperature

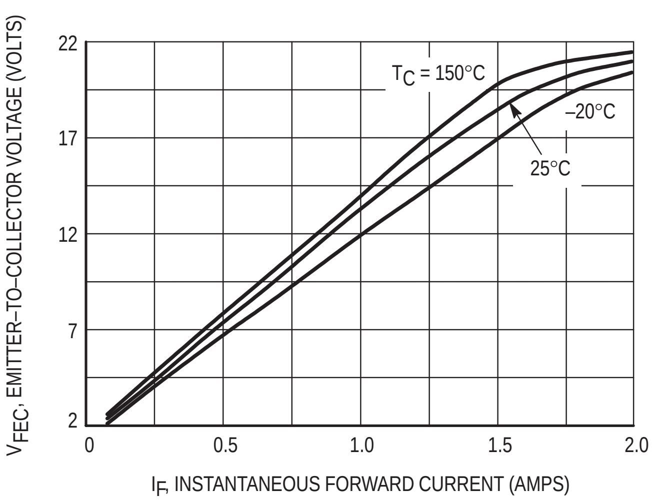


Figure 5. Diode Forward Voltage

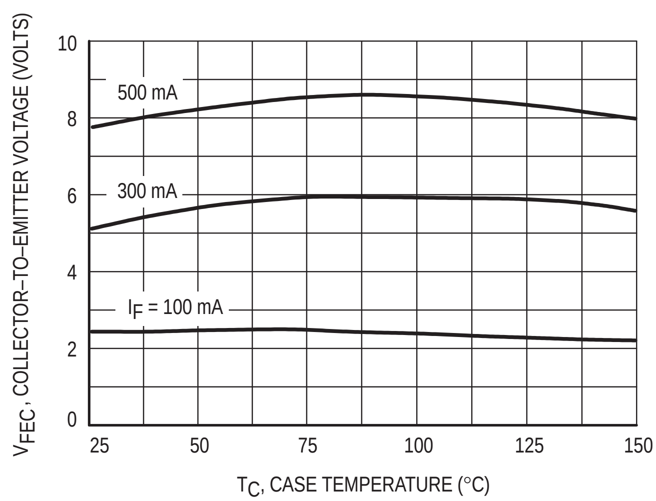


Figure 6. Diode Forward Voltage versus Case Temperature

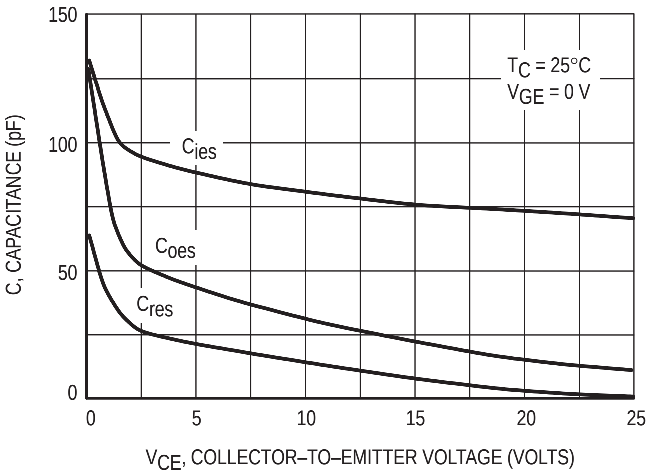


Figure 7. Capacitance Variation

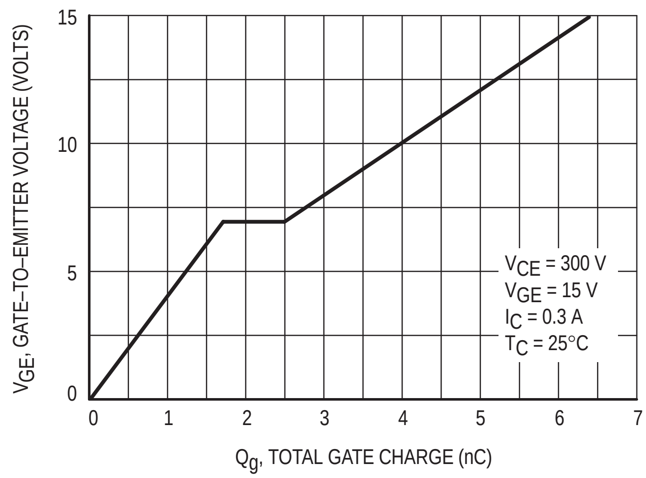


Figure 8. Gate–To–Emitter Voltage versus Total Charge

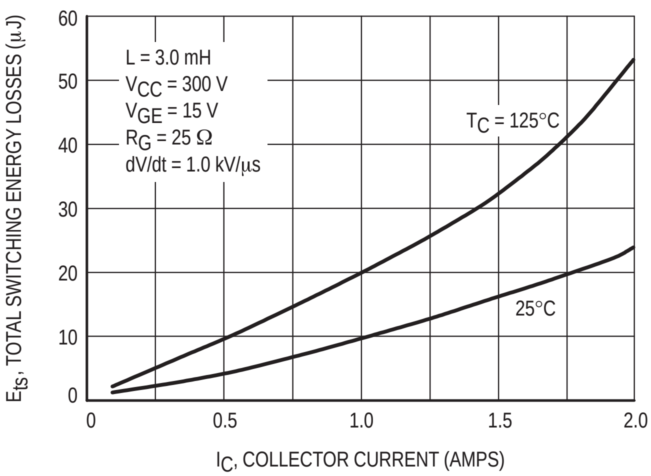


Figure 9. Total Switching Losses versus Collector Current

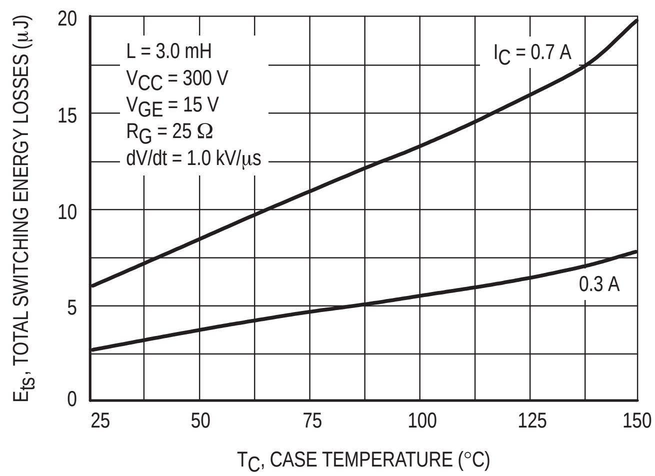


Figure 10. Total Switching Losses versus Case Temperature

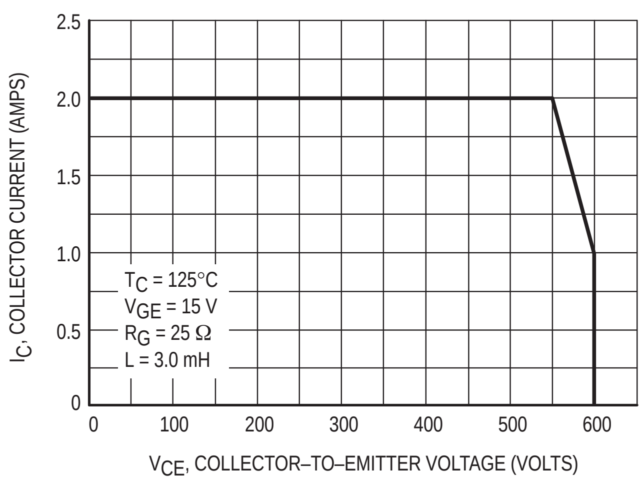


Figure 11. Minimum Turn–Off Safe Operating Area

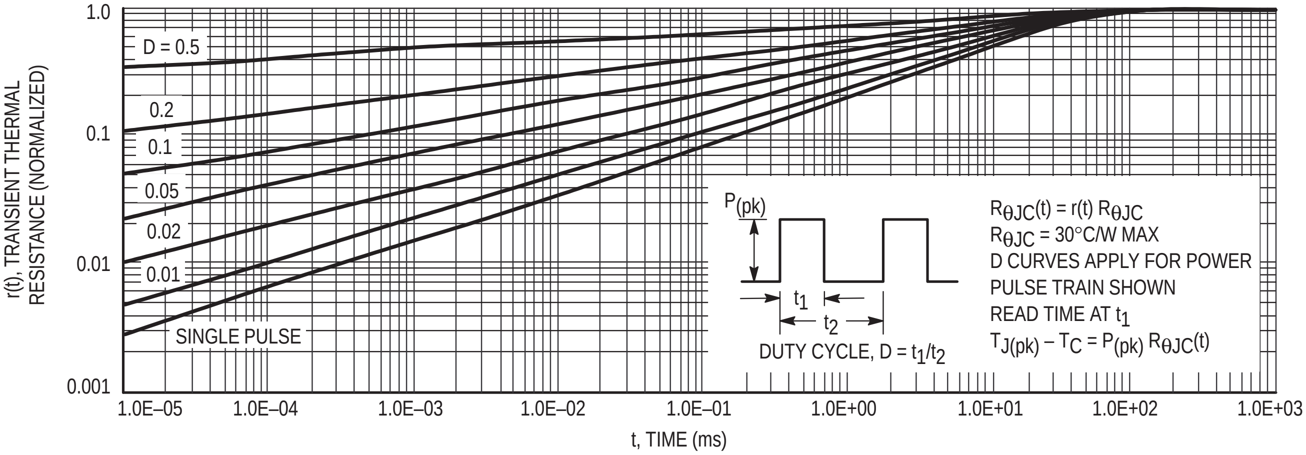


Figure 12. Typical Thermal Response

SWITCHMODE™ Soft Recovery Power Rectifier

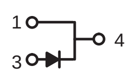
Plastic TO–220 Package

MSR860

**SOFT RECOVERY POWER RECTIFIER
8.0 AMPERES
600 VOLTS**

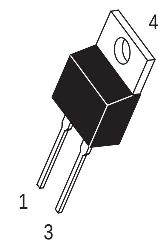
Designed for use as free wheeling diodes in variable speed motor control applications and switching power supplies. These state–of–the–art devices have the following features:

- Soft Recovery with Guaranteed Low Reverse Recovery Charge (Q_{RR}) and Peak Reverse Recovery Current (I_{RRM})
- 150°C Operating Junction Temperature
- Popular TO–220 Package
- Epoxy meets UL94, V_O @ 1/8″
- Low Forward Voltage
- Low Leakage Current
- High Temperature Glass Passivated Junction



Mechanical Characteristics:

- Case: Molded Epoxy
- Weight: 1.9 Grams (approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Shipped in 50 Units per Plastic Tube
- Marking: MSR860



**CASE 221B–04
STYLE 1
TO–220**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	600	V
Average Rectified Forward Current (At Rated V_R, T_C = 125°C)	I_O	8.0	A
Peak Repetitive Forward Current (At Rated V_R, Square Wave, 20 kHz, T_C = 125°C)	I_{FRM}	16	A
Non–Repetitive Peak Surge Current (Surge applied at rated load conditions, halfwave, single phase, 60 Hz)	I_{FSM}	100	A
Storage / Operating Case Temperature	T_{stg}, T_C	– 65 to 150	°C
Operating Junction Temperature	T_J	– 65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Case Thermal Resistance — Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.6 72.8	°C/W

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (1) (I_F = 8.0 A)	V_F	**T_J = 25°C**	**T_J = 150°C**	V
		1.7	1.3	
Typical		*1.4*	*1.1*	
Maximum Instantaneous Reverse Current (V_R = 600 V)	I_R	**T_J = 25°C**	**T_J = 150°C**	μA
		10	1000	
Typical		*2.0*	*80*	
Maximum Reverse Recovery Time (2) (V_R = 400 V, I_F = 8.0 A, di/dt = 200 A/μs)	t_{rr}	**T_J = 25°C**	**T_J = 125°C**	ns
		120	190	
Typical		*95*	*125*	
Typical Recovery Softness Factor (V_R = 400 V, I_F = 8.0 A, di/dt = 200 A/μs)	$s = t_b/t_a$	*2.5*	*3.0*	
Maximum Peak Reverse Recovery Current (V_R = 400 V, I_F = 8.0 A, di/dt = 200 A/μs)	I_{RRM}	5.8	8.3	A
Maximum Reverse Recovery Charge (V_R = 400 V, I_F = 8.0 A, di/dt = 200 A/μs)	Q_{RR}	350	700	nC

(1) Pulse Test: Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%
(2) T_{RR} measured projecting from 25% of I_{RRM} to zero current

REV 1

TYPICAL ELECTRICAL CHARACTERISTICS

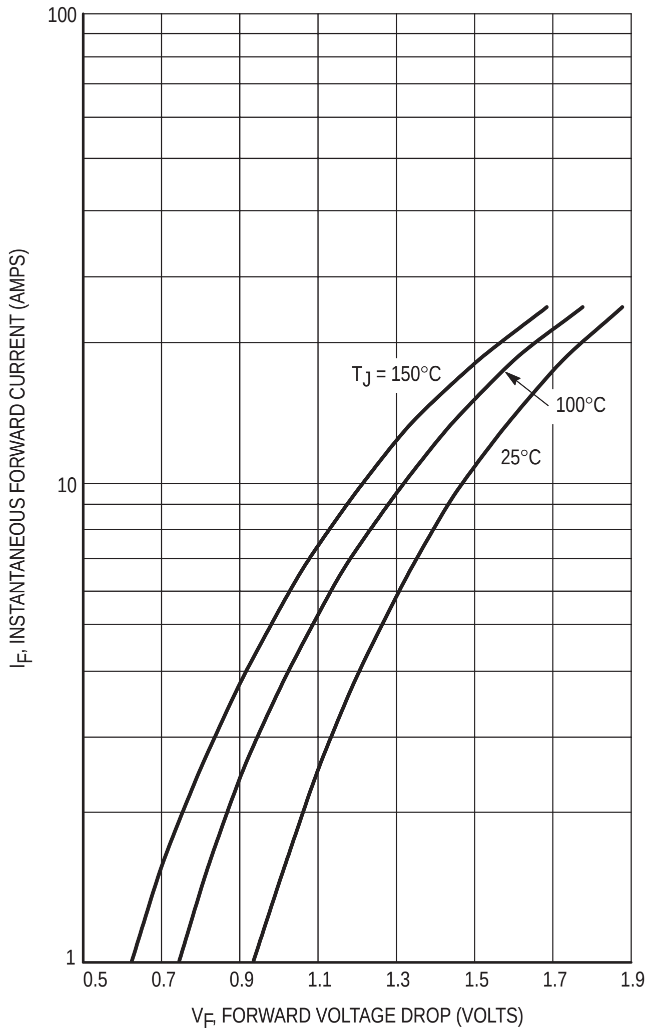


Figure 1. Typical Forward Voltage

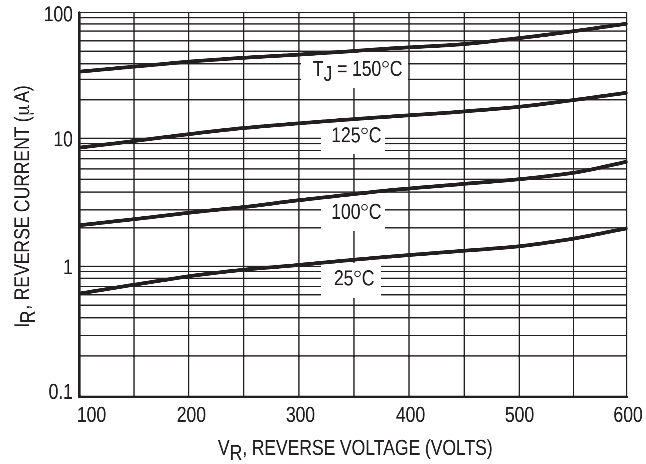


Figure 2. Typical Reverse Current

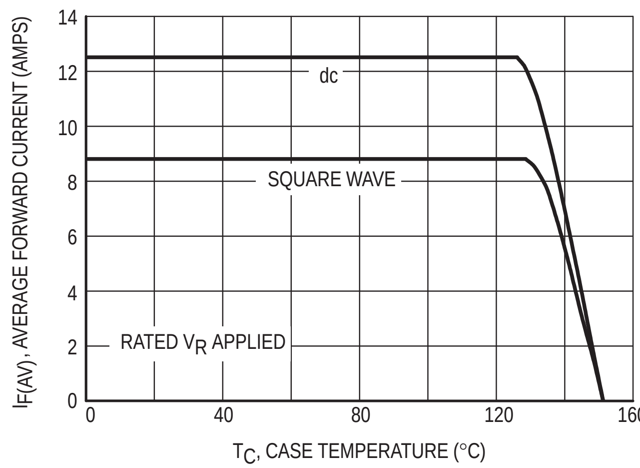


Figure 3. Current Derating, Case

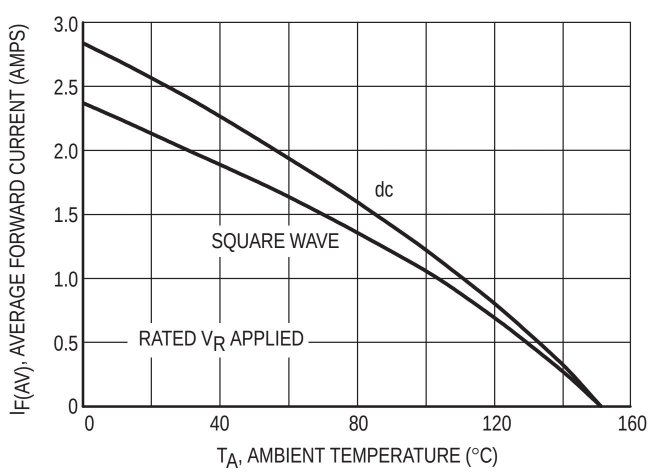


Figure 4. Current Derating, Ambient

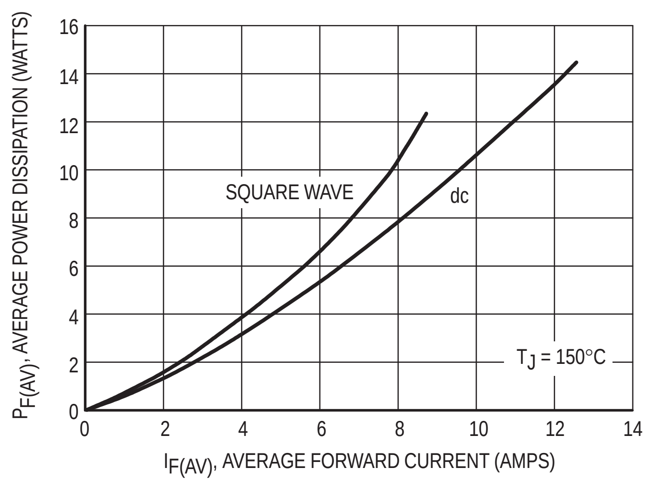


Figure 5. Power Dissipation

TYPICAL ELECTRICAL CHARACTERISTICS

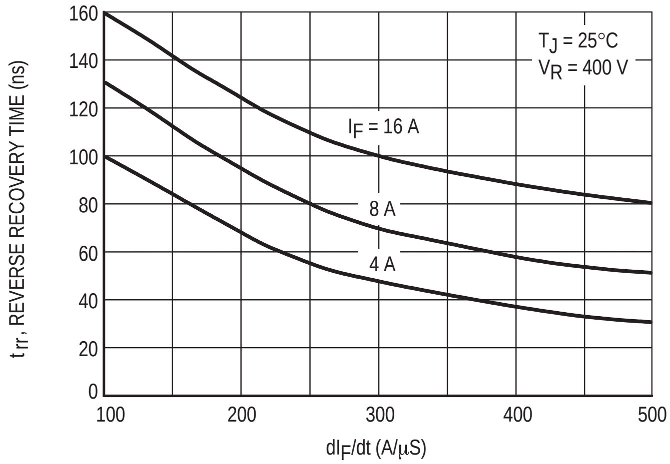


Figure 6. Typical Reverse Recovery Time

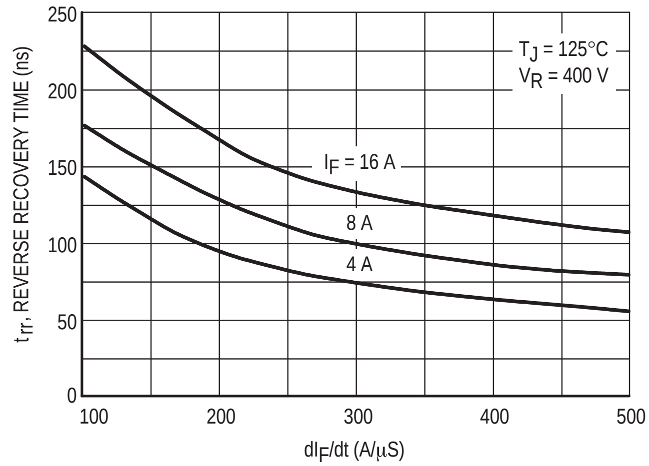


Figure 7. Typical Reverse Recovery Time

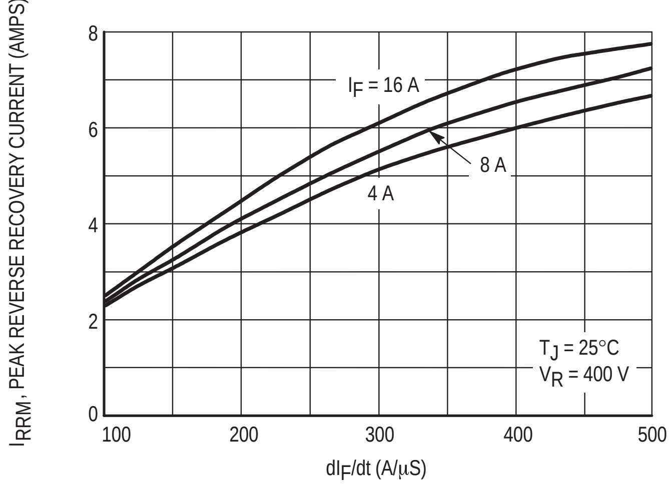


Figure 8. Typical Peak Reverse Recovery Current

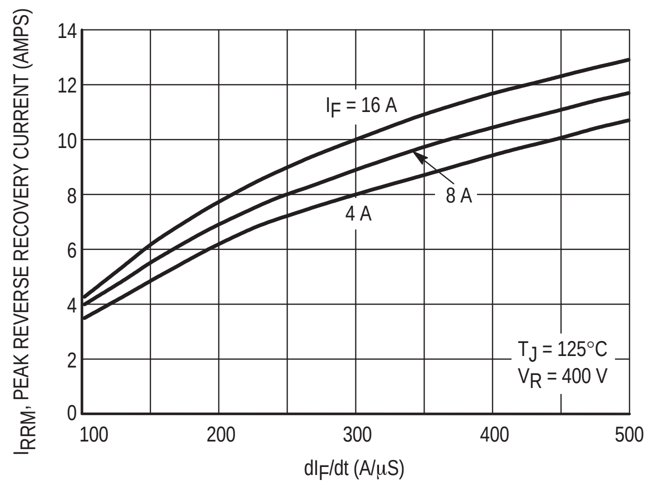


Figure 9. Typical Peak Reverse Recovery Current

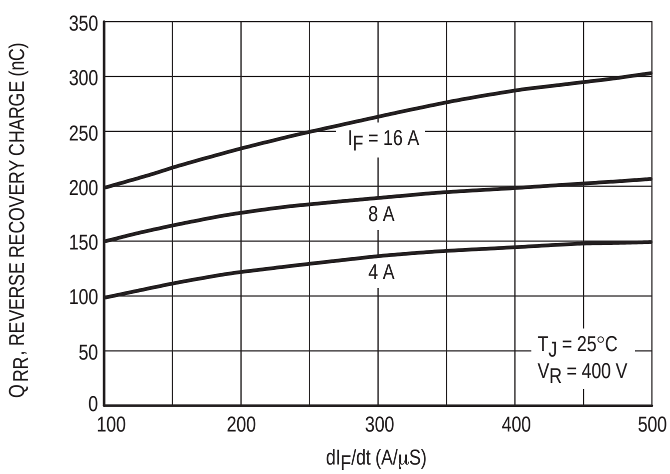


Figure 10. Typical Reverse Recovery Charge

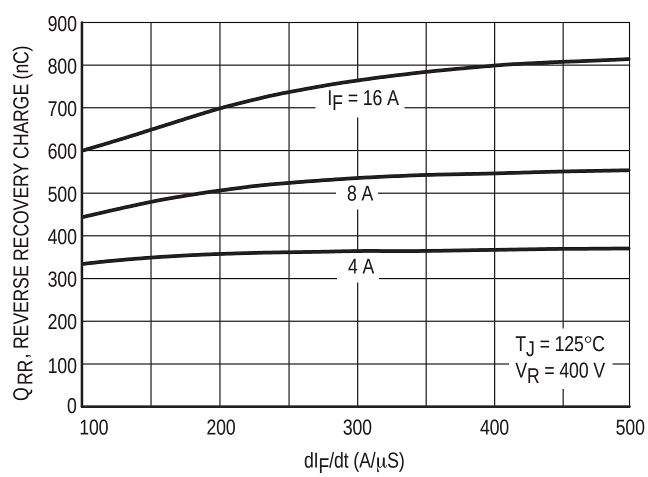


Figure 11. Typical Reverse Recovery Charge

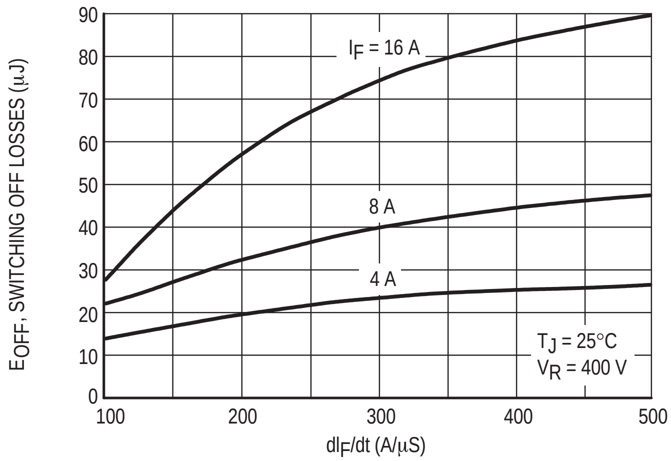


Figure 12. Typical Switching Off Losses

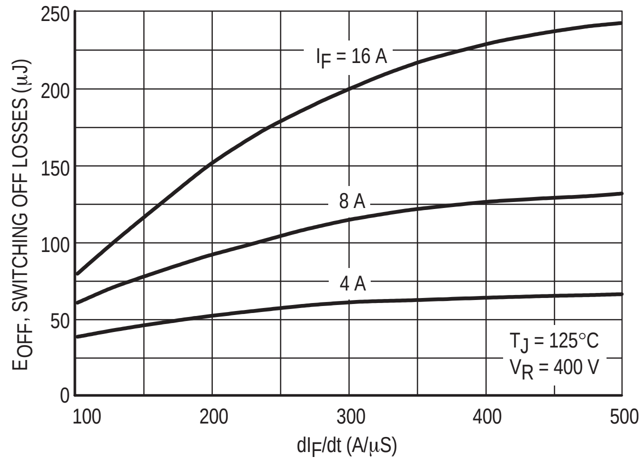


Figure 13. Typical Switching Off Losses

Advance Information

Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drive

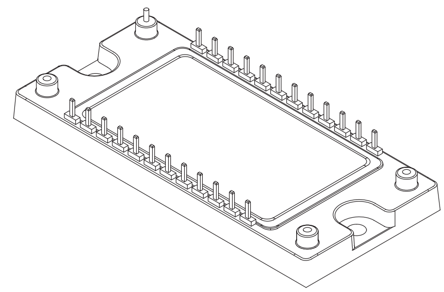
MHPM7A10E60DC3

Motorola Preferred Device

10 AMP, 600 VOLT HYBRID POWER MODULE

This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 1.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) with integrated ESD protection Gate–Emitter zener diodes and ultrafast soft (UFS) free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 400 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/



CASE 464D–01
ISSUE O

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A10E60DC3	600	10	1.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 150°C)	V_{RRM}	900	V
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 80°C)	I_{Cmax}	10	A
Repetitive Peak IGBT Collector Current (1)	$I_{C(pk)}$	20	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	10	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	6.8	A
Repetitive Peak Free–Wheeling Diode Current (1)	$I_{F(pk)}$	20	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	20	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	17	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	9.0	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 400 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 10 A)	V_F	—	0.97	1.2	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±50	μA
Collector–Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	μA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	600	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.0	2.4	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)	V_F	1.7	2.0	2.3	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	—	1020	—	pF
Input Gate Charge (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V)	Q_T	—	57	—	nC
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	2.6	3.2	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	4.8	6.0	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	3.4	4.2	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

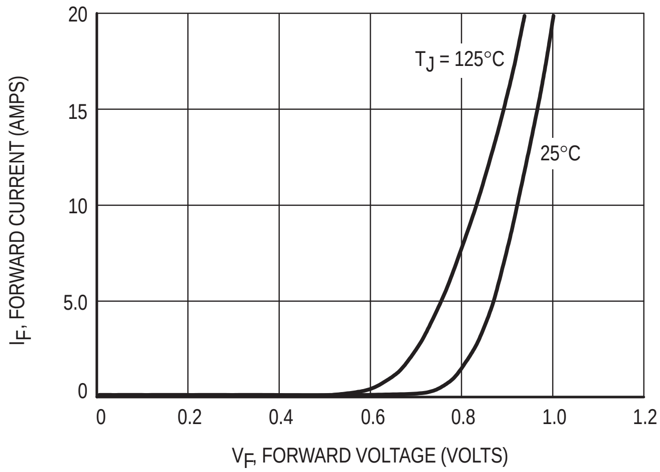


Figure 1. Forward Characteristics — Input Rectifier

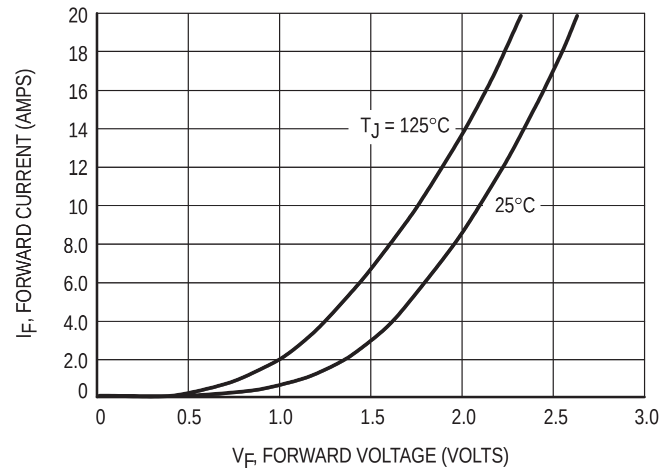


Figure 2. Forward Characteristics — Free–Wheeling Diode

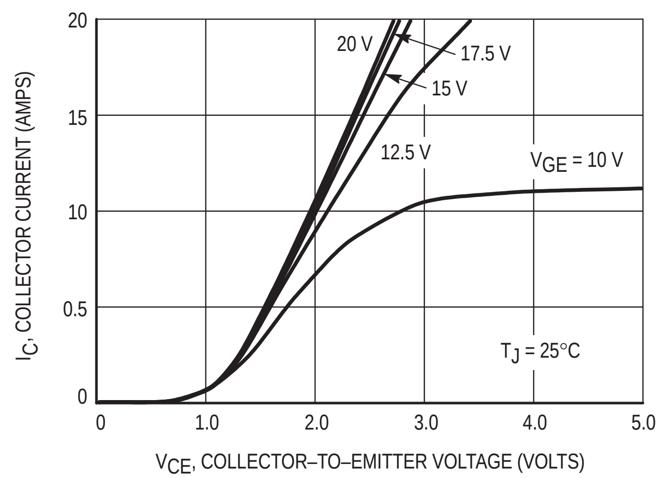


Figure 3. Forward Characteristics, T_J = 25°C

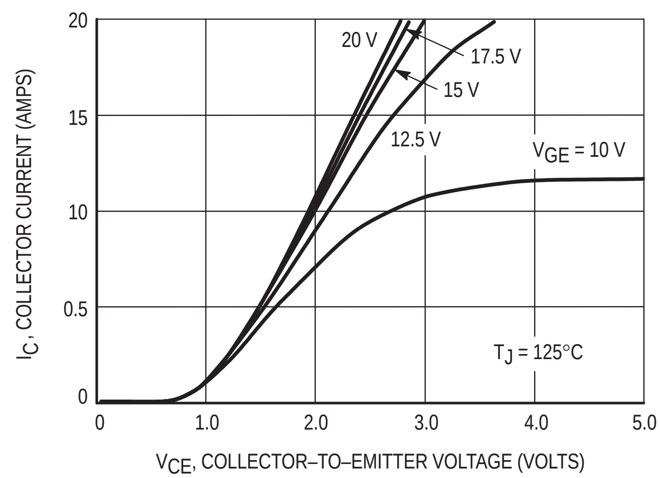


Figure 4. Forward Characteristics, T_J = 125°C

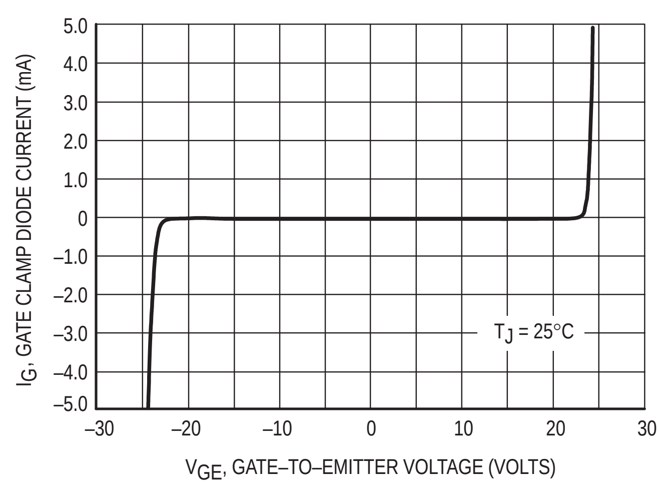


Figure 5. Gate–Emitter Zener Diode Clamp Characteristic

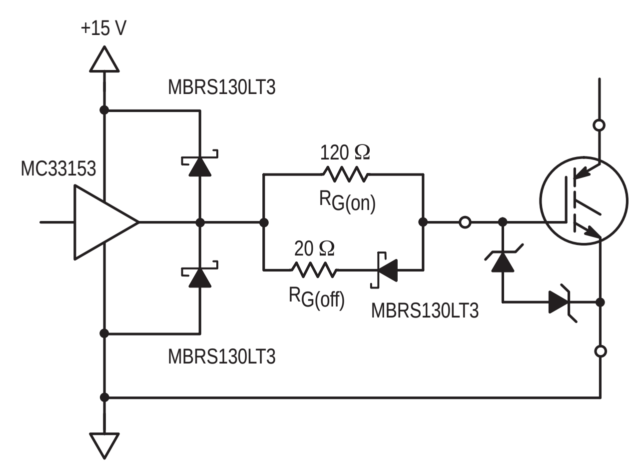


Figure 6. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

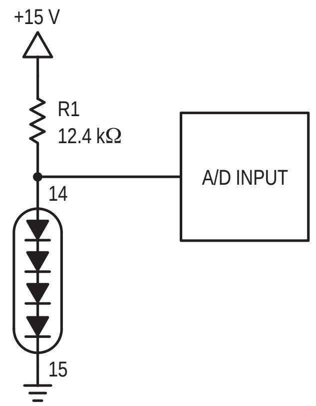


Figure 7. Recommended Temperature Sense Bias Circuit

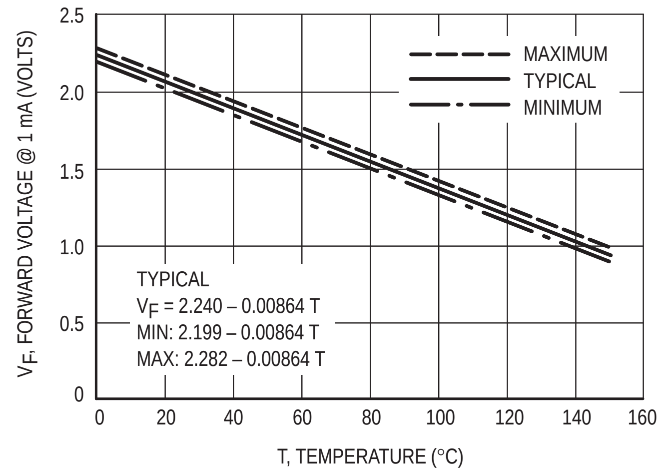


Figure 8. BAV99LT1 Temperature Sense Diode Performance: V_F = 2.59 – 7.31E–3 T_C

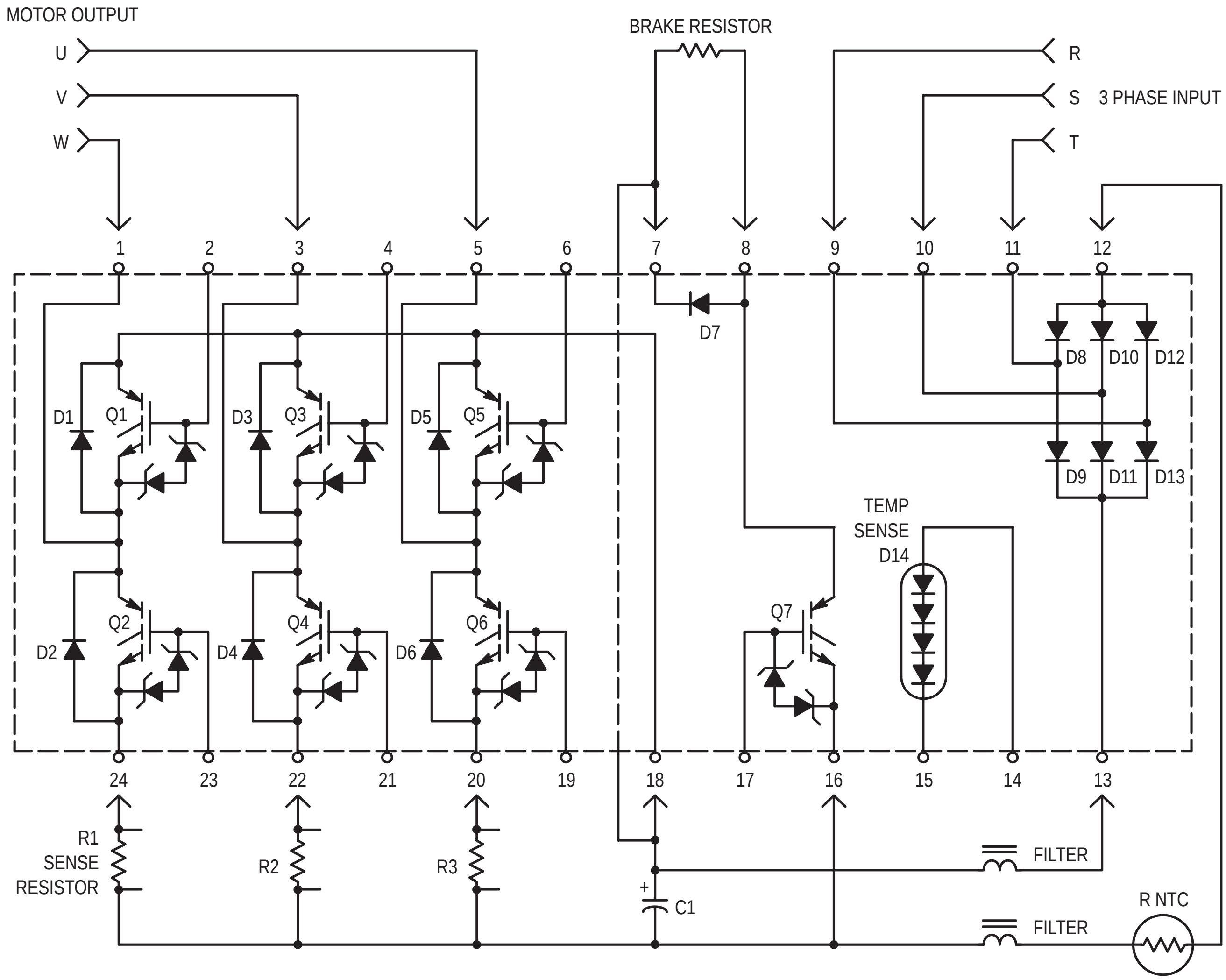
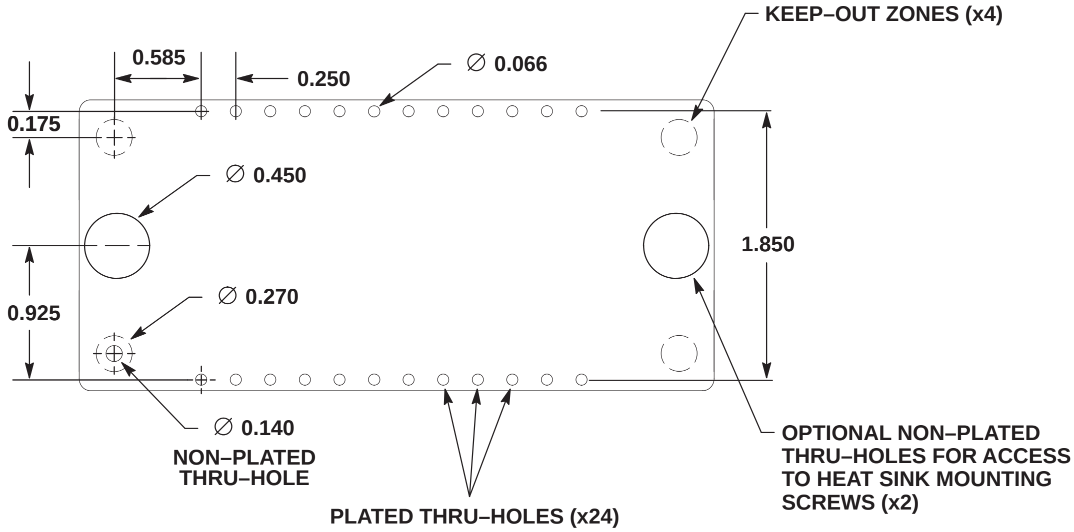


Figure 9. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 10. Package Footprint (Dimensions in Inches)

Advance Information

Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drive

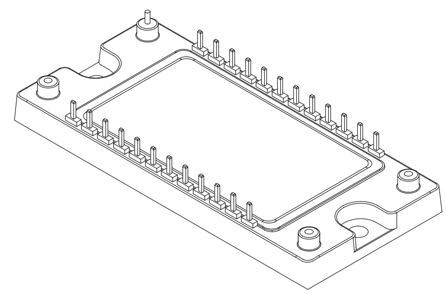
This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 2.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) with integrated ESD protection Gate–Emitter zener diodes and ultrafast soft (UFS) free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 400 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/

MHPM7A20E60DC3

Motorola Preferred Device

20 AMP, 600 VOLT
HYBRID POWER MODULE



CASE 464D–01
ISSUE O

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A20E60DC3	600	20	2.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 150°C)	V_{RRM}	900	V
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	20	A
Continuous IGBT Collector Current (T_C = 80°C)	I_{C80}	15.8	A
Repetitive Peak IGBT Collector Current (1)	$I_{C(pk)}$	40	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	20	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	14.1	A
Repetitive Peak Free–Wheeling Diode Current (1)	$I_{F(pk)}$	40	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	20	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	25	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	17	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 400 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 20 A)	V_F	—	1.0	1.25	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±50	μA
Collector–Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	μA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	600	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.2	2.6	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)	V_F	1.6	2.0	2.3	V
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	1.8	2.2	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	2.6	3.3	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	3.4	4.2	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

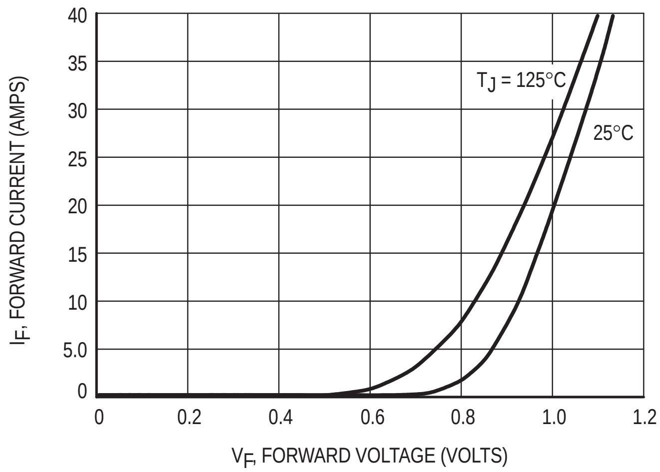


Figure 1. Forward Characteristics — Input Rectifier

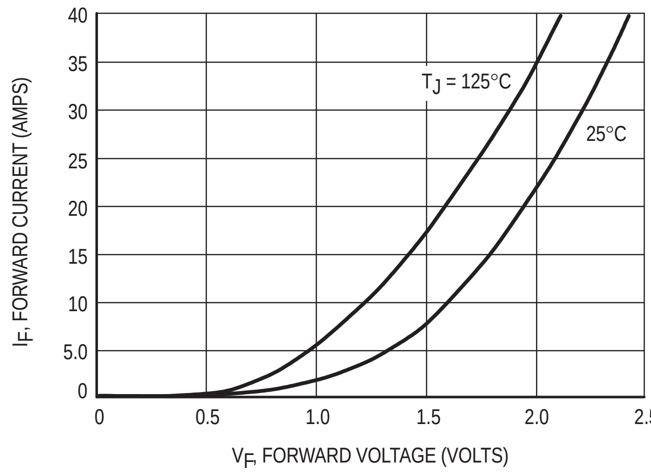


Figure 2. Forward Characteristics — Free–Wheeling Diode

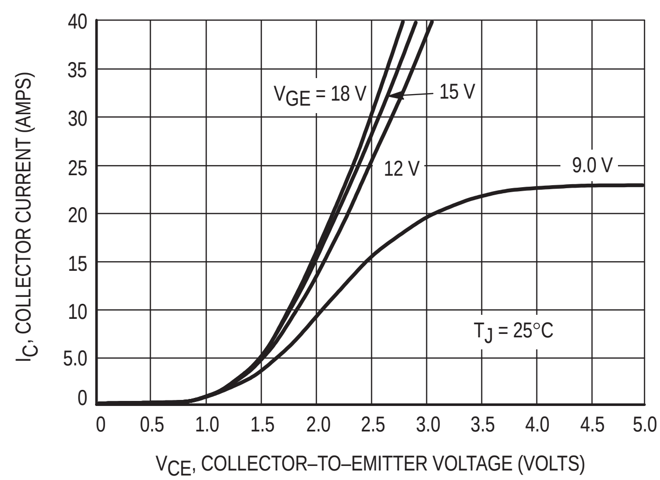


Figure 3. Forward Characteristics, T_J = 25°C

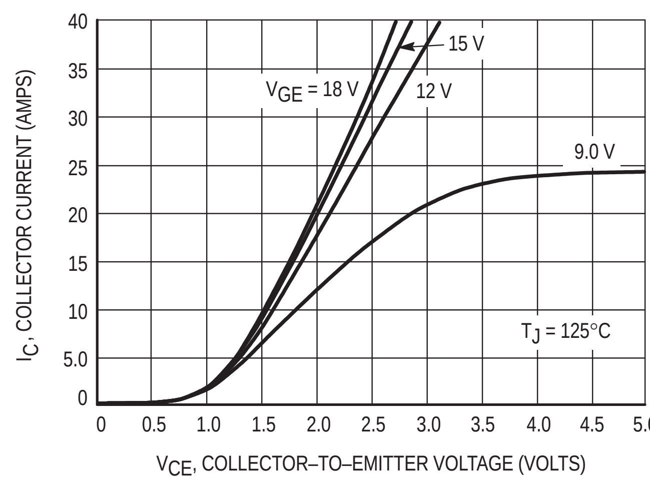


Figure 4. Forward Characteristics, T_J = 125°C

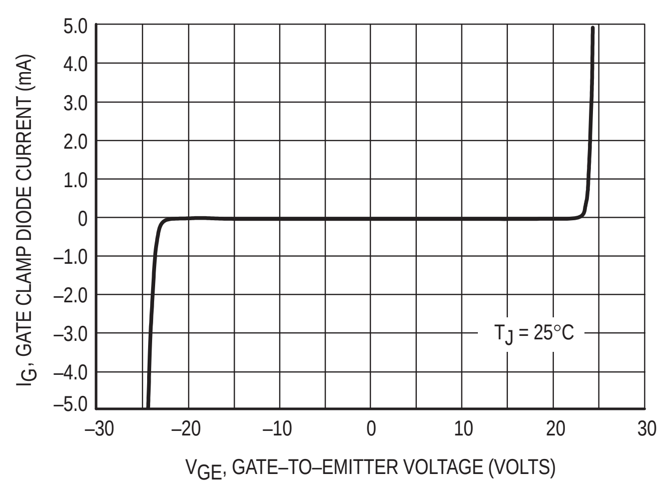


Figure 5. Gate–Emitter Zener Diode Clamp Characteristic

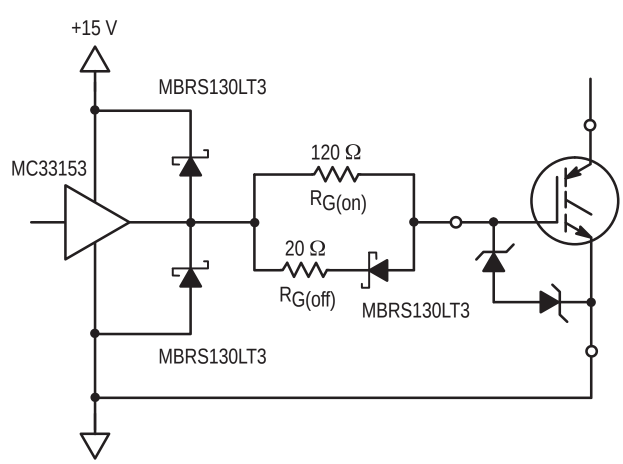


Figure 6. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

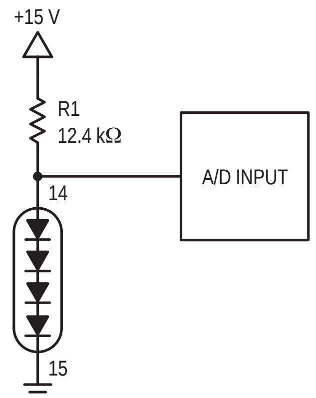


Figure 7. Recommended Temperature Sense Bias Circuit

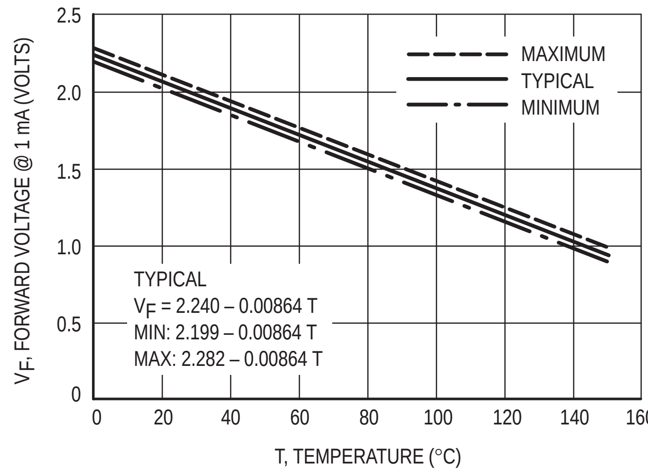


Figure 8. BAV99LT1 Temperature Sense Diode Performance: $V_F = 2.59 – 7.31E–3\ T_C$

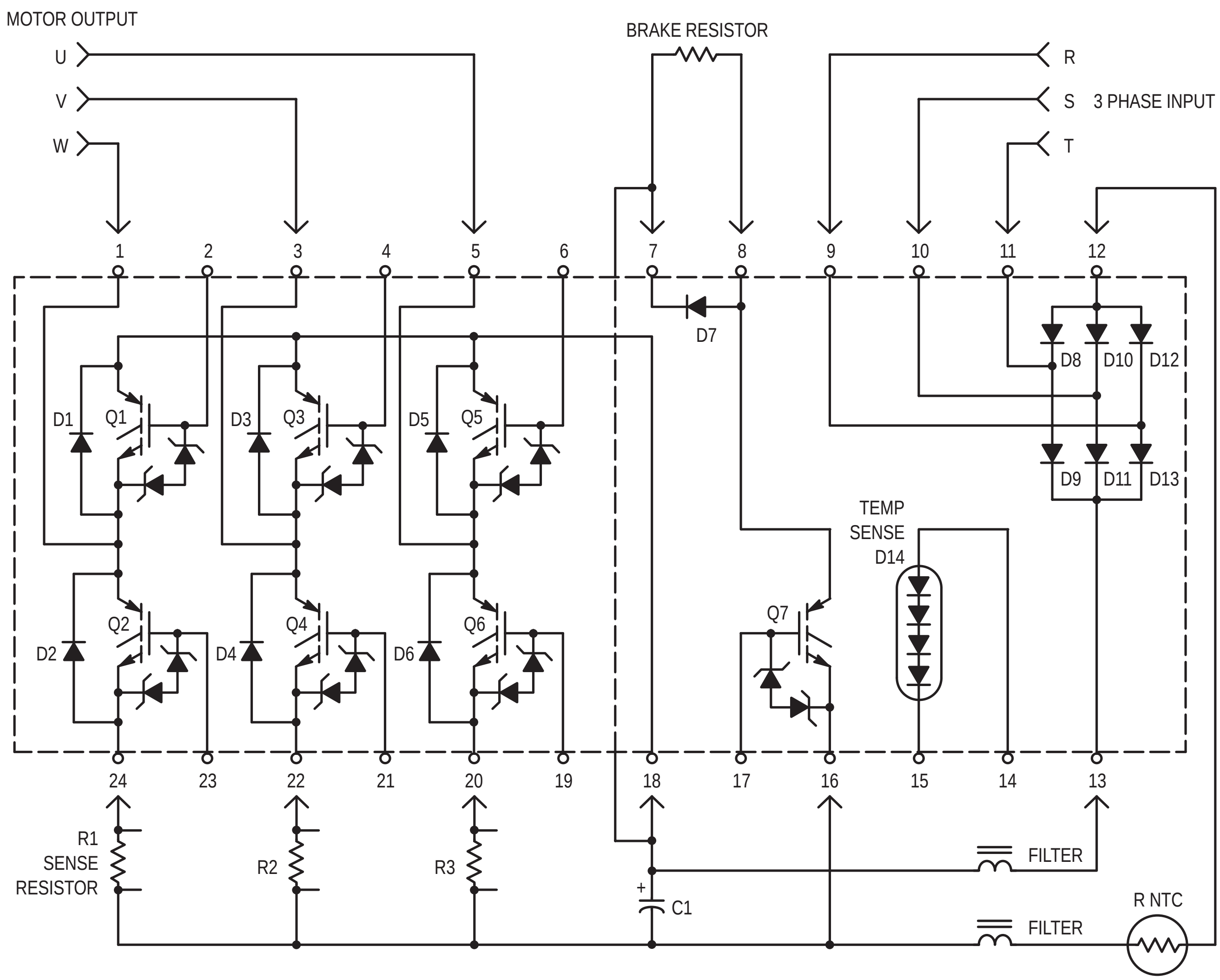
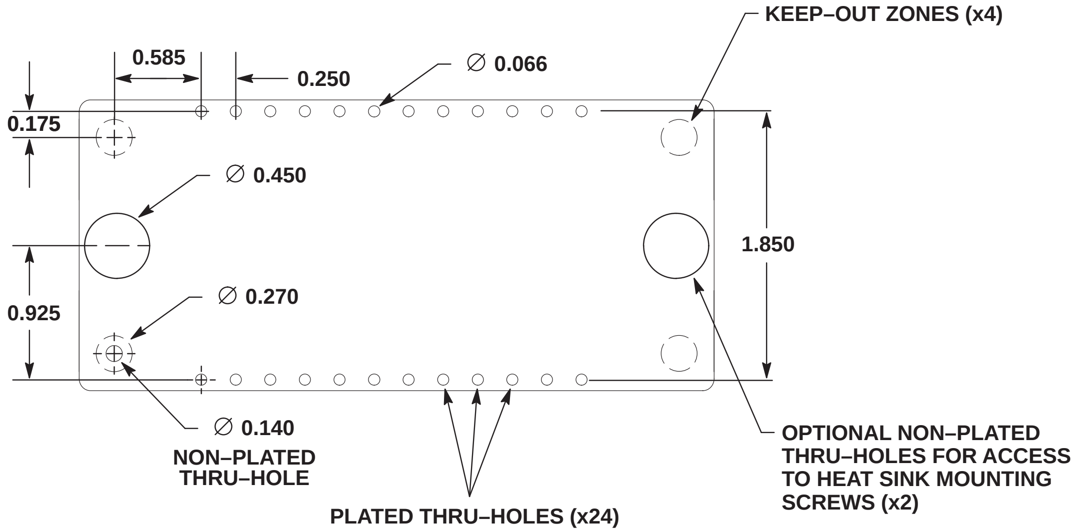


Figure 9. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 10. Package Footprint (Dimensions in Inches)

Advance Information

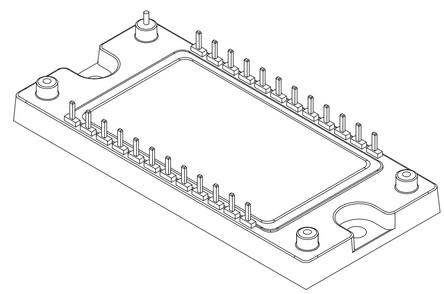
Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drive

MHPM7A30E60DC3

Motorola Preferred Device

30 AMP, 600 VOLT HYBRID POWER MODULE



CASE 464D–01
ISSUE O

This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 3.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) with integrated ESD protection Gate–Emitter zener diodes and ultrafast soft (UFS) free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 400 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A30E60DC3	600	30	3.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 150°C)	V_{RRM}	900	V
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	30	A
Continuous IGBT Collector Current (T_C = 80°C)	I_{C80}	21.8	A
Repetitive Peak IGBT Collector Current (1)	$I_{C(pk)}$	60	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	30	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	20	A
Repetitive Peak Free–Wheeling Diode Current (1)	$I_{F(pk)}$	60	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	27.6	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	34	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	23	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 400 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 30 A)	V_F	—	1.04	1.25	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±50	μA
Collector–Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	μA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	600	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.2	2.6	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)	V_F	1.6	1.8	2.1	V
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	1.3	1.6	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	1.9	2.4	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	2.6	3.3	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

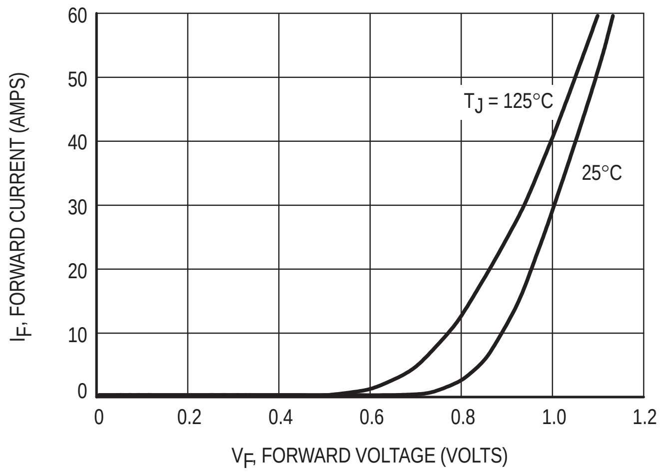


Figure 1. Forward Characteristics — Input Rectifier

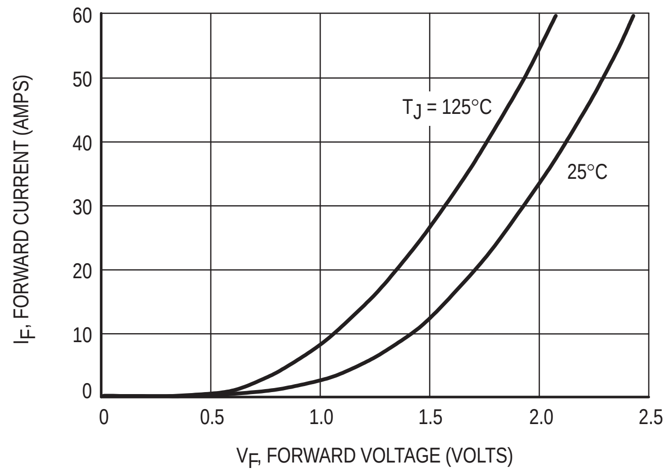


Figure 2. Forward Characteristics — Free–Wheeling Diode

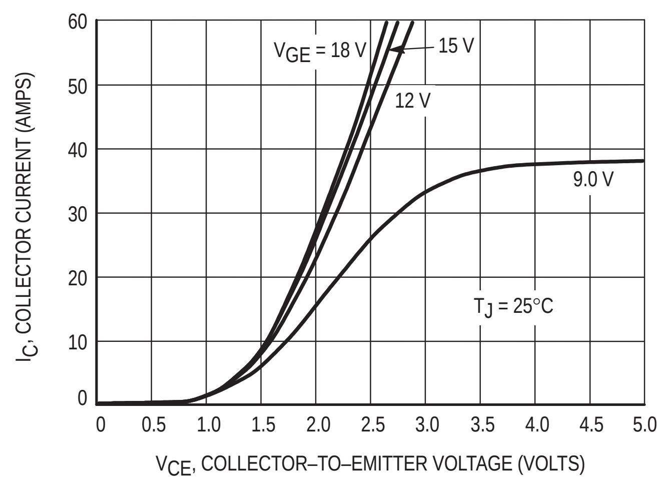


Figure 3. Forward Characteristics, T_J = 25°C

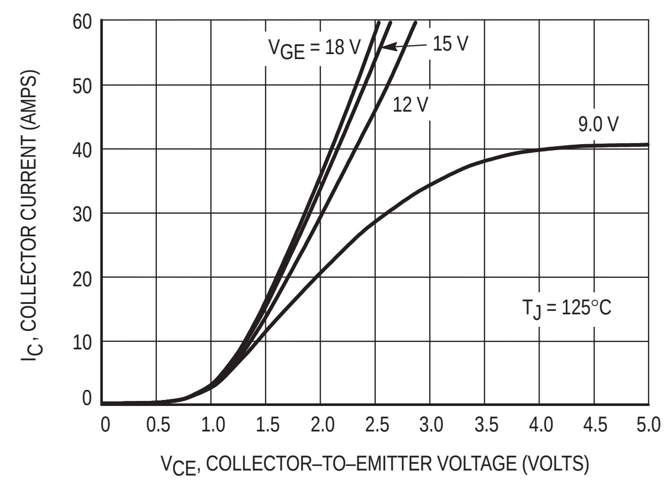


Figure 4. Forward Characteristics, T_J = 125°C

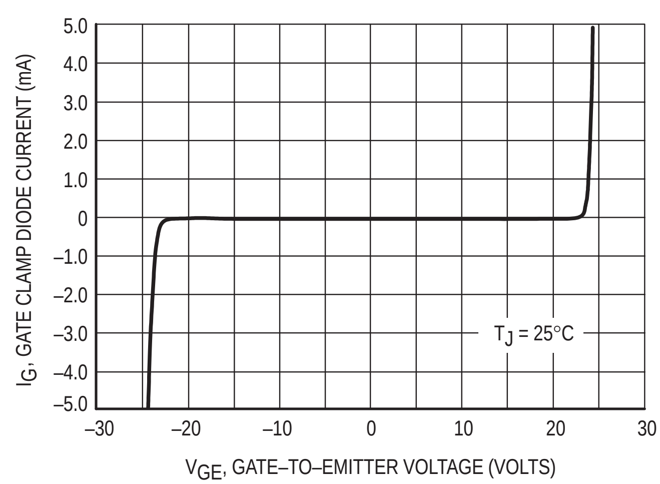


Figure 5. Gate–Emitter Zener Diode Clamp Characteristic

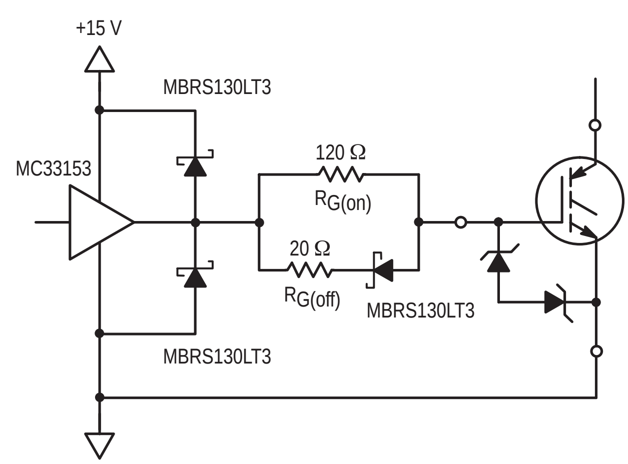


Figure 6. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

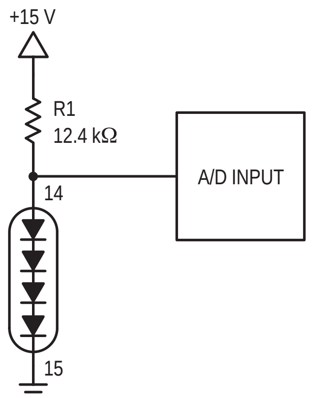


Figure 7. Recommended Temperature Sense Bias Circuit

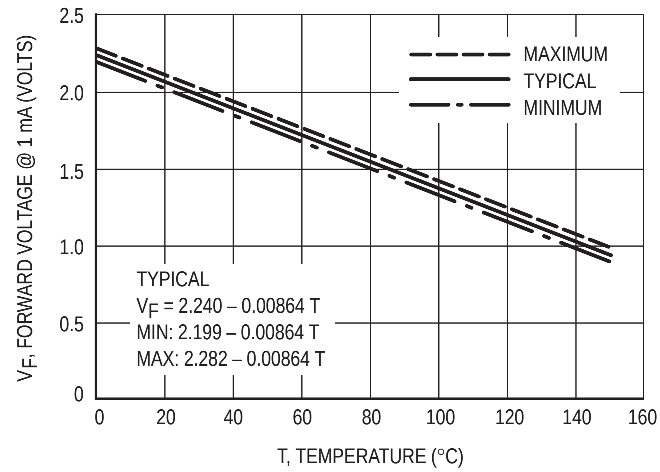


Figure 8. BAV99LT1 Temperature Sense Diode Performance: V_F = 2.59 – 7.31E–3 T_C

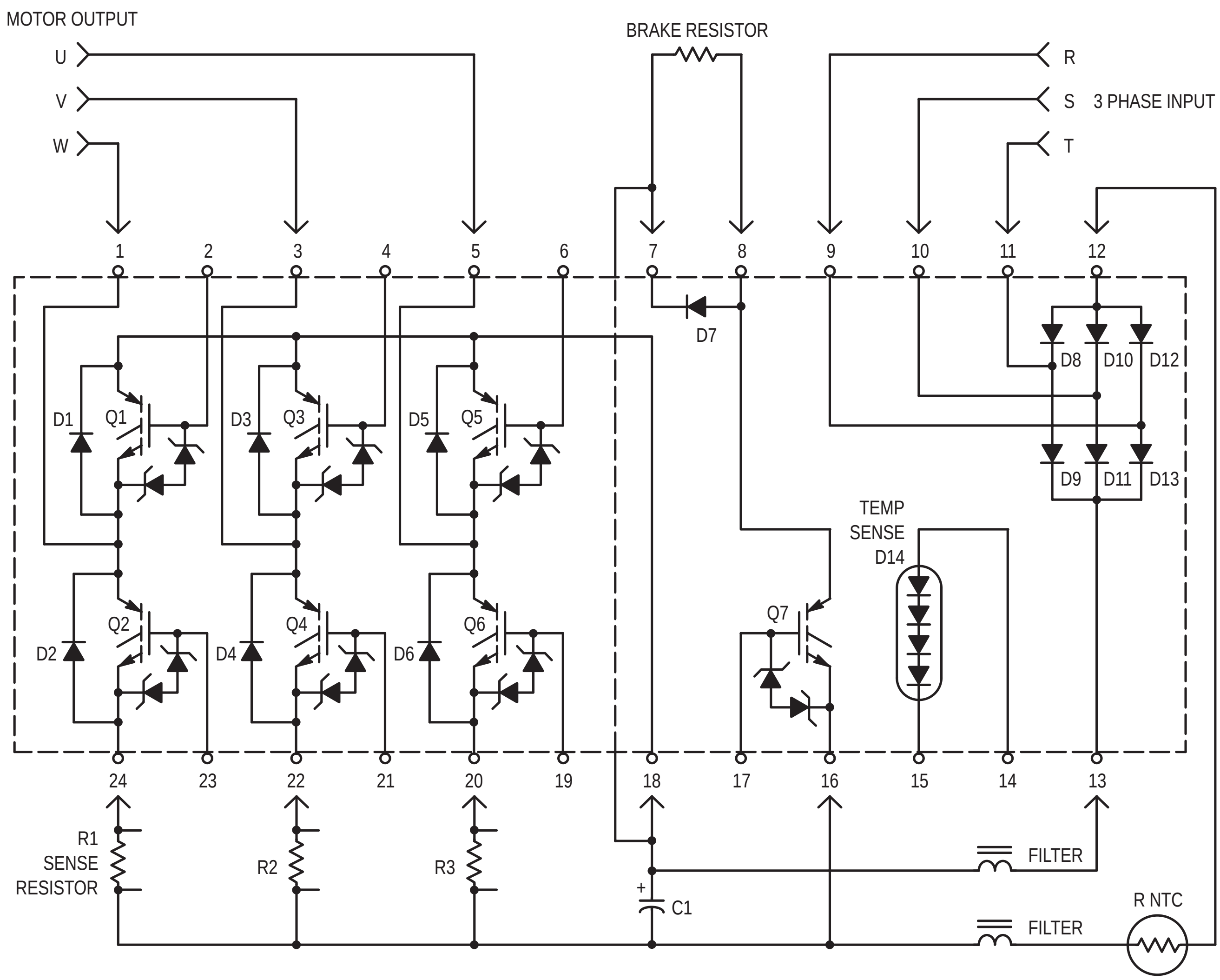
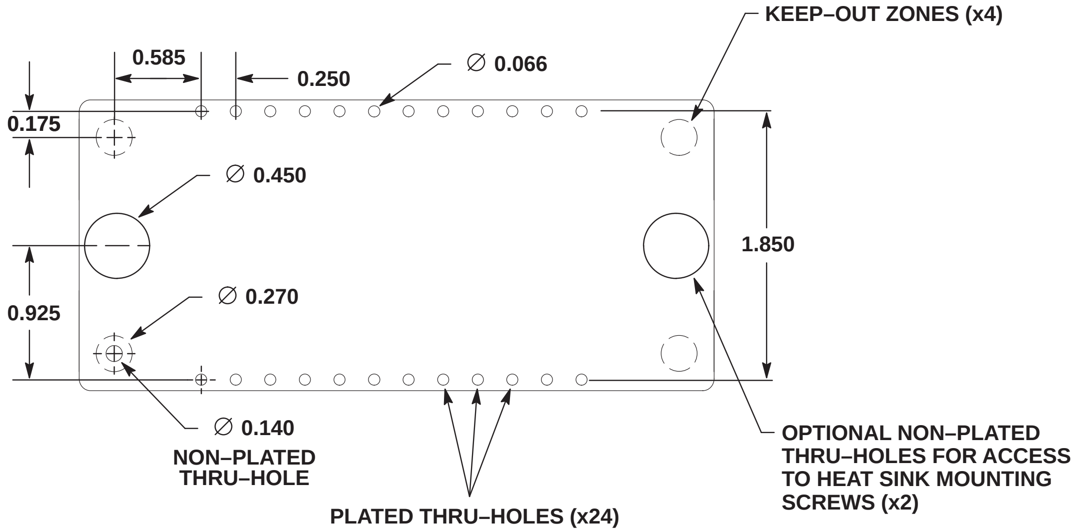


Figure 9. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 10. Package Footprint (Dimensions in Inches)

Advance Information

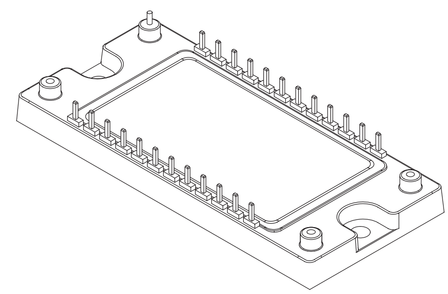
Hybrid Power Module

Integrated Power Stage for 1.0 hp 460 VAC Motor Drive

MHPM7A5S120DC3

Motorola Preferred Device

5.0 AMP, 1200 VOLT
HYBRID POWER MODULE



CASE 464D–01
ISSUE O

This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 1.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with fast soft free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 720 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A5S120DC3	1200	5.0	1.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Non–Repetitive Peak Input Rectifier Reverse Voltage (1) (T_J = 25°C to 150°C)	V_{RSM}	1600	V
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 125°C) (T_J = 25°C to 150°C)	V_{RRM2} V_{RRM1}	1600 900	V
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	5.0	A
Repetitive Peak IGBT Collector Current (2)	$I_{C(pk)}$	10	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	5.0	A
Repetitive Peak Free–Wheeling Diode Current (2)	$I_{F(pk)}$	10	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	16	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	19	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	8.0	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 720 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) Half–Sine 60 Hz, maximum reverse voltage capability decreases by 0.1% per °C at lower temperature
(2) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 5.0 A)	V_F	—	0.92	1.09	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±20	μA
Collector–Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	μA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	1200	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.5	3.5	V
Free–Wheeling Diode Forward Voltage (I_F = I_{F80}, V_{GE} = 0 V)	V_F	1.7	2.0	2.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	—	930	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	Q_T	—	31	—	nC
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	2.1	2.8	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	5.0	6.6	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	3.2	4.2	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

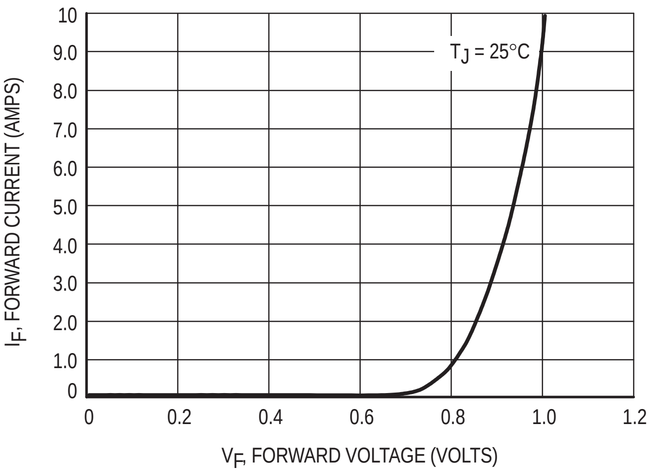


Figure 1. Forward Characteristics — Input Rectifier

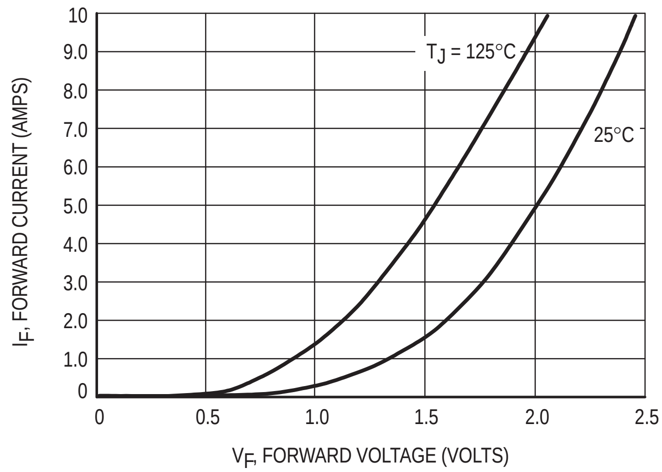


Figure 2. Forward Characteristics — Free–Wheeling Diode

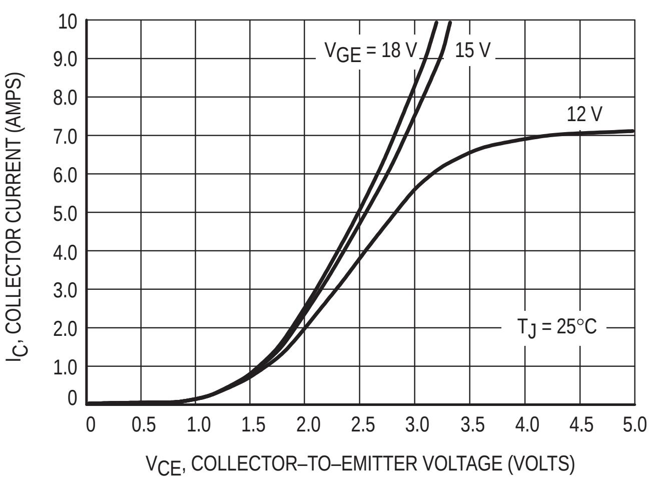


Figure 3. Forward Characteristics, T_J = 25°C

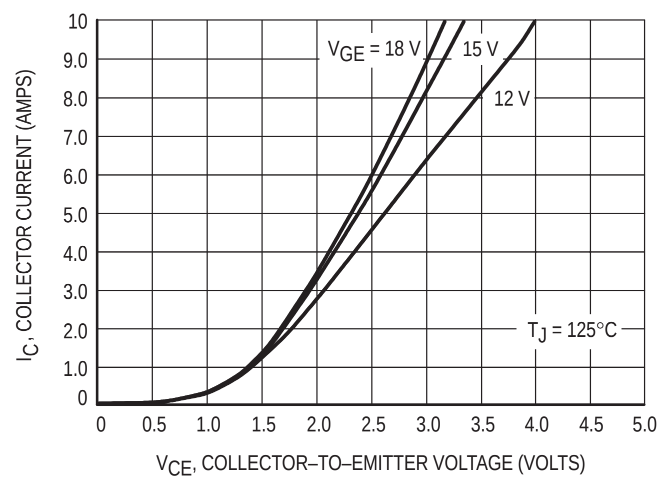


Figure 4. Forward Characteristics, T_J = 125°C

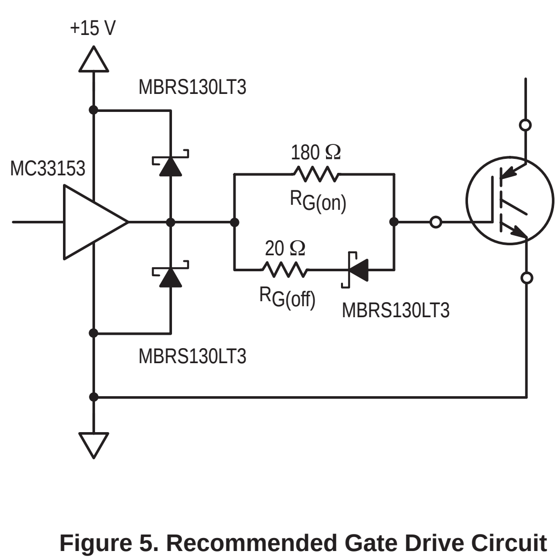


Figure 5. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

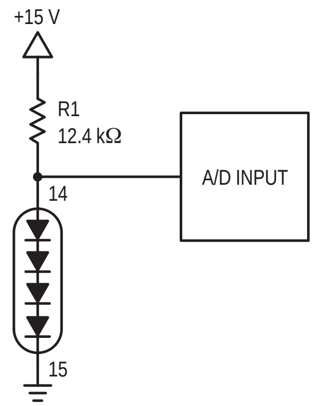


Figure 6. Recommended Temperature Sense Bias Circuit

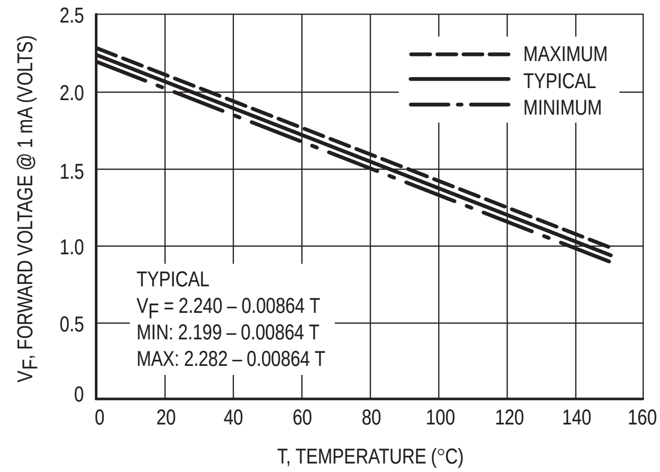


Figure 7. BAV99LT1 Temperature Sense Diode Performance: V_F = 2.59 – 7.31E–3 T_C

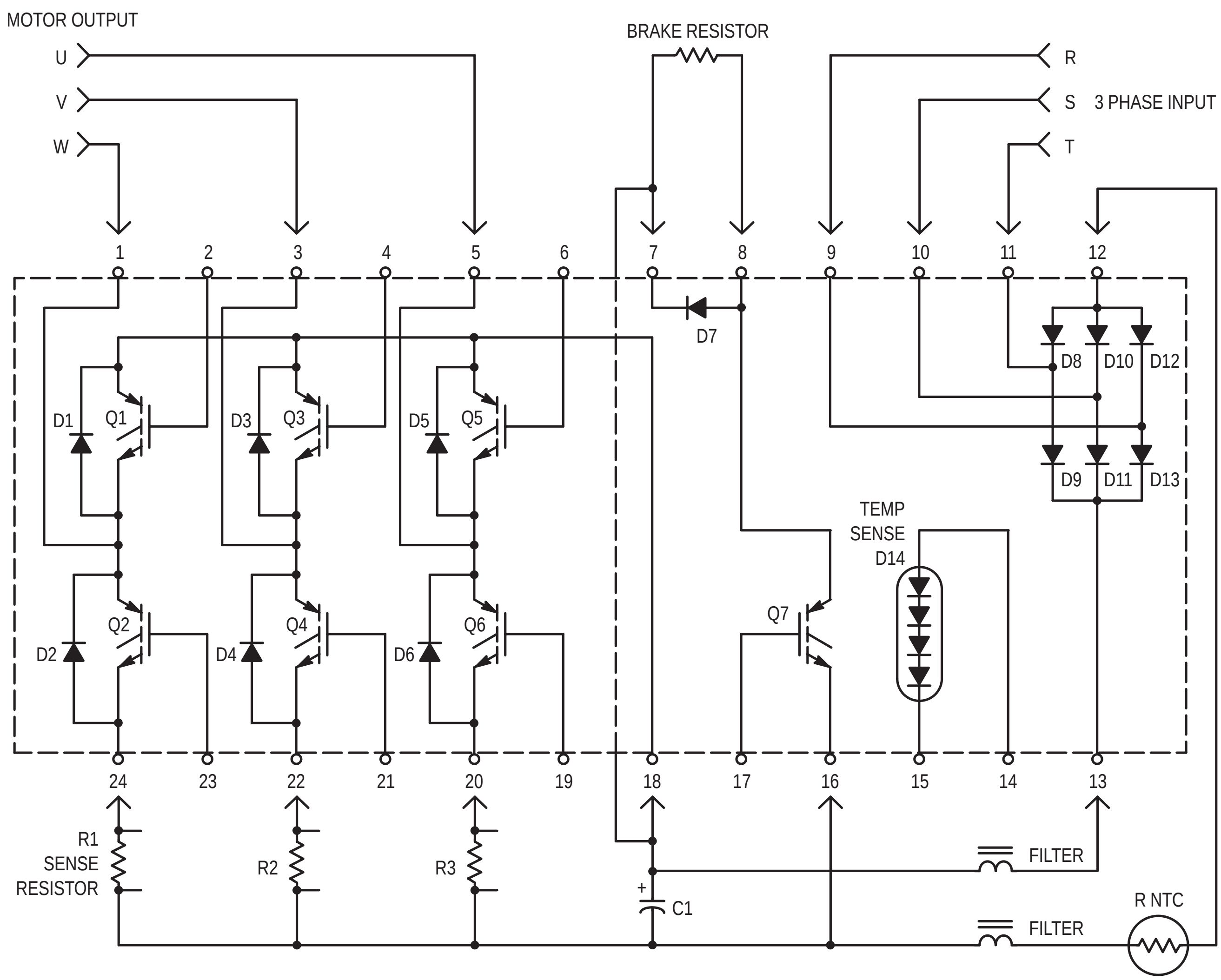
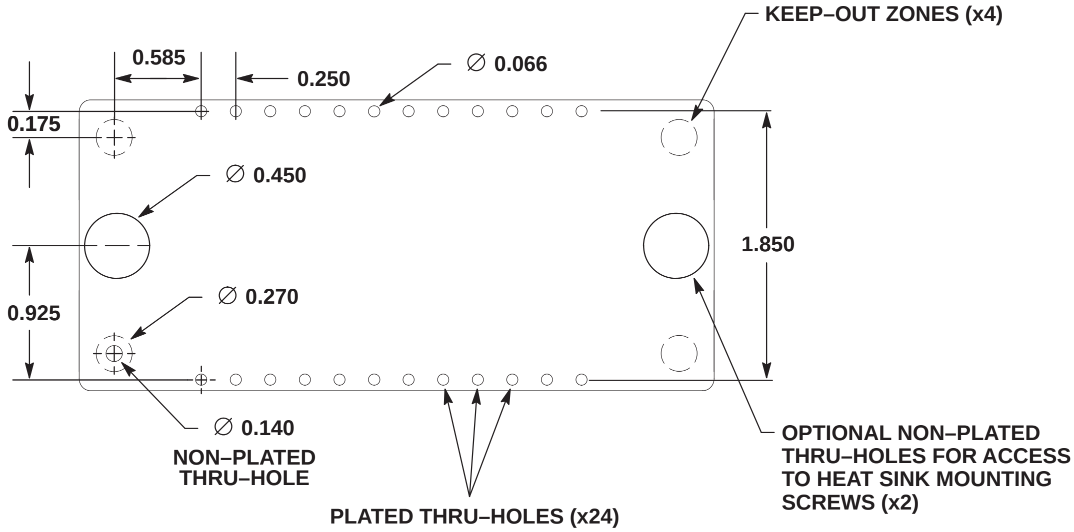


Figure 8. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 9. Package Footprint (Dimensions in Inches)

Advance Information
Hybrid Power Module
Integrated Power Stage for 2.0 hp 460 VAC Motor Drive

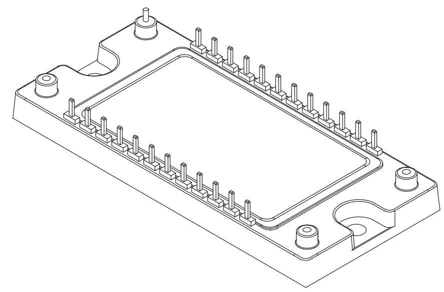
This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 2.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with fast soft free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 720 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/

MHPM7A10S120DC3

Motorola Preferred Device

10 AMP, 1200 VOLT
HYBRID POWER MODULE



CASE 464D–01
ISSUE O

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A10S120DC3	1200	10	2.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Non–Repetitive Peak Input Rectifier Reverse Voltage (1) (T_J = 25°C to 150°C)	V_{RSM}	1600	V
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 125°C) (T_J = 25°C to 150°C)	V_{RRM2} V_{RRM1}	1600 900	V
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	10	A
Repetitive Peak IGBT Collector Current (2)	$I_{C(pk)}$	20	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	10	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	8.6	A
Repetitive Peak Free–Wheeling Diode Current (2)	$I_{F(pk)}$	20	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	16	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	29	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	13	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 720 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) Half–Sine 60 Hz, maximum reverse voltage capability decreases by 0.1% per °C at lower temperature
(2) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 10 A)	V_F	—	1.02	1.25	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±20	μA
Collector–Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	μA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	1200	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.5	3.5	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)	V_F	1.8	2.0	2.4	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	—	1200	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	Q_T	—	65	—	nC
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	1.4	1.9	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	3.2	4.2	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	3.2	4.2	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

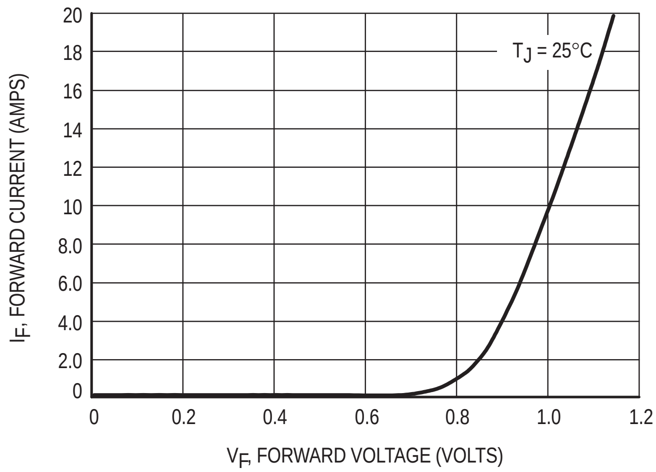


Figure 1. Forward Characteristics — Input Rectifier

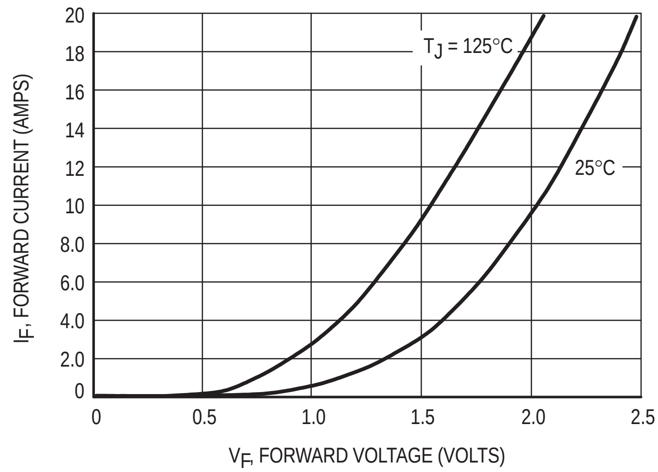


Figure 2. Forward Characteristics — Free–Wheeling Diode

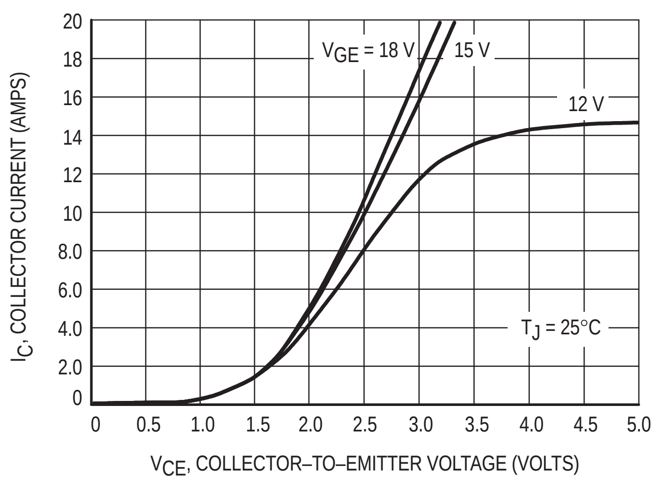


Figure 3. Forward Characteristics, T$_J$ = 25°C

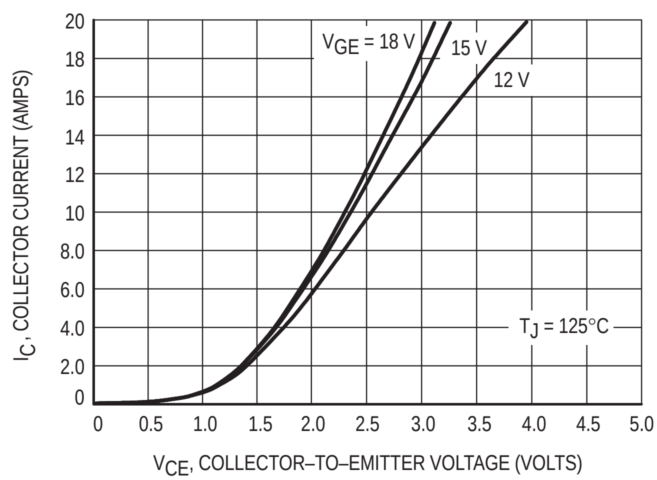


Figure 4. Forward Characteristics, T$_J$ = 125°C

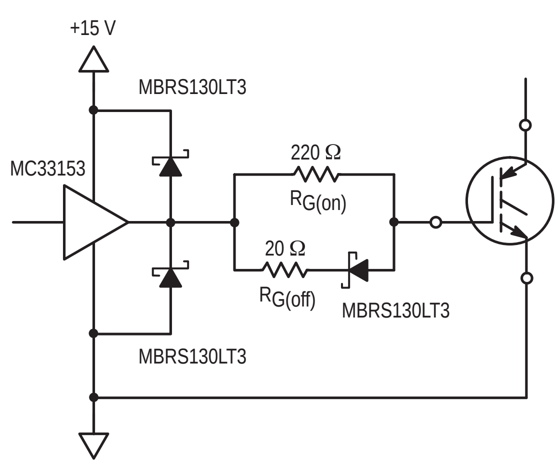


Figure 5. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

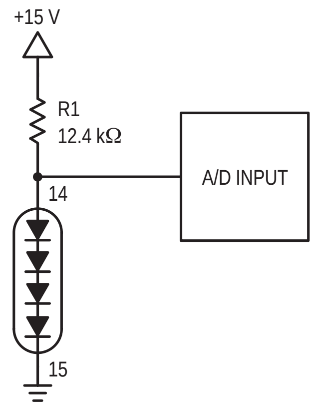


Figure 6. Recommended Temperature Sense Bias Circuit

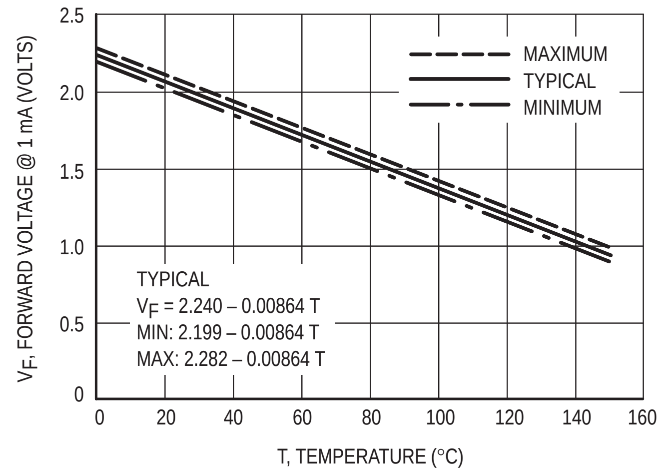


Figure 7. BAV99LT1 Temperature Sense Diode Performance: V_F = 2.59 – 7.31E–3 T_C

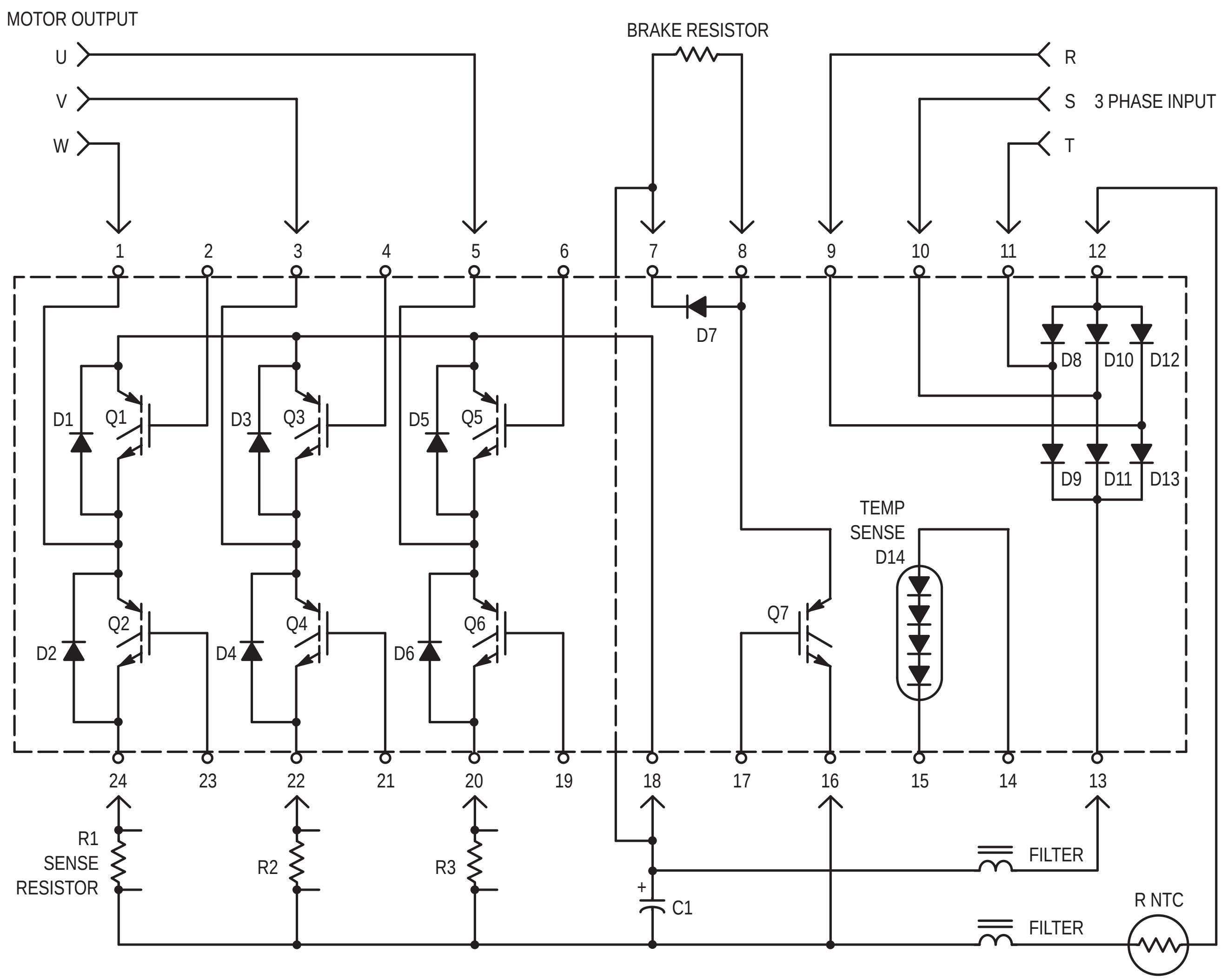
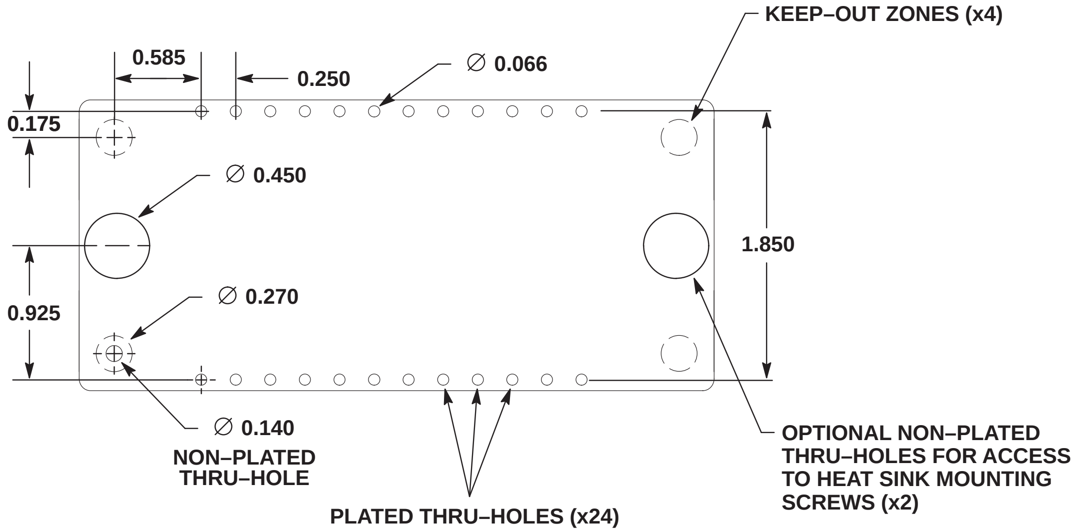


Figure 8. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 9. Package Footprint (Dimensions in Inches)

Advance Information
Hybrid Power Module
Integrated Power Stage for 3.0 hp 460 VAC Motor Drive

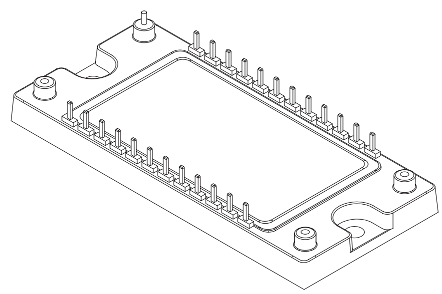
MHPM7A15S120DC3

Motorola Preferred Device

15 AMP, 1200 VOLT HYBRID POWER MODULE

This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 3.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with fast soft free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 720 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/



CASE 464D–01
ISSUE O

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A15S120DC3	1200	15	3.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Non–Repetitive Peak Input Rectifier Reverse Voltage (1) (T_J = 25°C to 150°C)	V_{RSM}	1600	V
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 125°C) (T_J = 25°C to 150°C)	V_{RRM2} V_{RRM1}	1600 900	V
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	15	A
Repetitive Peak IGBT Collector Current (2)	$I_{C(pk)}$	30	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	15	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	11.7	A
Repetitive Peak Free–Wheeling Diode Current (2)	$I_{F(pk)}$	30	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	16	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	36	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	16	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 720 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) Half–Sine 60 Hz, maximum reverse voltage capability decreases by 0.1% per °C at lower temperature
(2) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 15 A)	V_F	—	1.09	1.38	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±20	µA
Collector–Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	µA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	1200	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.5	3.5	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)	V_F	1.8	2.0	2.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	—	2800	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	Q_T	—	100	—	nC
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	1.1	1.5	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	2.4	3.3	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	3.2	4.2	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

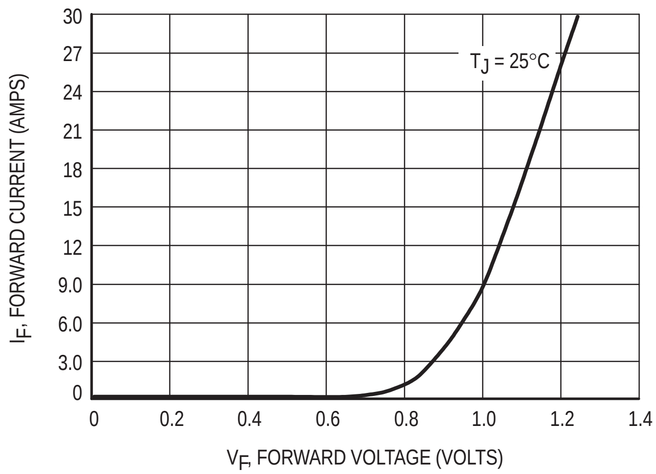


Figure 1. Forward Characteristics — Input Rectifier

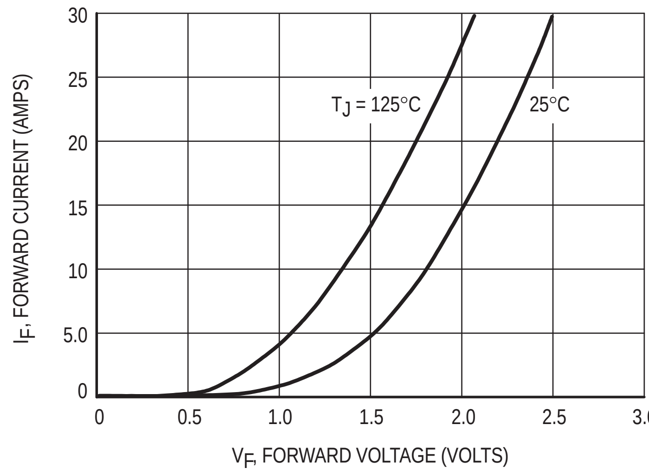


Figure 2. Forward Characteristics — Free–Wheeling Diode

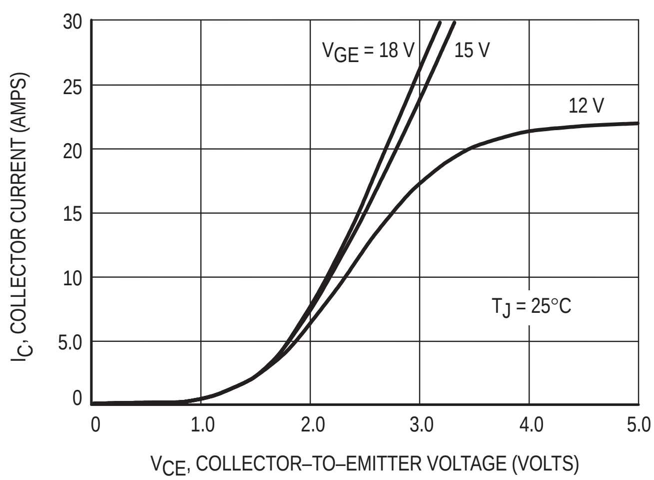


Figure 3. Forward Characteristics, T_J = 25°C

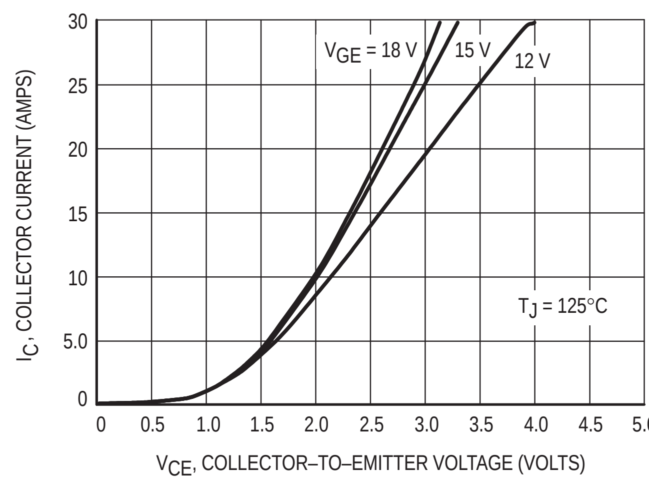


Figure 4. Forward Characteristics, T_J = 125°C

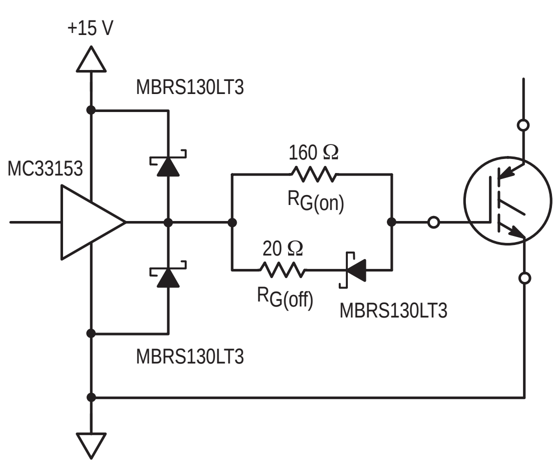


Figure 5. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

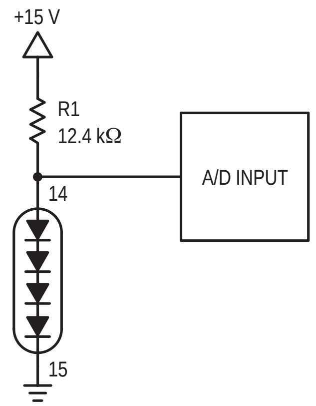


Figure 6. Recommended Temperature Sense Bias Circuit

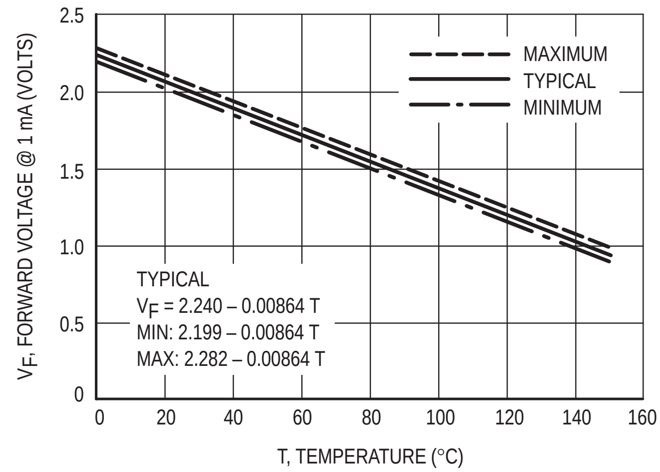


Figure 7. BAV99LT1 Temperature Sense Diode Performance: V_F = 2.59 – 7.31E–3 T_C

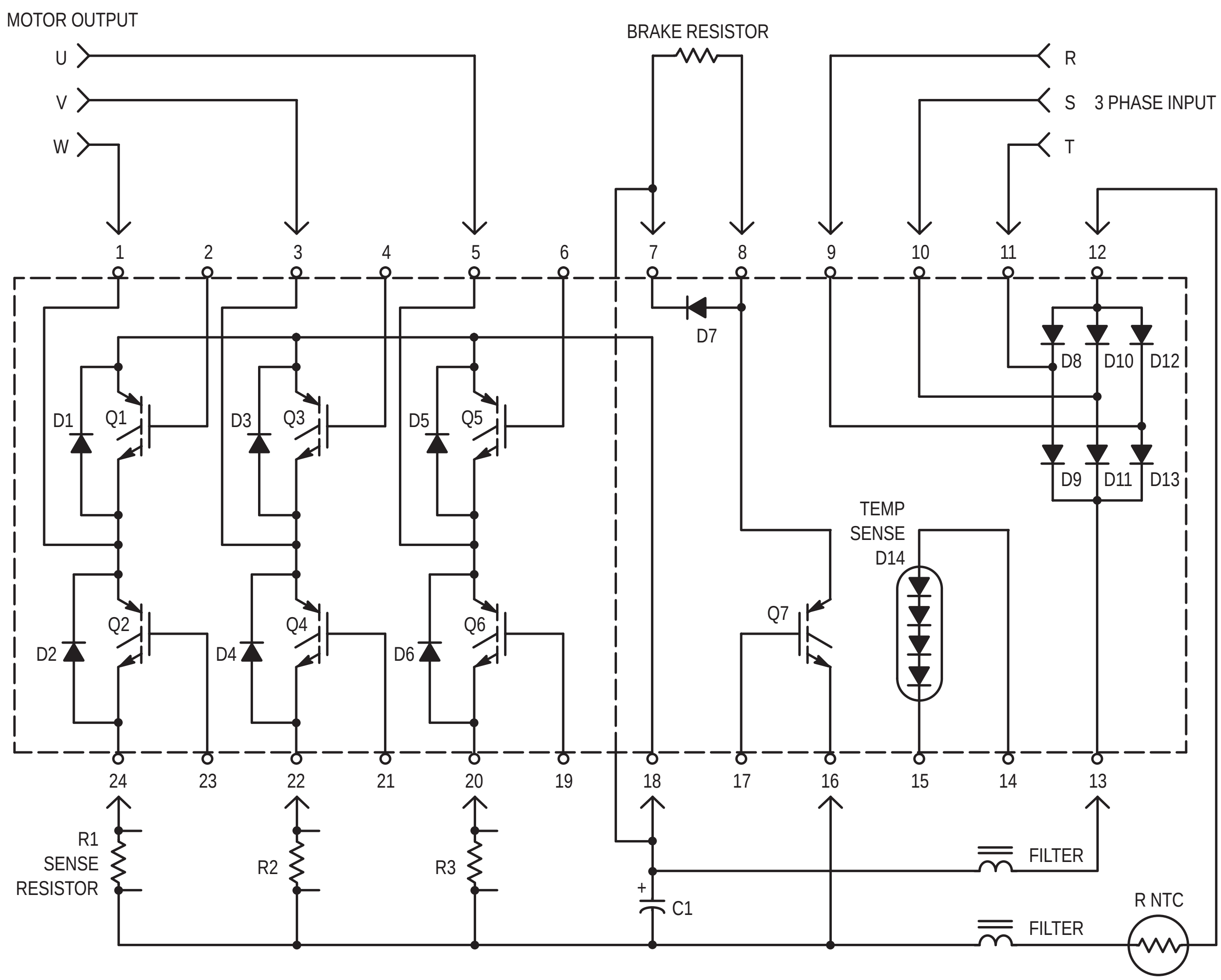
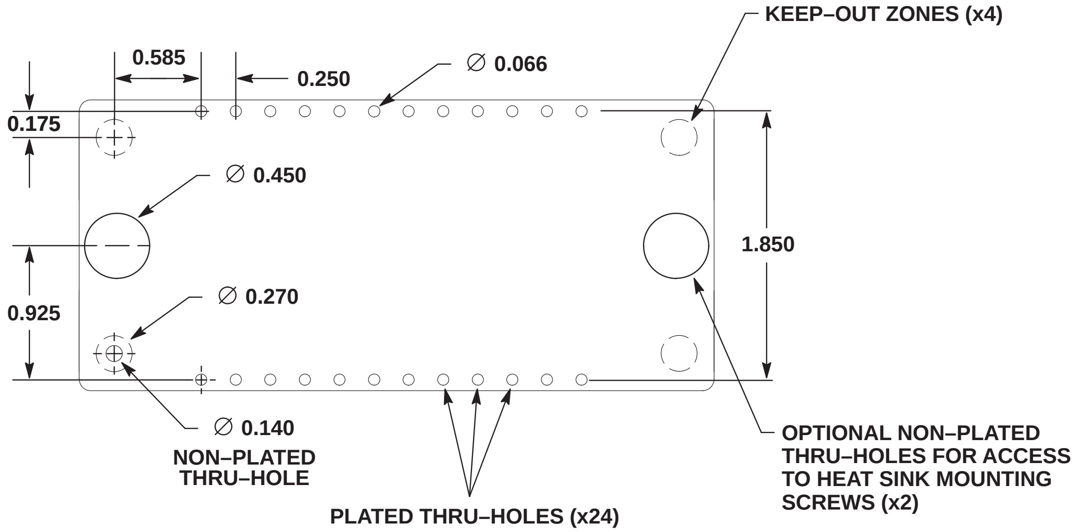


Figure 8. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
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2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 9. Package Footprint (Dimensions in Inches)

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Advance Information
Hybrid Power Module
Integrated Power Stage for 5.0 hp 460 VAC Motor Drive

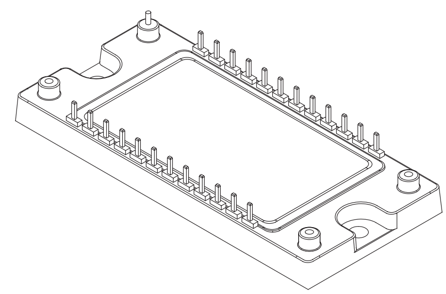
MHPM7A25S120DC3

Motorola Preferred Device

25 AMP, 1200 VOLT HYBRID POWER MODULE

This VersaPower™ module integrates a 3–phase inverter, 3–phase rectifier, brake, and temperature sense in a single convenient package. It is designed for 5.0 hp general purpose 3–phase induction motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with fast soft free–wheeling diodes to give optimum performance. The solderable top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 720 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Independent Brake Circuit Connections
- UL Recognition Pending
- Visit our website at http://www.mot–sps.com/tsg/



CASE 464D–01
ISSUE O

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM7A25S120DC3	1200	25	5.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Non–Repetitive Peak Input Rectifier Reverse Voltage (1) (T_J = 25°C to 150°C)	V_{RSM}	1600	V
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 125°C) (T_J = 25°C to 150°C)	V_{RRM2} V_{RRM2}	1600 900	V
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	25	A
Repetitive Peak IGBT Collector Current (2)	$I_{C(pk)}$	50	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	25	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	16.5	A
Repetitive Peak Free–Wheeling Diode Current (2)	$I_{F(pk)}$	50	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	23.4	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	50	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	23	W
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 720 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

(1) Half–Sine 60 Hz, maximum reverse voltage capability decreases by 0.1% per °C at lower temperature
(2) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I_F = 25 A)	V_F	—	1.1	1.375	V
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±20	µA
Collector–Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	µA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	1200	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)	$V_{CE(sat)}$	—	2.5	3.5	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)	V_F	1.8	2.1	2.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	—	2700	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	Q_T	—	100	—	nC
THERMAL CHARACTERISTICS, EACH DIE					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	0.8	1.1	°C/W
Thermal Resistance — Free–Wheeling (Fast Soft) Diode	$R_{\theta JC}$	—	1.8	2.4	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	2.4	3.3	°C/W
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	1.983	2.024	2.066	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–8.64	—	mV/°C

TYPICAL CHARACTERISTICS

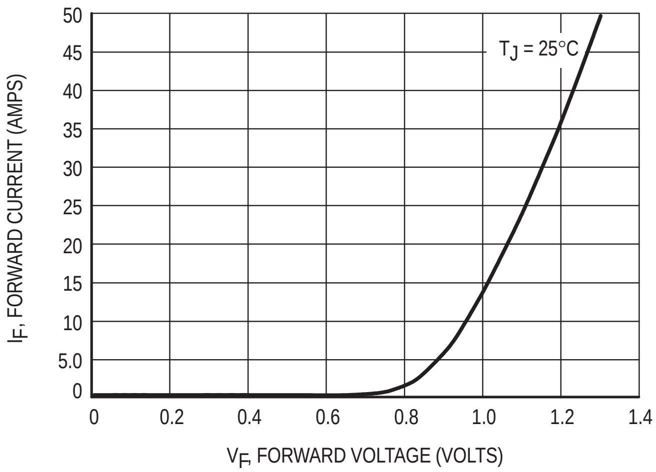


Figure 1. Forward Characteristics — Input Rectifier

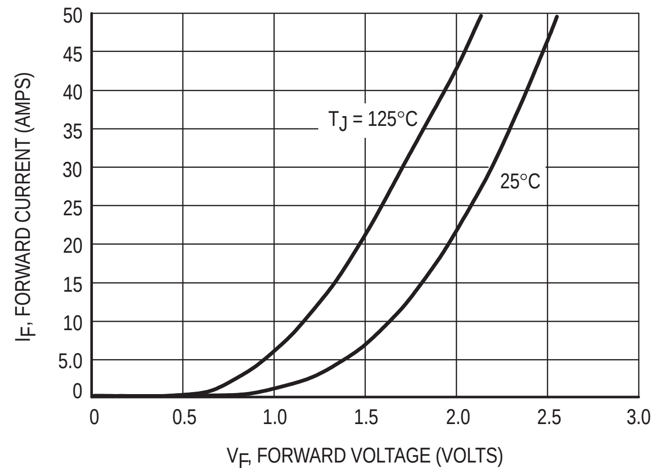


Figure 2. Forward Characteristics — Free–Wheeling Diode

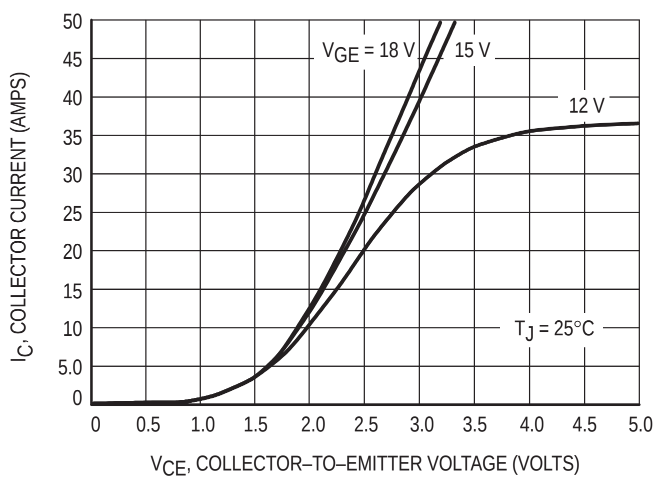


Figure 3. Forward Characteristics, T_J = 25°C

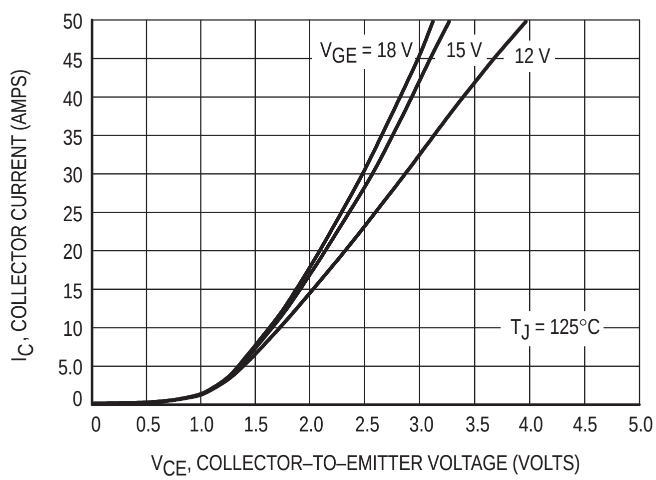


Figure 4. Forward Characteristics, T_J = 125°C

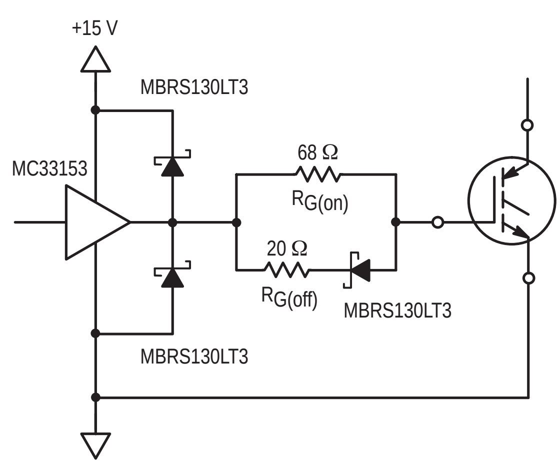


Figure 5. Recommended Gate Drive Circuit

TYPICAL CHARACTERISTICS

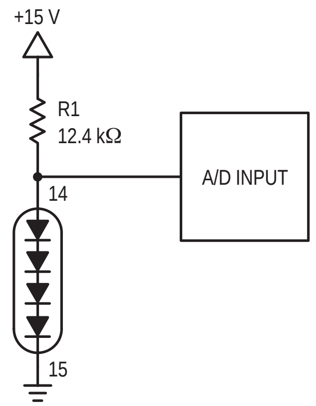


Figure 6. Recommended Temperature Sense Bias Circuit

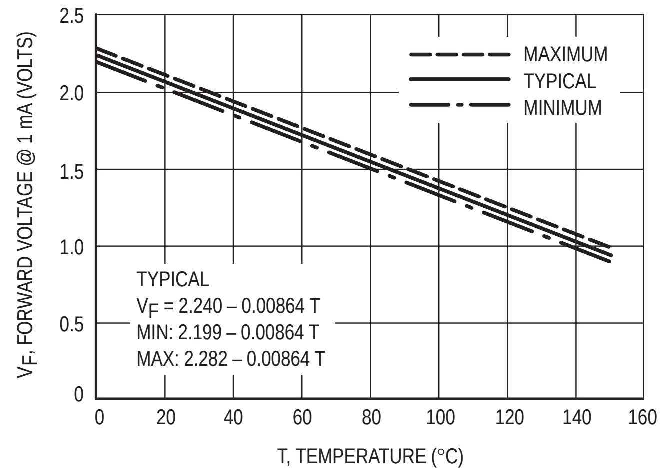


Figure 7. BAV99LT1 Temperature Sense Diode Performance: $V_F = 2.59 - 7.31E{-}3\ T_C$

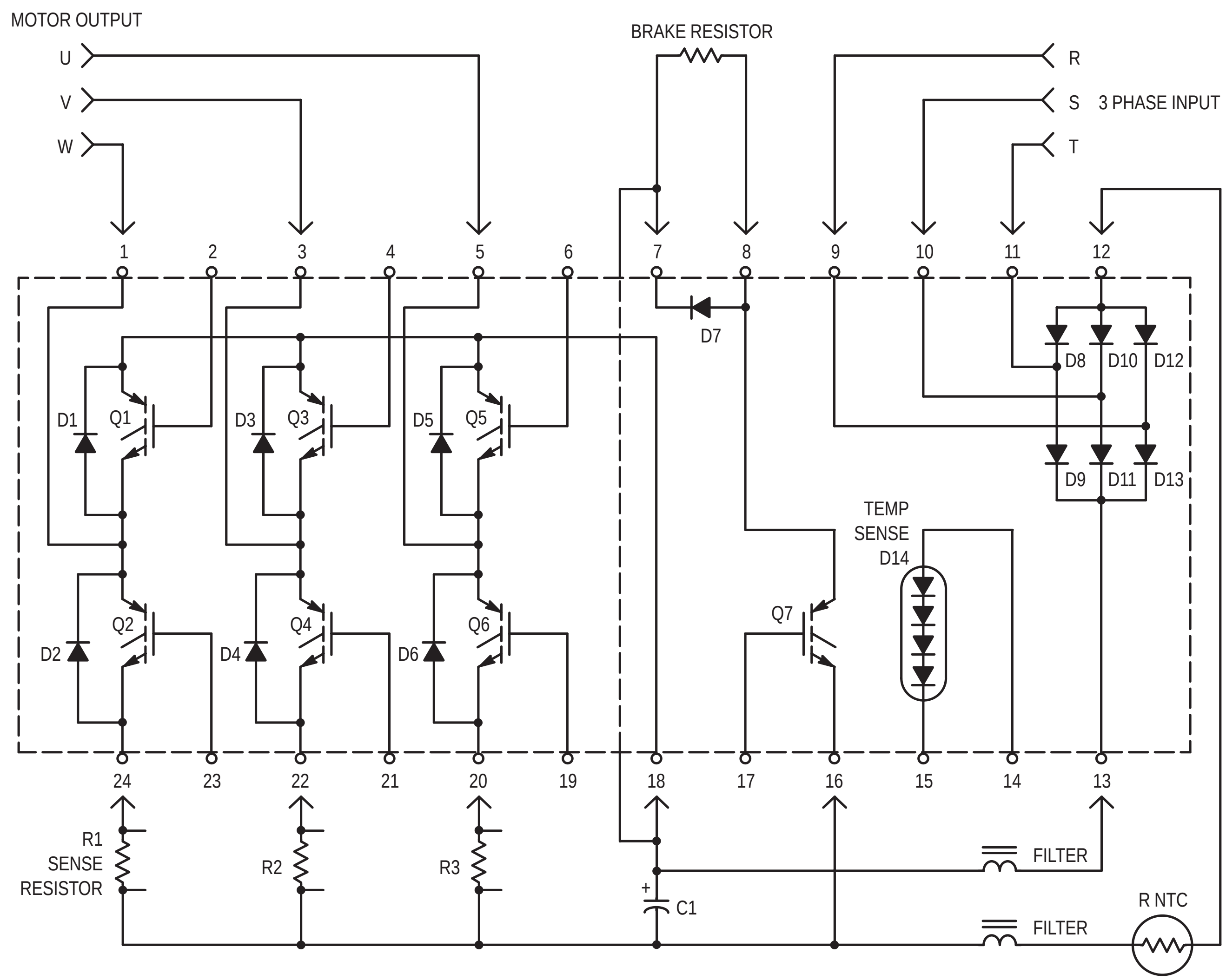
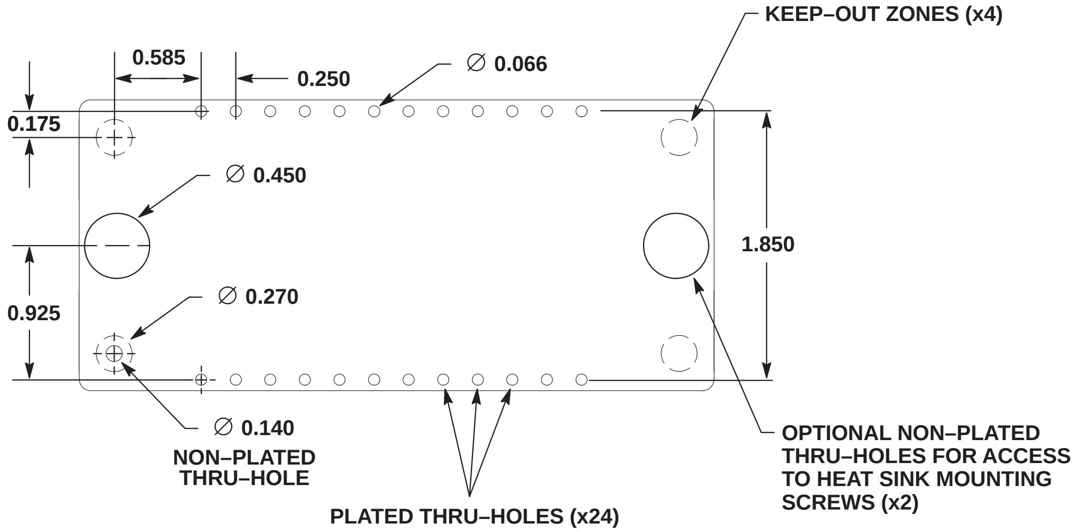


Figure 8. Schematic of Module, Showing Pin–Out and External Connections



NOTES:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Figure 9. Package Footprint (Dimensions in Inches)

Advance Information

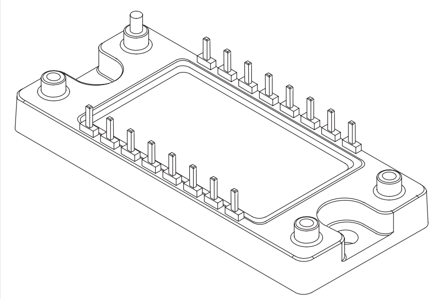
Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drives

MHPM6B15E60D3
MHPM6B10E60D3
MHPM6B7E60D3

Motorola Preferred Devices

7.0, 10, 15 AMP, 600 VOLT
HYBRID POWER MODULES



CASE 464–03
ISSUE B

These VersaPower™ modules integrate a 3–phase inverter and 3–phase rectifier in a single convenient package. They are designed for 0.5, 1.0, and 1.5 hp motor drive applications at frequencies up to 15 kHz. The inverter incorporates advanced E–Series insulated gate bipolar transistors (IGBT) matched with ultrafast soft (UFS) free–wheeling diodes to give optimum performance. The input bridge uses rugged, efficient diodes with high surge capability. The top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 400 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Gate–Emitter Clamp Diodes for ESD Protection
- UL Recognized
- Visit our website at http://www.mot–sps.com/tsg/

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM6B7E60D3	600	7.0	0.5
XHPM6B10E60D3	600	10	1.0
XHPM6B15E60D3	600	15	1.5

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 150°C)		V_{RRM}	900	V
IGBT Reverse Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	7E60 10E60 15E60	I_{Cmax}	7.0 10 15	A
Continuous IGBT Collector Current (T_C = 80°C)	7E60 10E60 15E60	I_{C80}	7.0 10 13	A
Repetitive Peak IGBT Collector Current (1)	7E60 10E60 15E60	$I_{C(pk)}$	14 20 30	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	7E60 10E60 15E60	I_{Fmax}	7.0 10 15	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	7E60 10E60 15E60	I_{F80}	5.2 6.8 10	A
Repetitive Peak Free–Wheeling Diode Current (1)	7E60 10E60 15E60	$I_{F(pk)}$	14 20 30	A

(1) 1.0 ms = 1.0% duty cycle

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)		I_{Omax}	20	A
Continuous Input Rectifier Current (T_C = 25°C)		I_{DC}	20	A
Non–Repetitive Peak Input Rectifier Forward Surge Current (2) (T_J = 95°C prior to start of surge)		I_{FSM}	475	A
IGBT Power Dissipation per die (T_C = 95°C)	7E60 10E60 15E60	P_D	14 17 23	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	7E60 10E60 15E60	P_D	7.4 9.0 13	W
Input Rectifier Power Dissipation per die (T_C = 95°C)		P_D	13	W
Junction Temperature Range		T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 400 V, T_J = 125°C)		t_{sc}	10	μs
Isolation Voltage, pin to baseplate		V_{ISO}	2500	Vac
Operating Case Temperature Range		T_C	–40 to +95	°C
Storage Temperature Range		T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes		—	12	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS						
Input Rectifier Forward Voltage (I = 15 A) T_J = 125°C		V_F	— —	0.97 0.88	1.2 —	V
Instantaneous Reverse Current (V = 900 V) T_J = 150°C		I_R	— —	50 3000	— —	μA
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)		I_{GES}	—	—	±50	μA
Collector–Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V)		I_{CES}	—	5.0	100	μA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)		$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)		$V_{(BR)CES}$	600	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V) T_J = 125°C		$V_{CE(SAT)}$	— —	2.0 1.8	2.4 —	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V) T_J = 125°C		V_F	1.7 —	2.0 1.8	2.3 —	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	7E60 10E60 15E60	C_{ies}	— — —	780 1020 1605	— — —	pF
THERMAL CHARACTERISTICS (EACH DIE)						
Thermal Resistance — IGBT	7E60 10E60 15E60	$R_{\theta JC}$	— — —	3.1 2.6 1.9	3.8 3.2 2.4	°C/W
Thermal Resistance — Free–Wheeling Diode	7E60 10E60 15E60	$R_{\theta JC}$	— — —	6.0 4.8 3.4	7.5 6.0 4.2	°C/W
Thermal Resistance — Input Rectifier		$R_{\theta JC}$	—	3.4	4.2	°C/W

(2) 1.0 ms = 10% pulse width (t_W 10%)

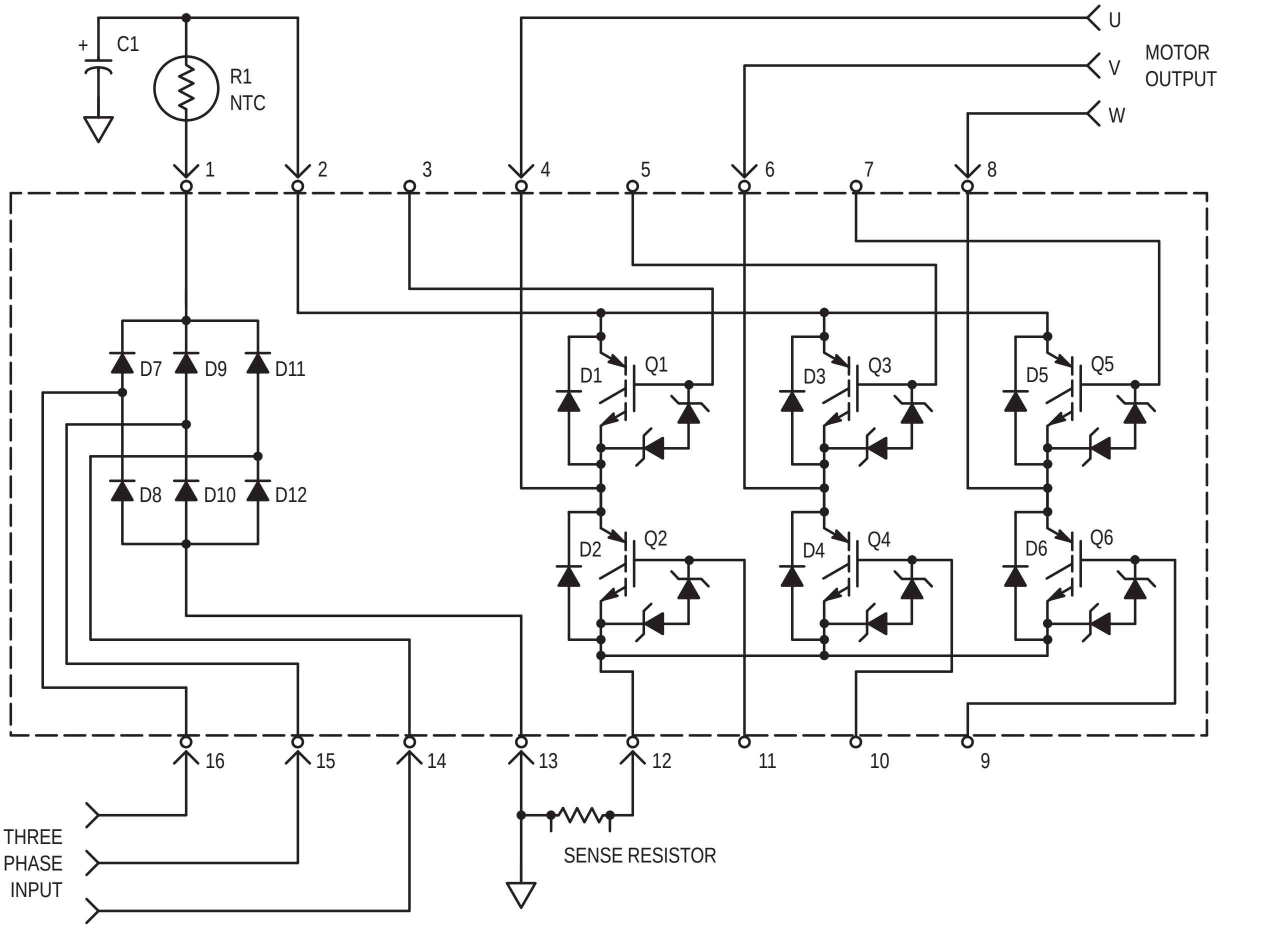


Figure 1. Schematic of Module, Showing Pin–Out and External Connections

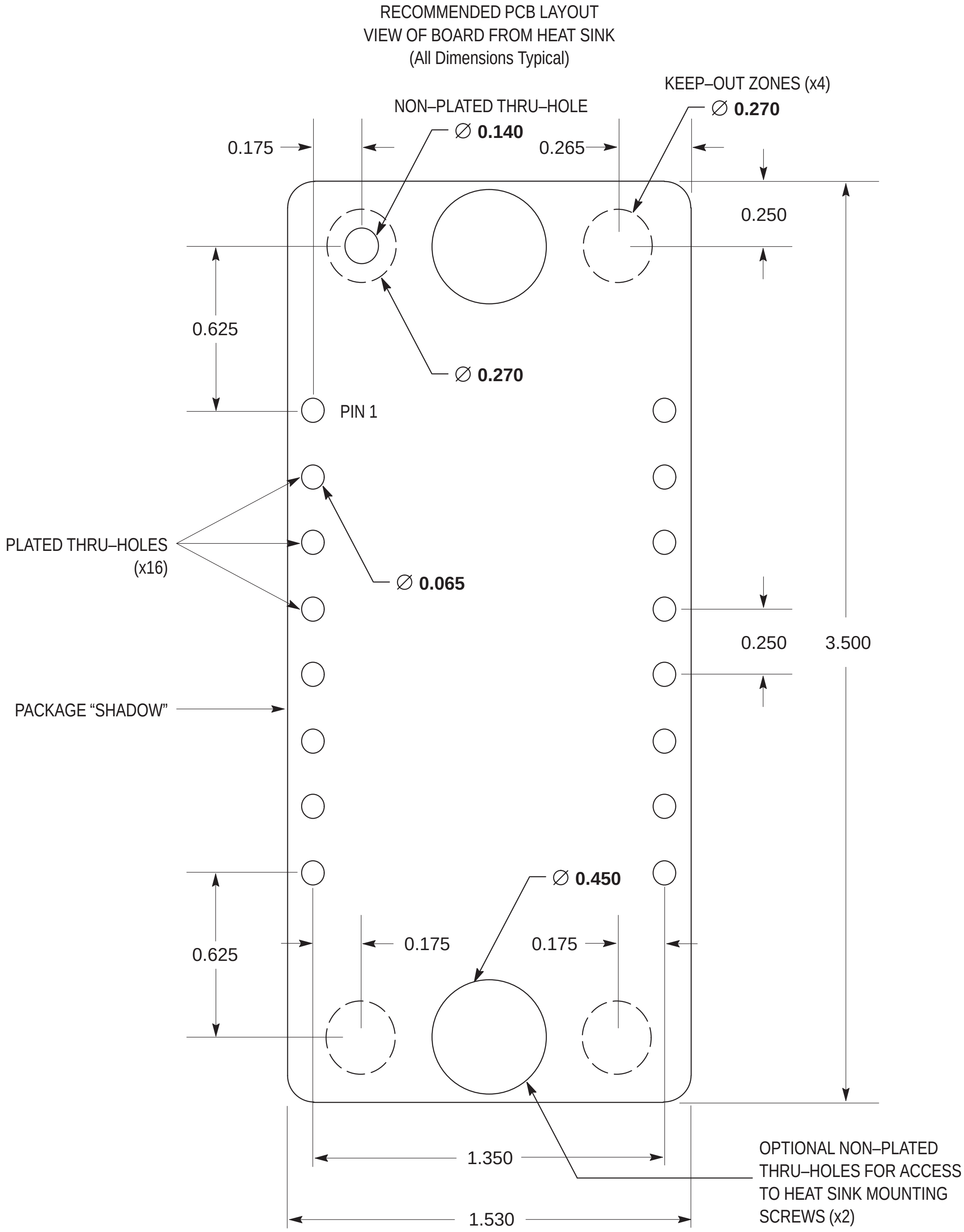


Figure 2. Package Footprint

NOTE:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates net size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Advance Information

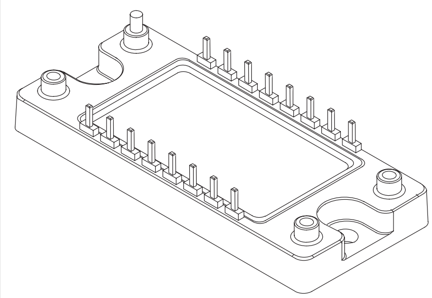
Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drives

MHPM6B20E60D3

Motorola Preferred Device

20 AMP, 600 VOLT HYBRID POWER MODULES



CASE 464–03
ISSUE B

This VersaPower™ module integrates a 3–phase inverter and 3–phase rectifier in a single convenient package. It is designed for 2.0 hp motor drive applications at frequencies up to 15 kHz. The inverter incorporates advanced EM–Series insulated gate bipolar transistors (IGBT) matched with ultrafast soft (UFS) free–wheeling diodes to give optimum performance. The input bridge uses rugged, efficient diodes with high surge capability. The top connector pins are designed for easy interfacing to the user's control board. It is pin–compatible with MHPM6B15E60D3 series modules for scalability.

- Short Circuit Rated 10 µs @ 125°C, 400 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- Gate–Emitter Clamp Diodes for ESD Protection
- UL Recognized
- Visit our website at http://www.mot–sps.com/tsg/

ORDERING INFORMATION

Device	Voltage Rating	Current Rating	Equivalent Horsepower
XHPM6B20E60D3	600	20	2.0

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Repetitive Peak Input Rectifier Reverse Voltage (T_J = 25°C to 150°C)	V_{RRM}	900	V
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	±20	V
Continuous IGBT Collector Current (T_C = 25°C)	I_{Cmax}	20	A
Continuous IGBT Collector Current (T_C = 80°C)	I_{C80}	15.8	A
Repetitive Peak IGBT Collector Current (1)	$I_{C(pk)}$	40	A
Continuous Free–Wheeling Diode Current (T_C = 25°C)	I_{Fmax}	20	A
Continuous Free–Wheeling Diode Current (T_C = 80°C)	I_{F80}	14.1	A
Repetitive Peak Free–Wheeling Diode Current (1)	$I_{F(pk)}$	40	A
Average Converter Output Current (Peak–to–Average ratio of 10, T_C = 95°C)	I_{Omax}	20	A
Continuous Input Rectifier Current (T_C = 25°C)	I_{DC}	20	A
Non–Repetitive Peak Input Rectifier Forward Surge Current (2) (T_J = 95°C prior to start of surge)	I_{FSM}	475	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	25	W
Free–Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	17	W
Input Rectifier Power Dissipation per die (T_C = 95°C)	P_D	13	W

(1) 1.0 ms = 1.0% duty cycle
(2) 1.0 ms = 10% pulse width (t_W 10%)

Preferred devices are Motorola recommended choices for future use and best overall value.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Junction Temperature Range	T_J	–40 to +150	°C
Short Circuit Duration (V_{CE} = 400 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, pin to baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	–40 to +95	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	12	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Input Rectifier Forward Voltage (I = 20 A) T_J = 125°C	V_F	— —	1.0 0.92	1.25 —	V
Instantaneous Reverse Current (V = 900 V) T_J = 150°C	I_R	— —	50 3000	— —	µA
Gate–Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ±20 V)	I_{GES}	—	—	±50	µA
Collector–Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V)	I_{CES}	—	5.0	100	µA
Gate–Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	600	—	—	V
Collector–Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V) T_J = 125°C	$V_{CE(SAT)}$	— —	2.2 2.5	2.6 —	V
Free–Wheeling Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V) T_J = 125°C	V_F	1.6 —	2.0 1.8	2.3 —	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	2080	—	pF
THERMAL CHARACTERISTICS (EACH DIE)					
Thermal Resistance — IGBT	$R_{\theta JC}$	—	1.8	2.2	°C/W
Thermal Resistance — Free–Wheeling Diode	$R_{\theta JC}$	—	2.6	3.3	°C/W
Thermal Resistance — Input Rectifier	$R_{\theta JC}$	—	3.4	4.2	°C/W

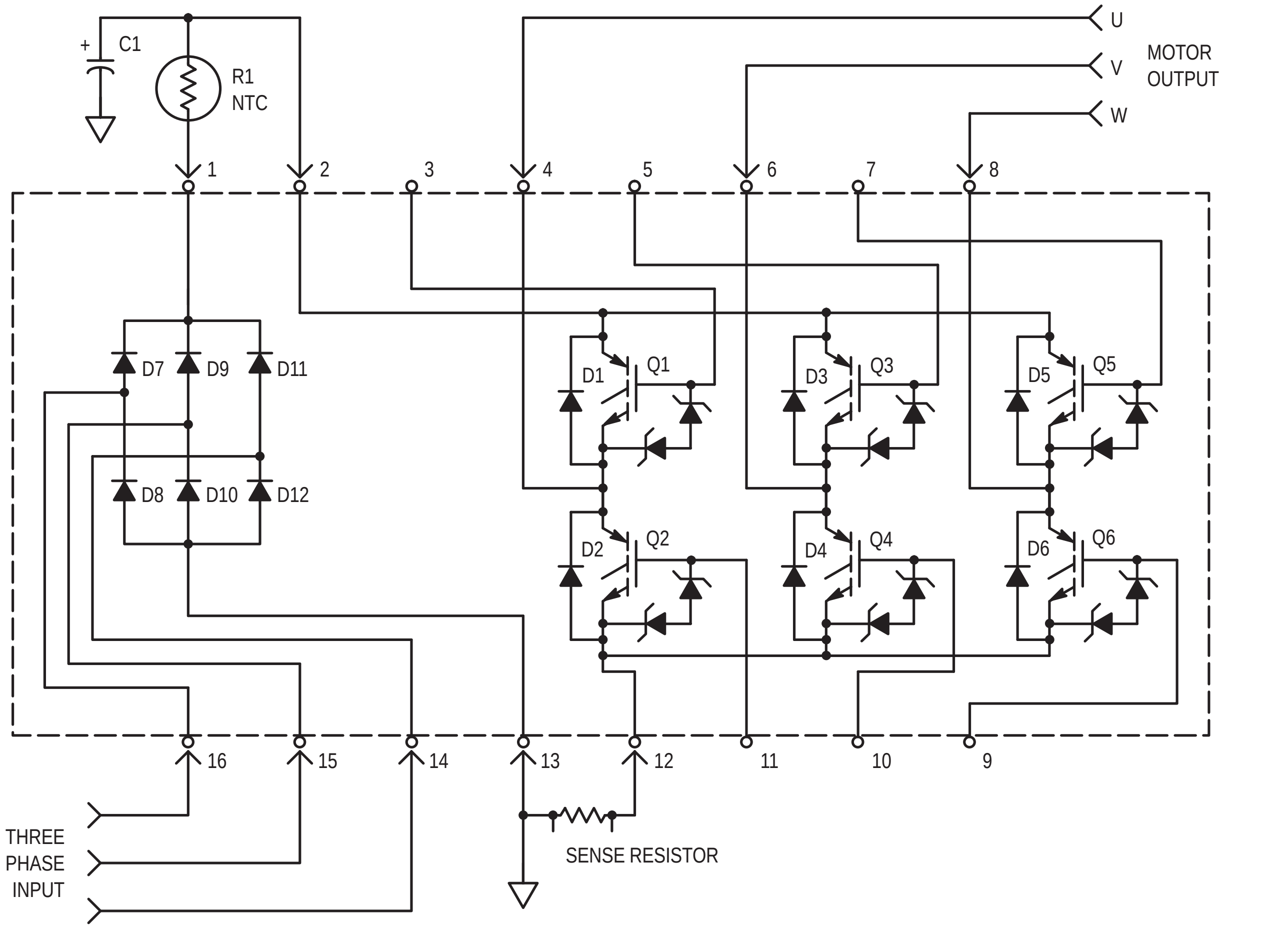


Figure 1. Schematic of Module, Showing Pin–Out and External Connections

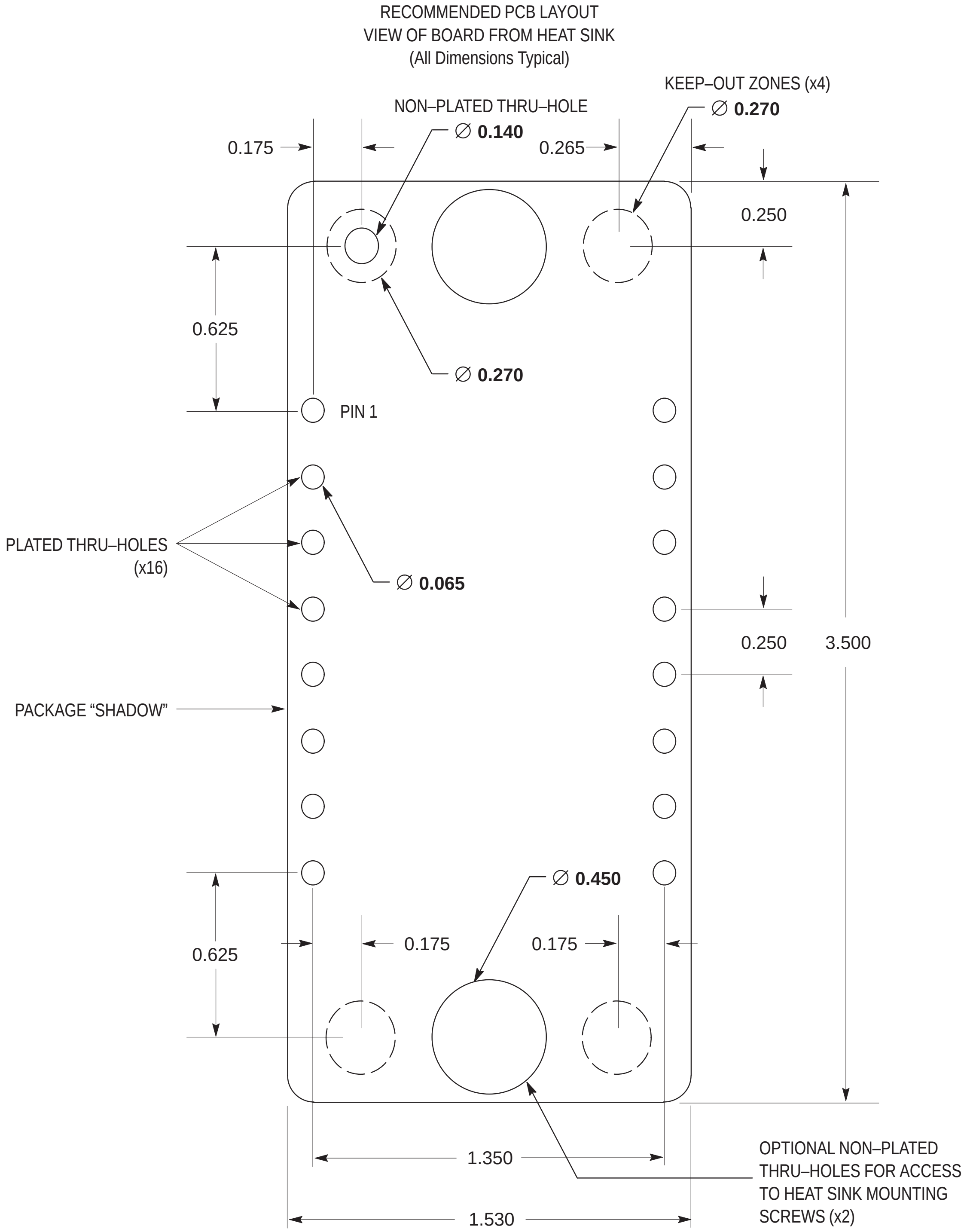


Figure 2. Package Footprint

NOTE:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates net size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Hybrid Power Module

Integrated Power Stage for 230 VAC Motor Drives

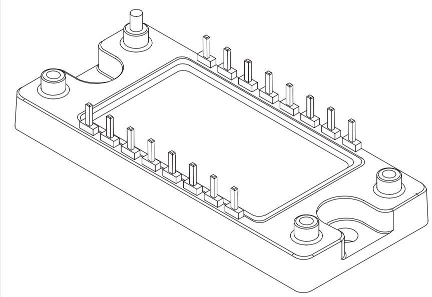
MHPM6B10A60D
MHPM6B20A60D

Motorola Preferred Devices

10, 20 AMP, 600 V
HYBRID POWER MODULES

These VersaPower™ modules integrate a 3–phase inverter in a single convenient package. They are designed for 1.0 and 2.0 hp motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimum performance. The top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 300 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- UL Recognized
- Visit our website at http://www.mot–sps.com/tsg/



CASE 464–03
ISSUE B

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
IGBT Reverse Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	± 20	V
Continuous IGBT Collector Current	10A60 20A60	I_{Cmax}	10 20	A
Repetitive Peak IGBT Collector Current (1)	10A60 20A60	$I_{C(pk)}$	20 40	A
Continuous Free–Wheeling Diode Current	10A60 20A60	I_{Fmax}	10 20	A
Repetitive Peak Free–Wheeling Diode Current (1)	10A60 20A60	$I_{F(pk)}$	20 40	A
IGBT Power Dissipation (T_C = 25°C)	10A60 20A60	P_D	52 78	W
Diode Power Dissipation (T_C = 25°C)	10A60 20A60	P_D	19 38	W
IGBT Power Dissipation (T_C = 95°C)	10A60 20A60	P_D	23 34	W
Diode Power Dissipation (T_C = 95°C)	10A60 20A60	P_D	8.3 17	W
Junction Temperature Range		T_J	– 40 to +150	°C
Short Circuit Duration (V_{CE} = 300 V, T_J = 25°C)		t_{sc}	10	µs
Isolation Voltage		V_{ISO}	2500	Vac
Operating Case Temperature Range		T_C	– 40 to +95	°C
Storage Temperature Range		T_{stg}	– 40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes (#8 or M4 screws)		—	12	in–lb

(1) 1.0 ms = 1.0% duty cycle

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 125°C	I_{CES}	—	6.0 2000	100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)	$V_{(BR)CES}$	600	—	—	V
Collector-Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V) T_J = 125°C	$V_{CE(SAT)}$	— —	2.35 2.31	3.5 —	V
Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V) T_J = 125°C	V_F	— —	1.23 1.12	2.0 —	V
Input Capacitance (V_{CE} = 10 V, V_{GE} = 0 V, f = 1.0 Mhz) 10A60 20A60	C_{ies}	— —	2300 4400	— —	pF
Input Gate Charge (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V) 10A60 20A60	Q_T	— —	75 135	— —	nC
INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 25°C)					
Recommended Gate Resistor Turn–On 10A60 20A60 Turn–Off	$R_{G(on)}$ $R_{G(off)}$	— — —	180 47 20	— — —	Ω
Turn-On Delay Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	$t_{d(on)}$	— —	375 215	— —	ns
Rise Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	t_r	— —	160 125	— —	ns
Turn–Off Delay Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	$t_{d(off)}$	—	219	—	ns
Fall Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	t_f	—	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	E_{on}	— —	0.85 1.6	1.0 2.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified) 10A60 20A60	E_{off}	— —	0.17 0.4	1.0 2.0	mJ
Diode Reverse Recovery Time (I_F = I_{Fmax}, V = 300 V, R_G as specified)	t_{rr}	—	150	—	ns
Peak Reverse Recovery Current (I_F = I_{Fmax}, V = 300 V, R_G as specified) 10A60 20A60	I_{rrm}	— —	6.8 12	— —	A
Diode Stored Charge (I_F = I_{Fmax}, V = 300 V, R_G as specified) 10A60 20A60	Q_{rr}	— —	560 1060	— —	nC

INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Turn–On Delay Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	$t_{d(on)}$				ns
10A60		—	335	—	
20A60		—	200	—	
Rise Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	t_r				ns
10A60		—	160	—	
20A60		—	125	—	
Turn–Off Delay Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	$t_{d(off)}$	—	230	—	ns
Fall Time (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	t_f	—	460	—	ns
Turn–On Energy (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	E_{on}				mJ
10A60		—	1.2	—	
20A60		—	2.2	—	
Turn–Off Energy (V_{CE} = 300 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	E_{off}				mJ
10A60		—	0.44	—	
20A60		—	0.82	—	
Diode Reverse Recovery Time (I_F = I_{Fmax}, V = 300 V, R_G as specified)	t_{rr}	—	240	—	ns
Peak Reverse Recovery Current (I_F = I_{Fmax}, V = 300 V, R_G as specified) 10A60	I_{rrm}	—	10	—	A
20A60		—	18	—	
Diode Stored Charge (I_F = I_{Fmax}, V = 300 V, R_G as specified) 10A60	Q_{rr}	—	1330	—	nC
20A60		—	2400	—	

THERMAL CHARACTERISTICS (Each Die)

Thermal Resistance — IGBT 10A60	$R_{\theta JC}$	—	1.94	2.43	°C/W
20A60		—	1.28	1.60	
Thermal Resistance — Free–Wheeling Diode 10A60	$R_{\theta JC}$	—	5.28	6.60	°C/W
20A60		—	2.61	3.26	

TYPICAL CHARACTERISTICS

(see also application information)

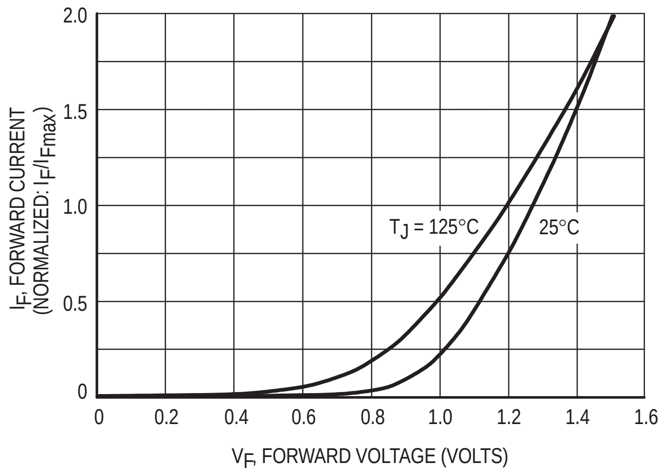


Figure 1. Forward Characteristics — Free–Wheeling Diode

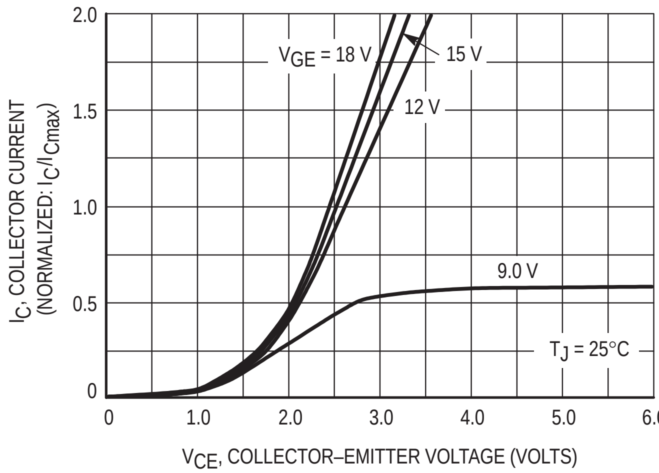


Figure 2. Forward Characteristics, T_J = 25°C

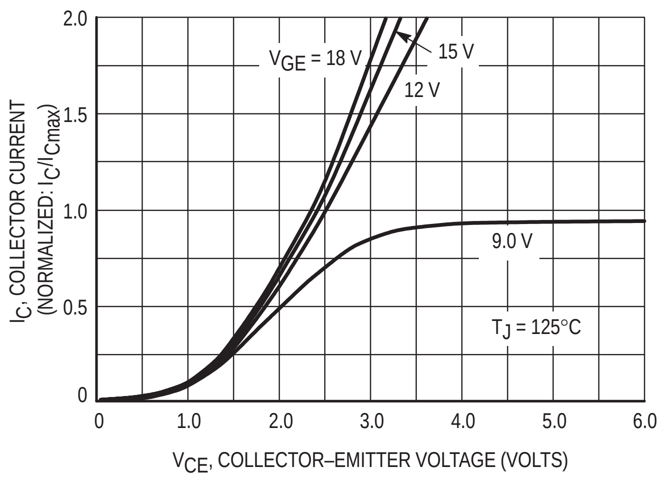


Figure 3. Forward Characteristics, T_J = 125°C

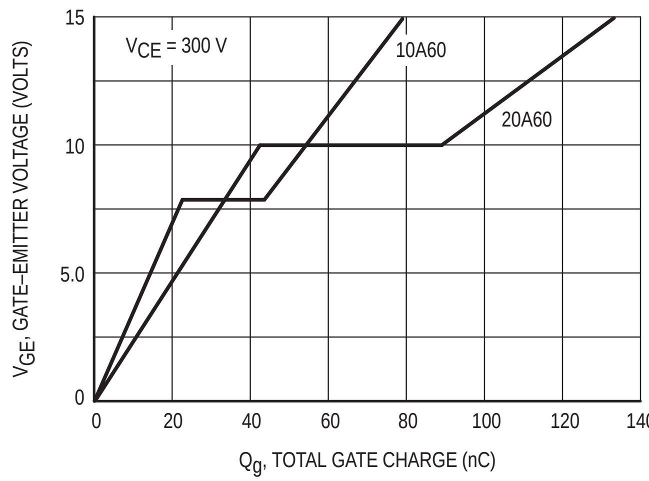


Figure 4. Gate–Emitter Voltage versus Total Gate Charge

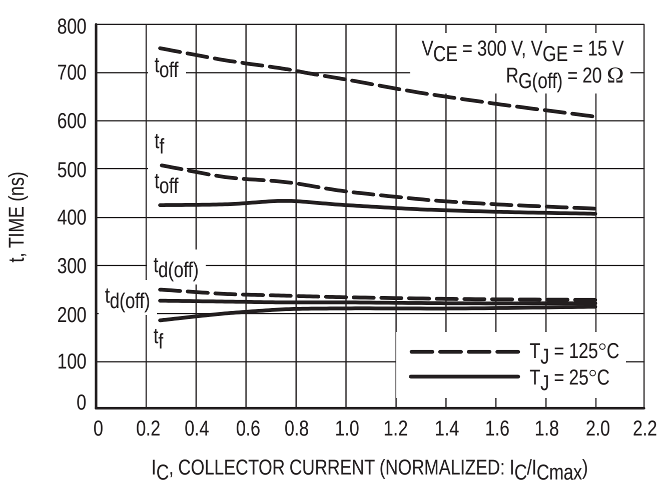


Figure 5. Inductive Switching Times versus Collector Current

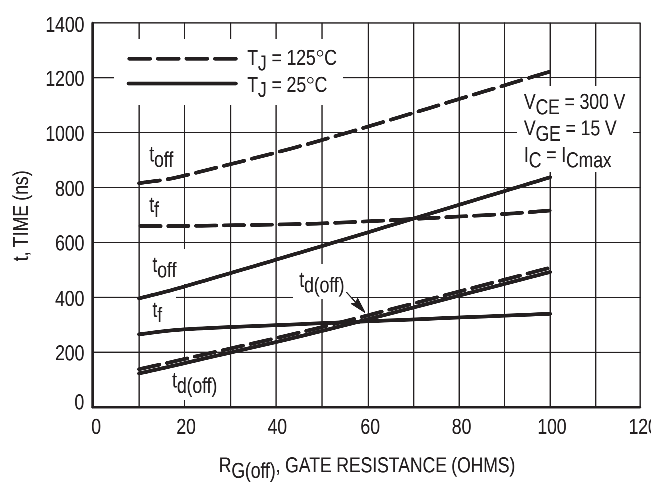


Figure 6. Inductive Switching Times versus Gate Resistance

TYPICAL CHARACTERISTICS

(see also application information)

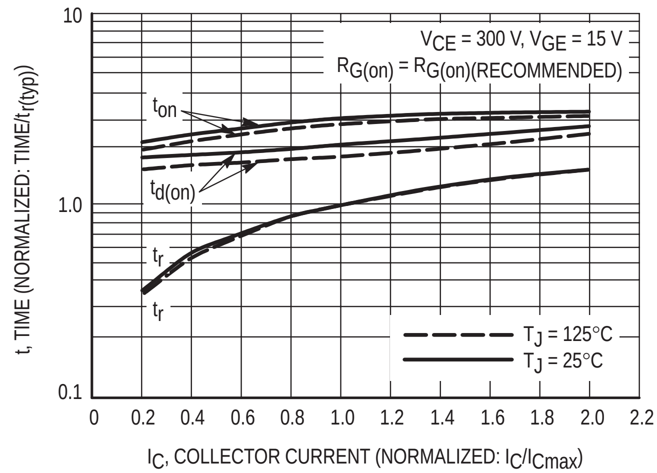


Figure 7. Inductive Switching Times versus Collector Current

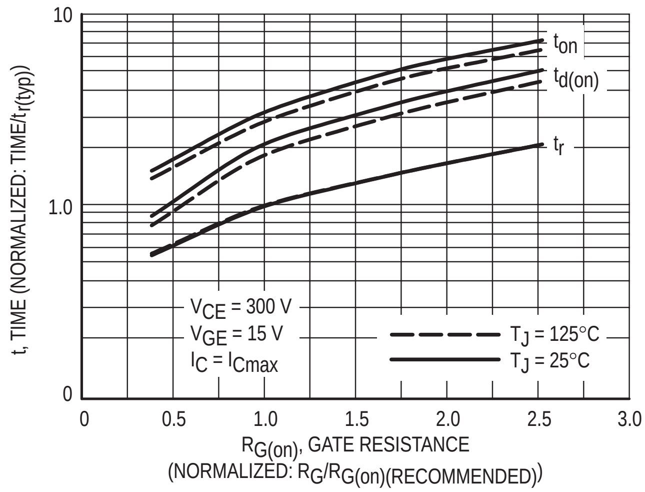


Figure 8. Inductive Switching Times versus Gate Resistance

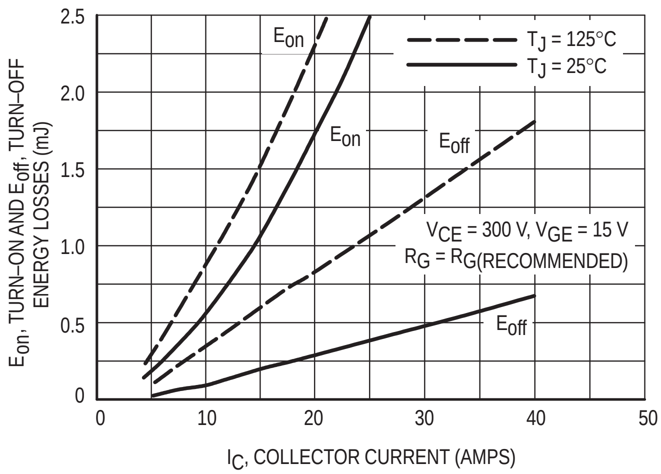


Figure 9. Turn–On and Turn–Off Energy Losses versus Collector Current

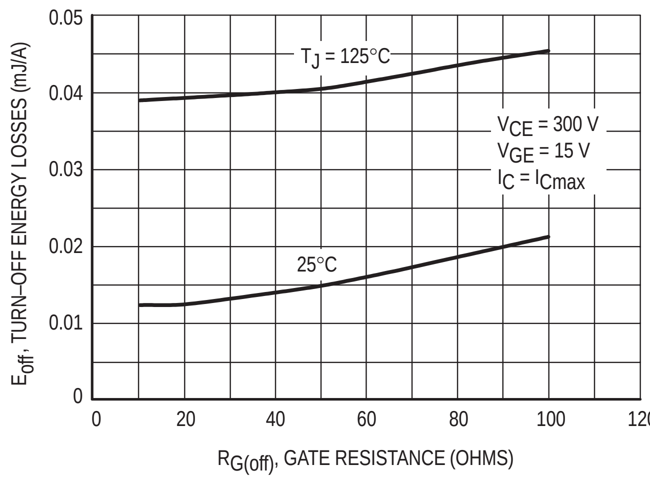


Figure 10. Turn–Off Energy Losses versus Gate Resistance

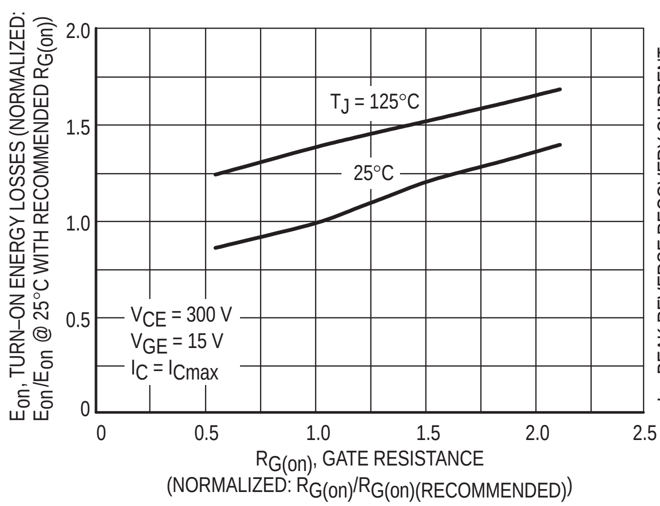


Figure 11. Turn–On Energy Losses versus Gate Resistance

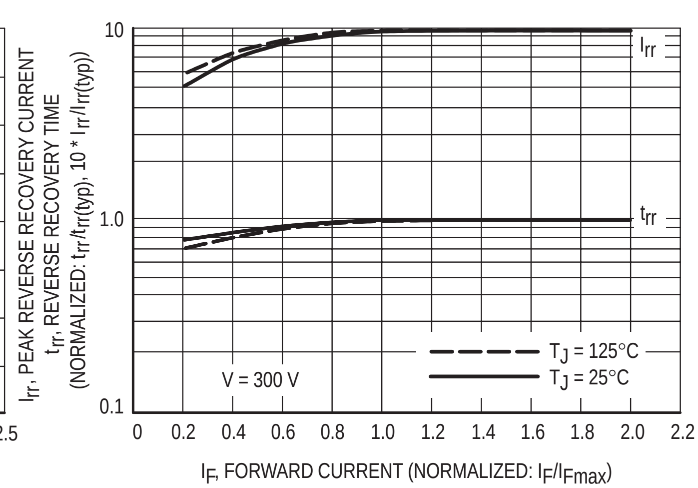


Figure 12. Reverse Recovery Characteristics — Free–Wheeling Diode

TYPICAL CHARACTERISTICS

(see also application information)

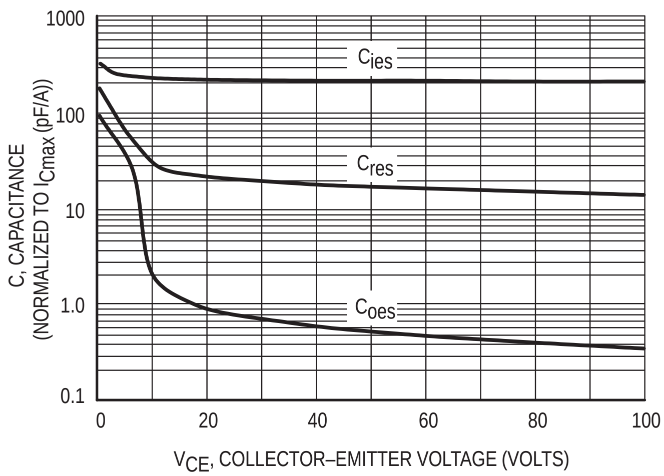


Figure 13. Capacitance Variation

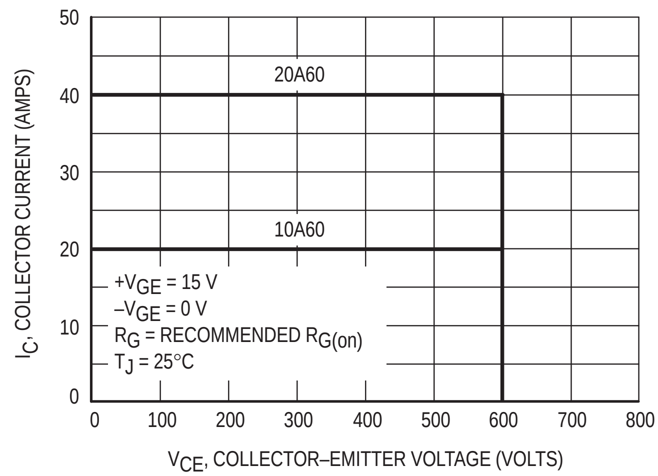


Figure 14. Reverse Biased Safe Operating Area (RBSOA)

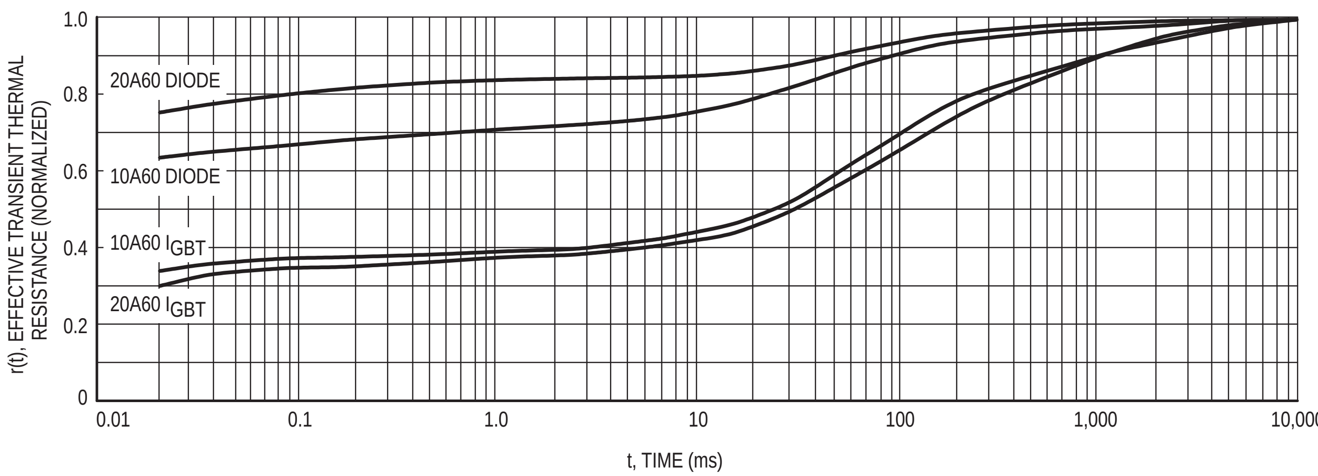


Figure 15. Thermal Response

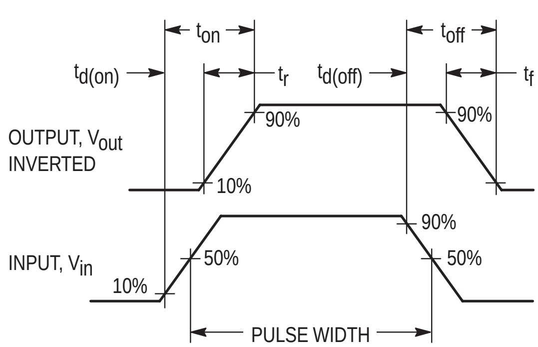


Figure 16. Switching Waveforms

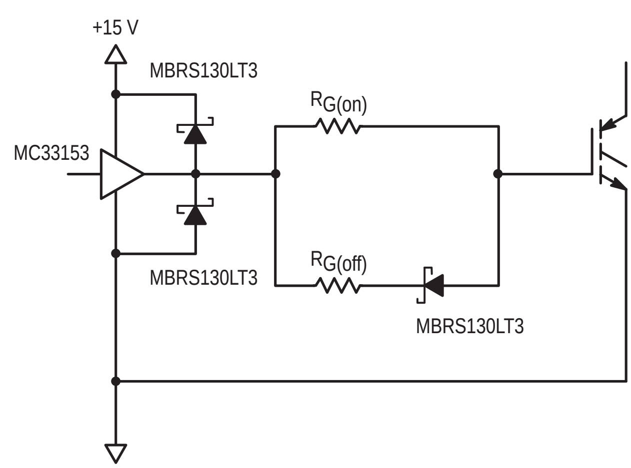


Figure 17. Recommended Gate Drive Circuit

APPLICATION INFORMATION

These modules are designed to be used as the power stage of a three–phase AC induction motor drive. They may be used for up to 230 VAC applications. Switching frequencies up to 10 kHz have been considered in the design.

Gate resistance recommendations have been listed. Separate turn–on and turn–off resistors are listed, to be used in a circuit resembling Figure 17. All switching characteristics are given based on following these recommendations, but appropriate graphs are shown for operation with different gate resistance. In order to equalize across the two different module ratings, a normalization process was used. Actual typical values are listed in the second section of this specification sheet, "Electrical Specifications," but many of the graphs are given in normalized units.

The first three graphs, the DC characteristics, are normalized for current. The devices are designed to operate the same at rated maximum current (10 and 20 A). The curves extend to $I_{C(pk)}$, the maximum allowable instantaneous current.

The next graph, turn–off times versus current, is again normalized to the rated maximum current. The following graph, turn–off times versus $R_{G(off)}$, is intentionally not normalized, as both modules behave similarly during turn–off.

Turn–on times have been normalized. Again, the graph showing variation due to current has been normalized for rated maximum current. The graph showing variation due to gate resistance normalizes against the recommended $R_{G(on)}$ for each module. In addition, the times are normalized to t_r at the appropriate temperature. For example, $t_{d(on)}$ for a 10 A module operating at 125°C at 4.0 A can be found by multiplying the typical t_r for a 10 A module at 125°C (160 ns) by the value shown on the graph at a normalized current of 0.4 (1.6) to get 256 ns. The most salient features demonstrated by these graphs are the general trends: rise time is a larger fraction of total turn–on time at 125°C, and in general, larger gate resistance results in slower switching.

Graphs of switching energies follow a similar structure. The first of these graphs, showing variation due to current, is not normalized, as any of these devices operating within its limits follows the same trend. E_{off} does not need to be normalized to show variation with $R_{G(off)}$, as both are specified with the same nominal resistance. E_{on}, however, has been appropriately normalized. Gate resistance has been normalized to the recommended $R_{G(on)}$. In order to show the effect of elevated temperature, all energies were normalized to E_{on} at 25°C using the recommended $R_{G(on)}$.

Reverse recovery characteristics are also normalized. I_F is normalized to rated maximum current. I_{rrm} is normalized so that at maximum current at either 25°C or 125°C, the graph indicates "10", while t_{rr} is normalized to be "1" at maximum current at either temperature.

Capacitance values are normalized for I_{Cmax}. Due to poor scaling, gate charge and thermal characteristics are shown separately for each module.

Many issues must be considered when doing PCB layout. Figure 19 shows the footprint of a module, allowing for reasonable tolerances. A polarizing post is provided near pin 1 to ensure that the module is properly inserted during final assembly. When laying out traces, two issues are of primary importance: current carrying capacity and voltage clearance. Many techniques may be used to maximize both, including using traces on both sides of the PCB to double total copper thickness, providing cut–outs in high–current traces near high–voltage pins, and even removing portions of the board to increase "over–the–surface" creapage distance. Some additional advantage may be gained by potting the entire board assembly in a good dielectric. Consult appropriate regulatory standards, such as UL 840, for more details on high–voltage creapage and clearance.

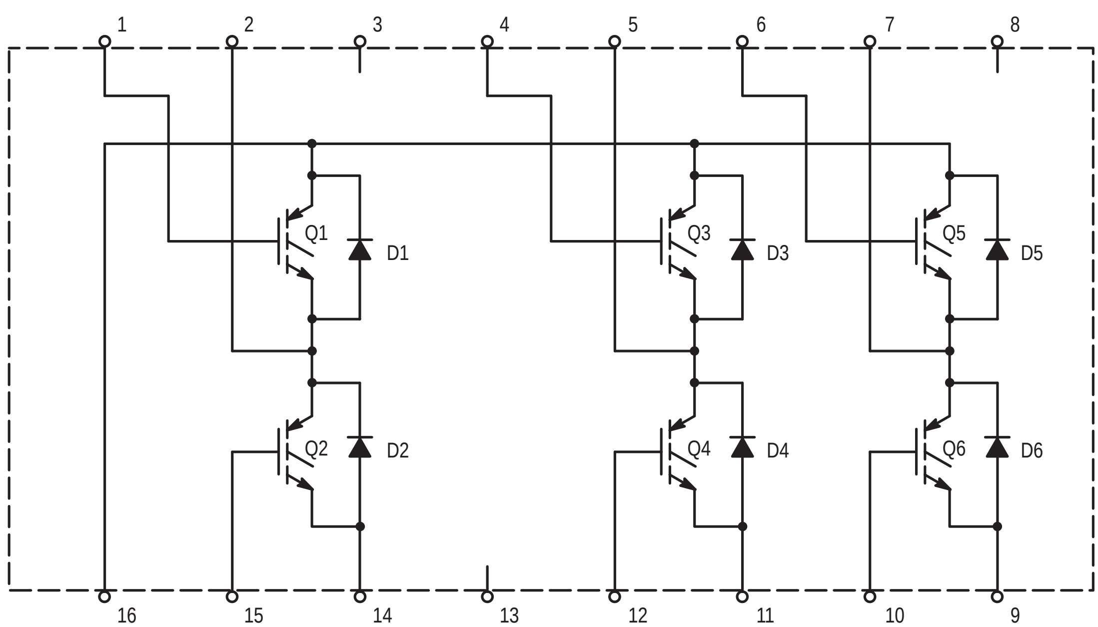


Figure 18. Schematic of Internal Circuit, Showing Package Pin–Out

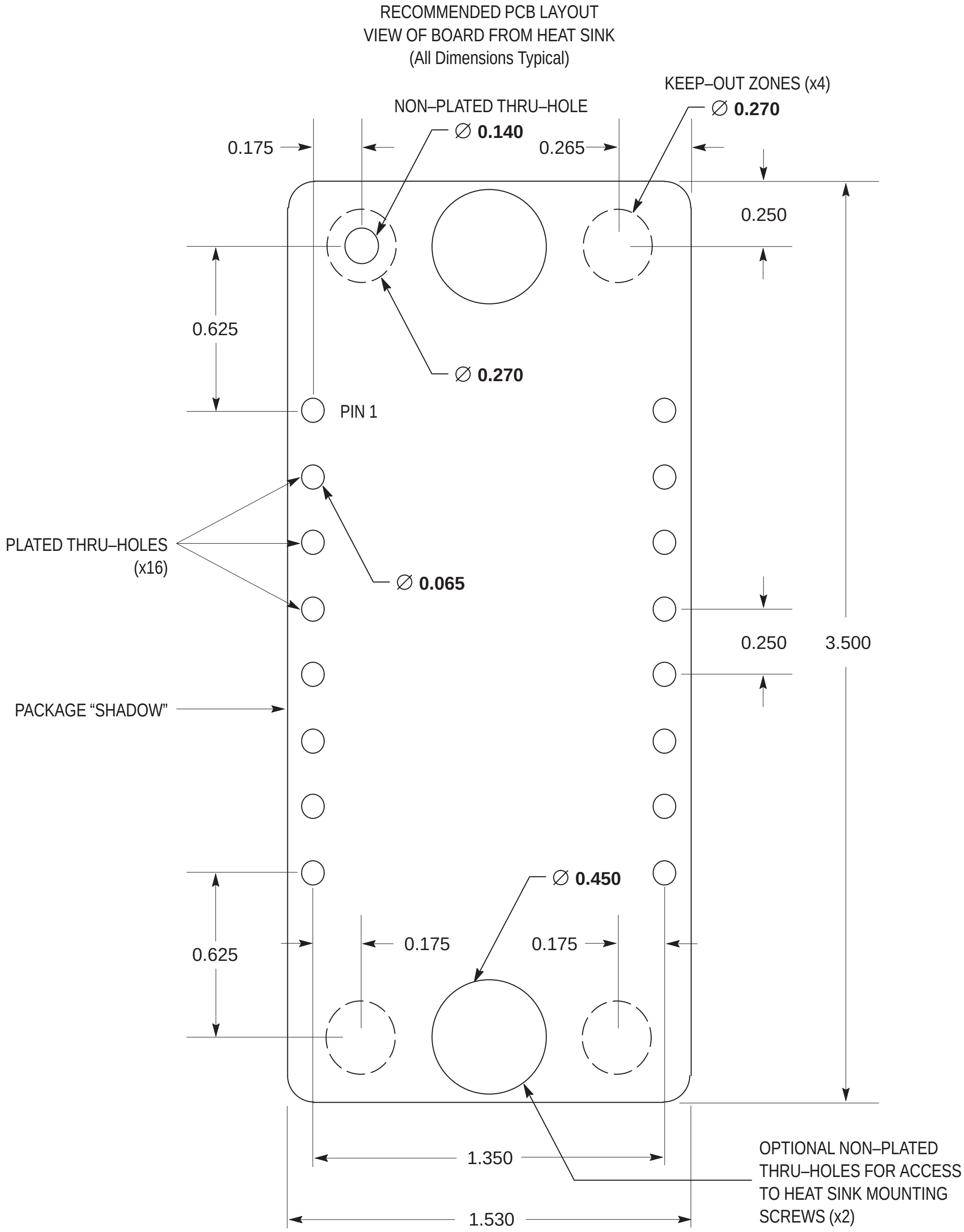


Figure 19. Package Footprint

NOTE:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates finished hole size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

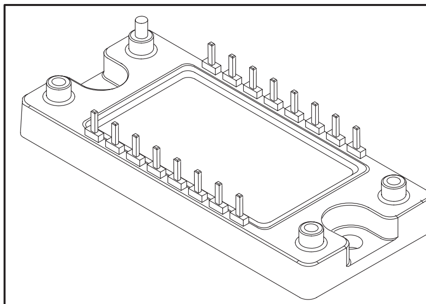
Hybrid Power Module

Integrated Power Stage for 460 VAC Motor Drives

MHPM6B5A120D
MHPM6B10A120D
MHPM6B15A120D

Motorola Preferred Devices

5.0, 10, 15 AMP, 1200 V
HYBRID POWER MODULES



CASE 464–03
ISSUE B

These VersaPower™ modules integrate a 3–phase inverter in a single convenient package. They are designed for 1.0, 2.0 and 3.0 hp motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimum performance. The top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 600 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- UL Recognized
- Visit our website at http://www.mot–sps.com/tsg/

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
IGBT Reverse Voltage		V_{CES}	1200	V
Gate-Emitter Voltage		V_{GES}	± 20	V
Continuous IGBT Collector Current	5A120 10A120 15A120	I_{Cmax}	5.0 10 15	A
Repetitive Peak IGBT Collector Current (1)	5A120 10A120 15A120	$I_{C(pk)}$	10 20 30	A
Continuous Free–Wheeling Diode Current	5A120 10A120 15A120	I_{Fmax}	5.0 10 15	A
Repetitive Peak Free–Wheeling Diode Current (1)	5A120 10A120 15A120	$I_{F(pk)}$	10 20 30	A
IGBT Power Dissipation per die (T_C = 25°C)	5A120 10A120 15A120	P_D	43 65 82	W
Diode Power Dissipation per die (T_C = 25°C)	5A120 10A120 15A120	P_D	19 38 38	W
IGBT Power Dissipation per die (T_C = 95°C)	5A120 10A120 15A120	P_D	19 29 36	W
Diode Power Dissipation per die (T_C = 95°C)	5A120 10A120 15A120	P_D	8.3 17 17	W
Junction Temperature Range		T_J	– 40 to +150	°C
Short Circuit Duration (V_{CE} = 600 V, T_J = 125°C)		t_{sc}	10	µs

(1) 1.0 ms = 1.0% duty cycle
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted) — continued

Rating	Symbol	Value	Unit
Isolation Voltage	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to +95	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes (#8 or M4 screws)	—	12	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS						
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)		I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 125°C		I_{CES}	—	6.0 2000	100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)		$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)		$V_{(BR)CES}$	1200	—	—	V
Collector-Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V) T_J = 125°C		$V_{CE(SAT)}$	— —	2.54 2.33	3.5 —	V
Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V) T_J = 125°C		V_F	— —	1.67 1.31	2.0 —	V
Input Capacitance (V_{CE} = 10 V, V_{GE} = 0 V, f = 1.0 Mhz)	5A120 10A120 15A120	C_{ies}	— — —	930 1840 2800	— — —	pF
Input Gate Charge (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	5A120 10A120 15A120	Q_T	— — —	31 65 100	— — —	nC
INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 25°C)						
Recommended Gate Resistor Turn–On Turn–Off	 5A120 10A120 15A120 	 $R_{G(on)}$ $R_{G(off)}$	 — — — —	 270 220 220 20	 — — — —	Ω
Turn-On Delay Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	$t_{d(on)}$	— — —	255 350 425	— — —	ns
Rise Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	t_r	— — —	140 250 225	— — —	ns
Turn–Off Delay Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)		$t_{d(off)}$	—	170	—	ns
Fall Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)		t_f	—	290	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	E_{on}	— — —	0.96 2.8 4.0	— — —	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	E_{off}	— — —	0.15 0.39 0.52	1.0 2.0 2.5	mJ
Diode Reverse Recovery Time (I_F = I_{Fmax}, V = 600 V, R_G as specified)	5A120 10A120 15A120	t_{rr}	— — —	130 170 165	— — —	ns

Characteristic		Symbol	Min	Typ	Max	Unit
INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 25°C) – continued						
Peak Reverse Recovery Current ($I_F = I_{Fmax}$, V = 600 V, R_G as specified)	5A120 10A120 15A120	I_{rrm}	— — —	5.0 6.0 9.6	— — —	A
Diode Stored Charge ($I_F = I_{Fmax}$, V = 600 V, R_G as specified)	5A120 10A120 15A120	Q_{rr}	— — —	335 575 860	— — —	nC
INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 125°C)						
Turn–On Delay Time (V_{CE} = 600 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	$t_{d(on)}$	— — —	230 315 375	— — —	ns
Rise Time (V_{CE} = 600 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	t_r	— — —	130 220 235	— — —	ns
Turn–Off Delay Time (V_{CE} = 600 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)		$t_{d(off)}$	—	176	—	ns
Fall Time (V_{CE} = 600 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)		t_f	—	676	—	ns
Turn–On Energy (V_{CE} = 600 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	E_{on}	— — —	1.3 3.9 5.5	— — —	mJ
Turn–Off Energy (V_{CE} = 600 V, $I_C = I_{Cmax}$, V_{GE} = 15 V, R_G as specified)	5A120 10A120 15A120	E_{off}	— — —	0.711 1.290 1.939	— — —	mJ
Diode Reverse Recovery Time ($I_F = I_{Fmax}$, V = 600 V, R_G as specified)	5A120 10A120 15A120	t_{rr}	— — —	190 375 310	— — —	ns
Peak Reverse Recovery Current ($I_F = I_{Fmax}$, V = 600 V, R_G as specified)	5A120 10A120 15A120	I_{rrm}	— — —	8.4 10 15	— — —	A
Diode Stored Charge ($I_F = I_{Fmax}$, V = 600 V, R_G as specified)	5A120 10A120 15A120	Q_{rr}	— — —	825 2100 2500	— — —	nC
THERMAL CHARACTERISTICS (Each Die)						
Thermal Resistance — IGBT	5A120 10A120 15A120	$R_{\theta JC}$	— — —	2.30 1.54 1.21	2.88 1.92 1.52	°C/W
Thermal Resistance — Free–Wheeling Diode	5A120 10A120 15A120	$R_{\theta JC}$	— — —	5.28 2.61 2.61	6.60 3.26 3.26	°C/W

TYPICAL CHARACTERISTICS

(see also application information)

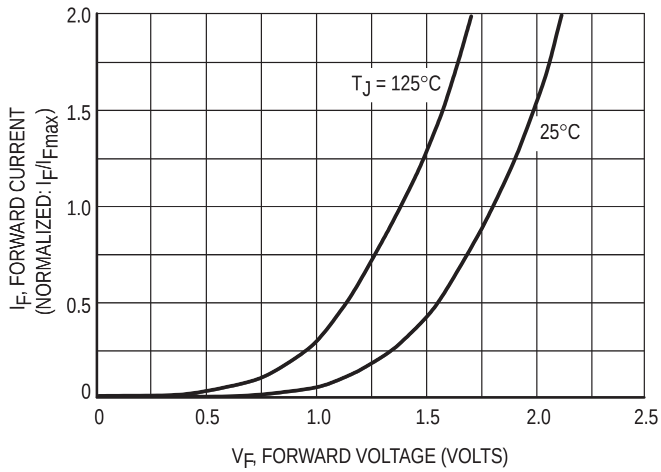


Figure 1. Forward Characteristics — Free–Wheeling Diode

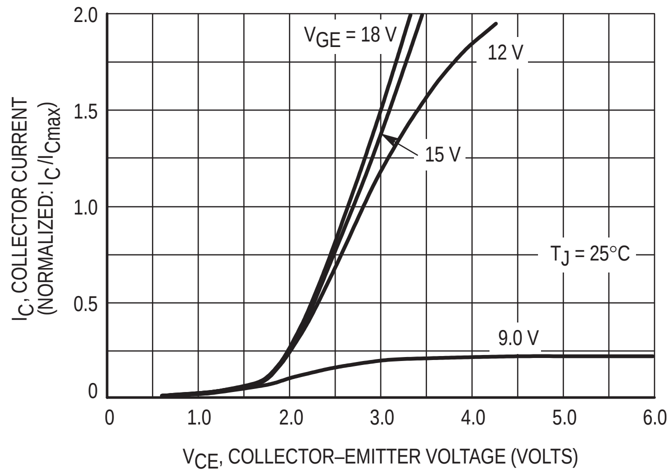


Figure 2. Forward Characteristics, T_J = 25°C

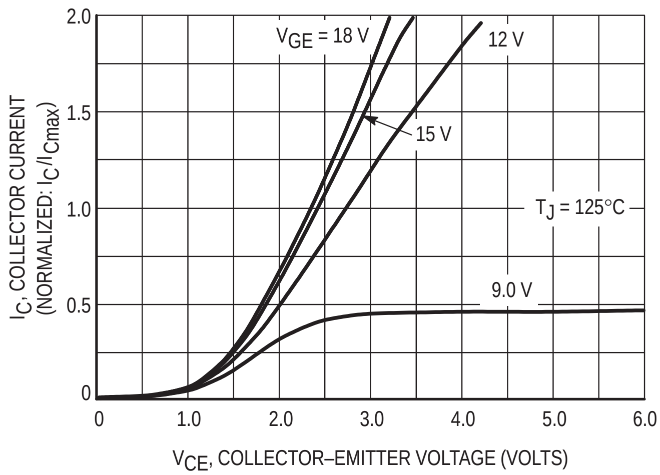


Figure 3. Forward Characteristics, T_J = 125°C

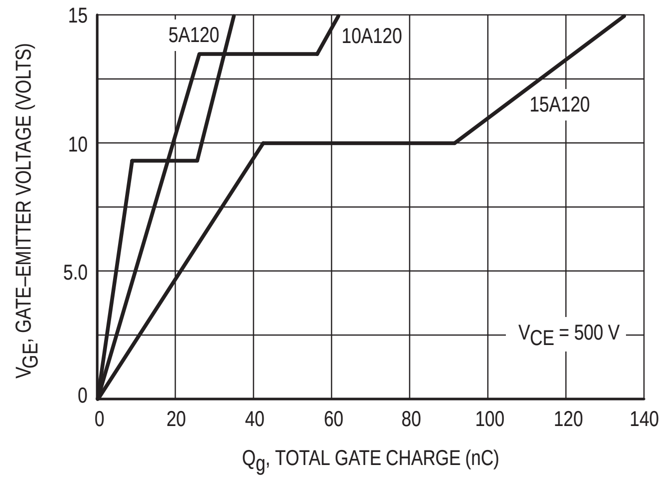


Figure 4. Gate–Emitter Voltage versus Total Gate Charge

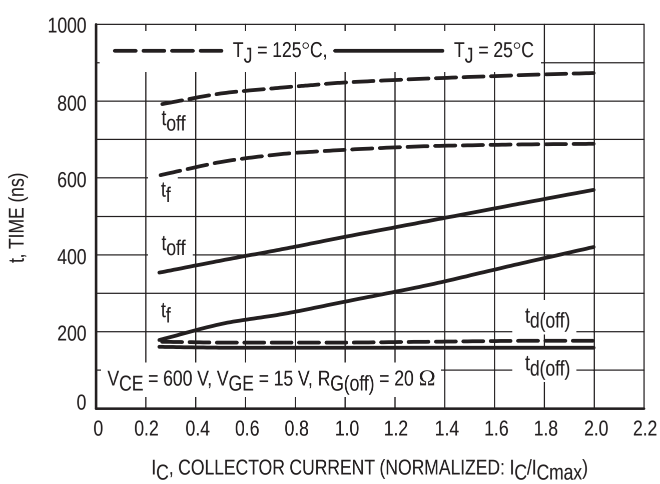


Figure 5. Inductive Switching Times versus Collector Current

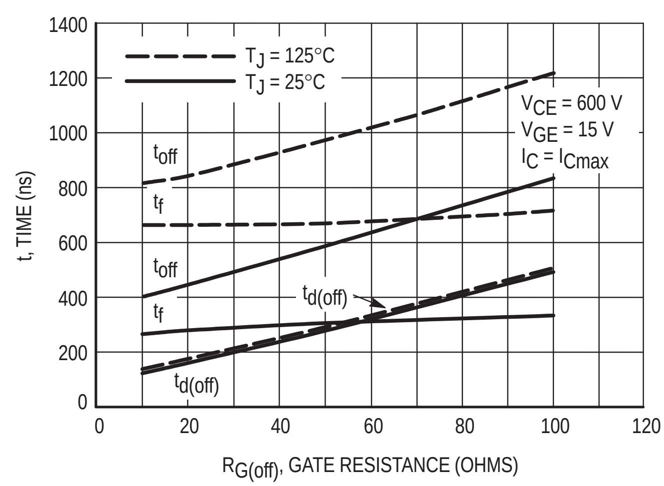


Figure 6. Inductive Switching Times versus Gate Resistance

TYPICAL CHARACTERISTICS

(see also application information)

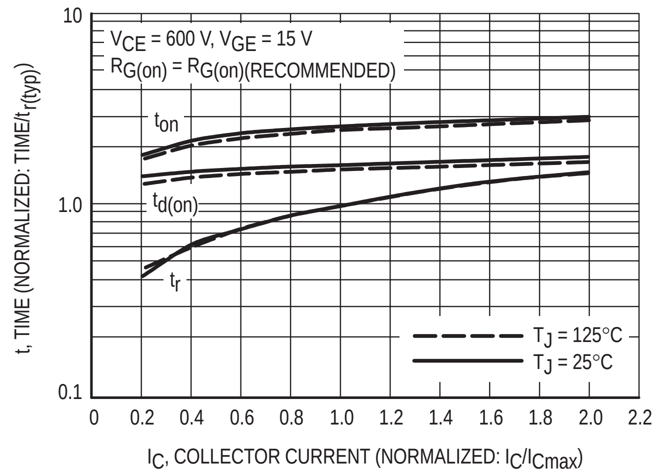


Figure 7. Inductive Switching Times versus Collector Current

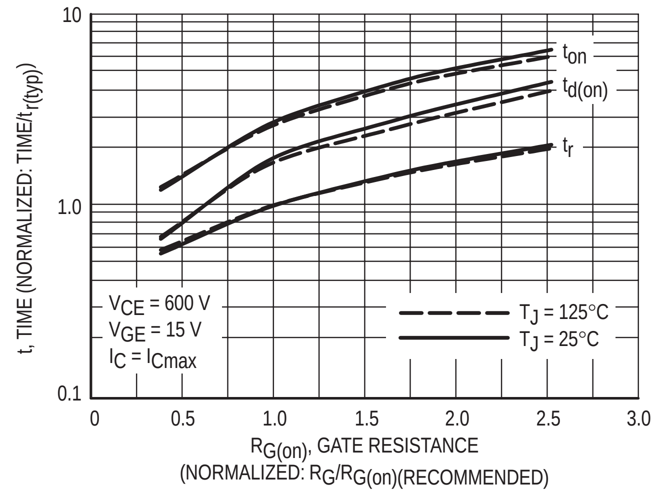


Figure 8. Inductive Switching Times versus Gate Resistance

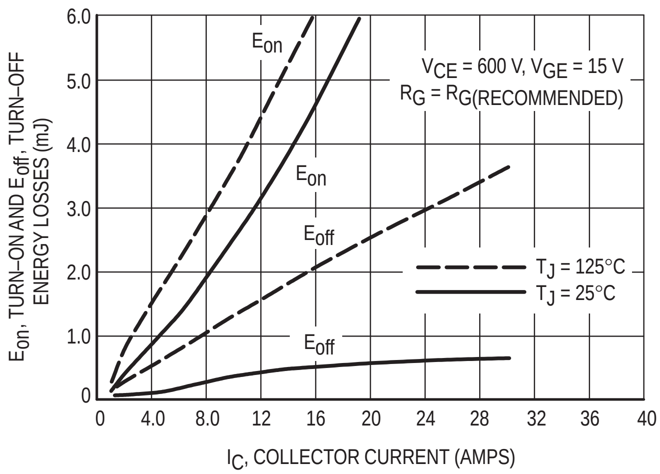


Figure 9. Turn–On and Turn–Off Energy Losses versus Collector Current

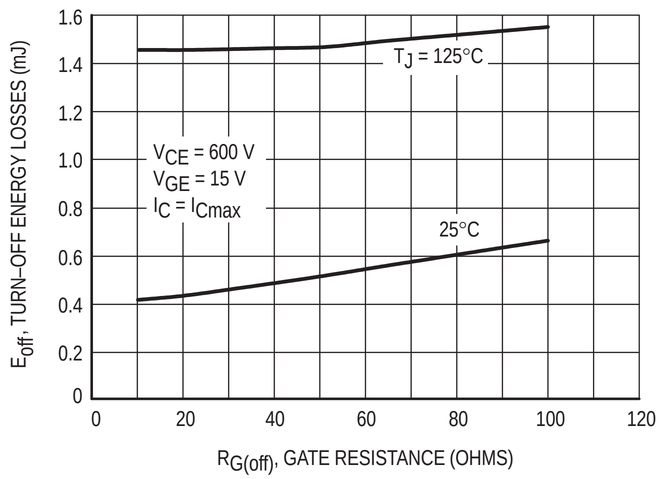


Figure 10. Turn–Off Energy Losses versus Gate Resistance

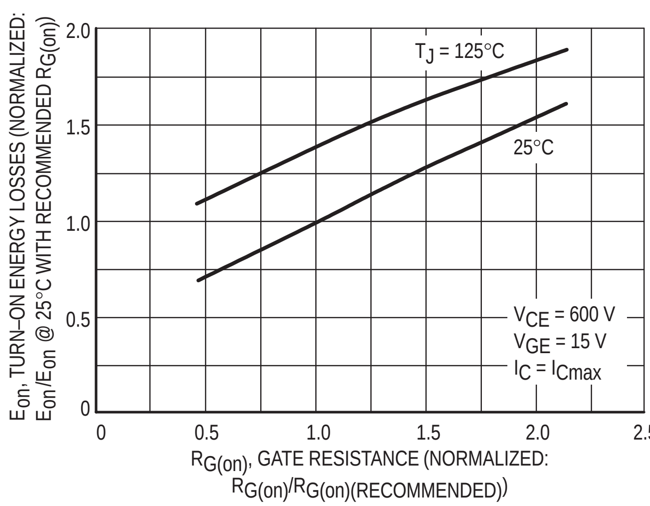


Figure 11. Turn–On Energy Losses versus Gate Resistance

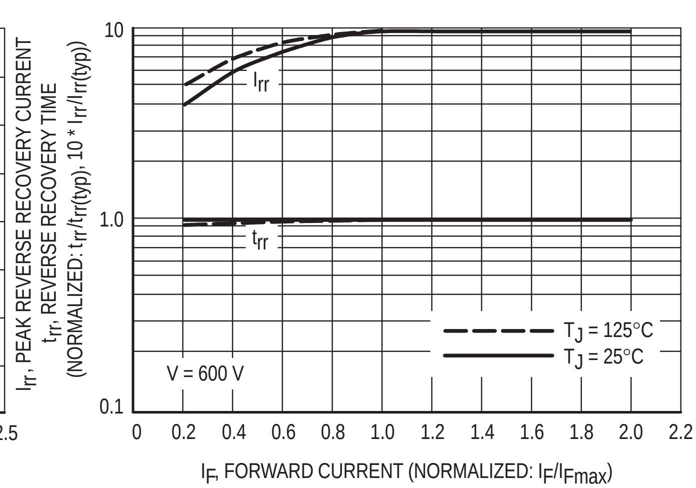
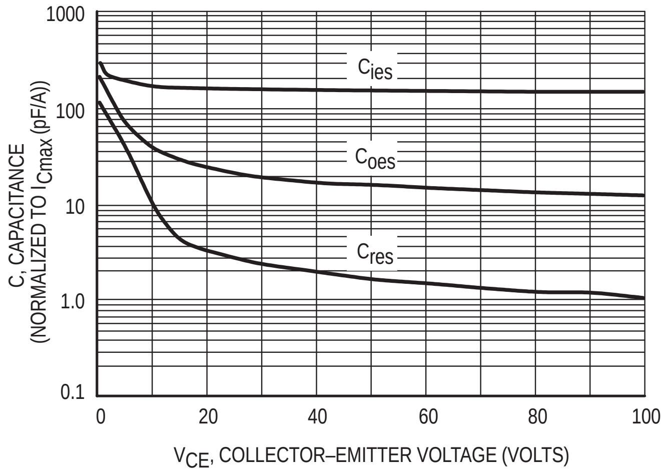


Figure 12. Reverse Recovery Characteristics — Free–Wheeling Diode

TYPICAL CHARACTERISTICS

(see also application information)



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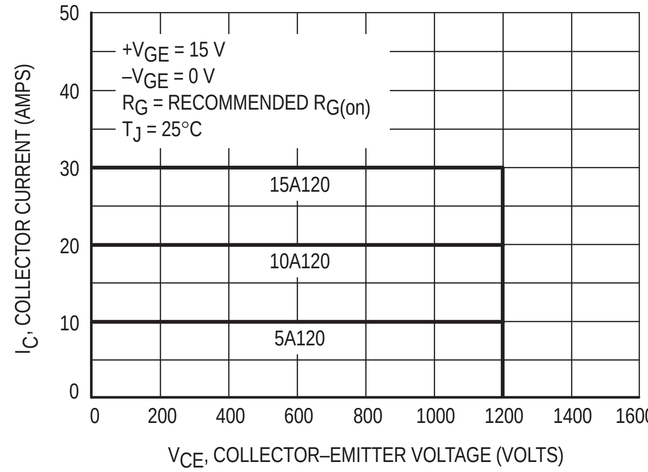


Figure 14. Reverse Biased Safe Operating Area (RBSOA)

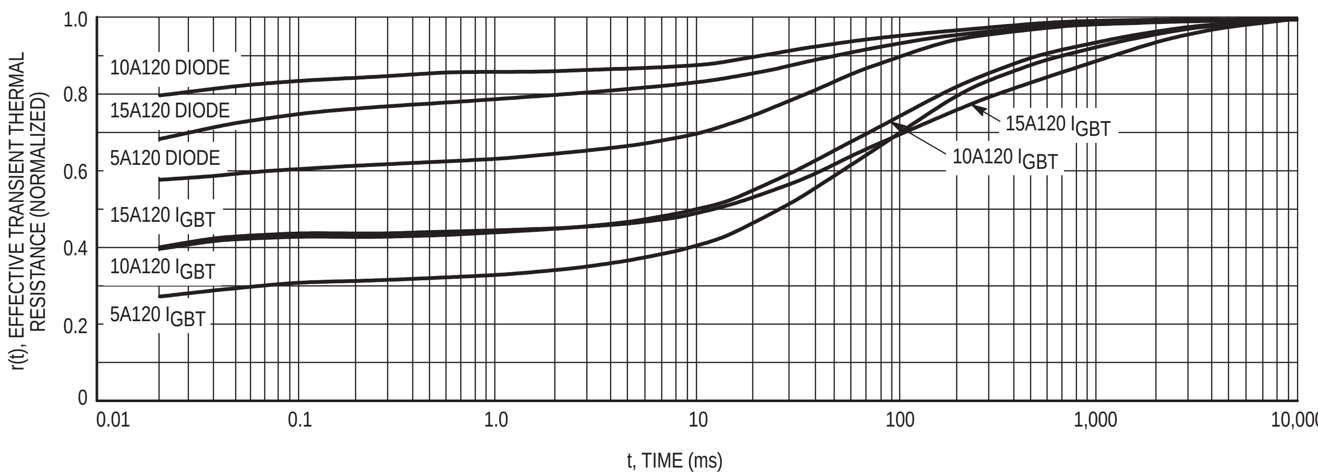


Figure 15. Thermal Response

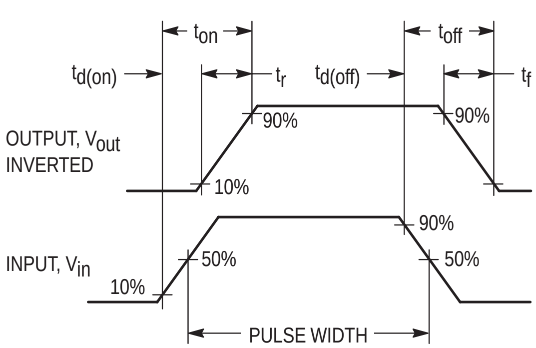


Figure 16. Switching Waveforms

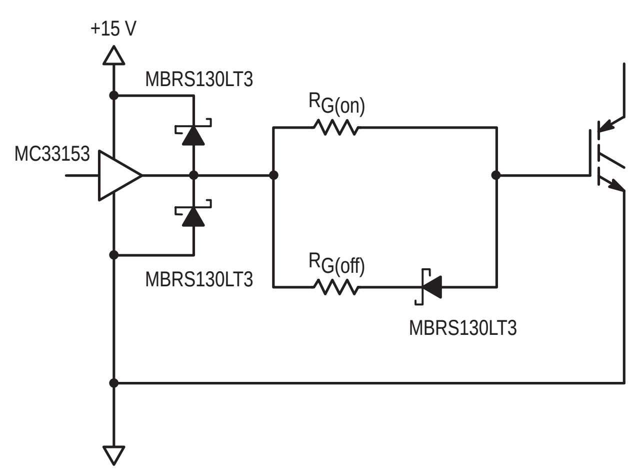


Figure 17. Recommended Gate Drive Circuit

APPLICATION INFORMATION

These modules are designed to be used as the power stage of a three–phase AC induction motor drive. They may be used for up to 460 VAC applications. Switching frequencies up to 10 kHz have been considered in the design.

Gate resistance recommendations have been listed. Separate turn–on and turn–off resistors are listed, to be used in a circuit resembling Figure 17. All switching characteristics are given based on following these recommendations, but appropriate graphs are shown for operation with different gate resistance. In order to equalize across the three different module ratings, a normalization process was used. Actual typical values are listed in the second section of this specification sheet, “Electrical Specifications,” but many of the graphs are given in normalized units.

The first three graphs, the DC characteristics, are normalized for current. The devices are designed to operate the same at rated maximum current (5.0, 10 and 15 A). The curves extend to $I_{C(pk)}$, the maximum allowable instantaneous current.

The next graph, turn–off times versus current, is again normalized to the rated maximum current. The following graph, turn–off times versus $R_{G(off)}$, is intentionally not normalized, as all three modules behave similarly during turn–off.

Turn–on times have been normalized. Again, the graph showing variation due to current has been normalized for rated maximum current. The graph showing variation due to gate resistance normalizes against the recommended $R_{G(on)}$ for each module. In addition, the times are normalized to t_r at the appropriate temperature. For example, $t_{d(on)}$ for a 10 A module operating at 125°C at 4.0 A can be found by multiplying the typical t_r for a 10 A module at 125°C (220 ns) by the value shown on the graph at a normalized current of 0.4 (1.4) to get 308 ns. The most salient features demonstrated by these graphs are the general trends: rise time is a larger fraction of total turn–on time at 125°C, and in general, larger gate resistance results in slower switching.

Graphs of switching energies follow a similar structure. The first of these graphs, showing variation due to current, is not normalized, as any of these devices operating within its limits follows the same trend. E_{off} does not need to be normalized to show variation with $R_{G(off)}$, as all three are specified with the same nominal resistance. E_{on}, however, has been appropriately normalized. Gate resistance has been normalized to the recommended $R_{G(on)}$. In order to show the effect of elevated temperature, all energies were normalized to E_{on} at 25°C using the recommended $R_{G(on)}$.

Reverse recovery characteristics are also normalized. I_F is normalized to rated maximum current. I_{rrm} is normalized so that at maximum current at either 25°C or 125°C, the graph indicates “10”, while t_{rr} is normalized to be “1” at maximum current at either temperature.

Capacitance values are normalized for I_{Cmax}. Due to poor scaling, gate charge and thermal characteristics are shown separately for each module.

Many issues must be considered when doing PCB layout. Figure 19 shows the footprint of a module, allowing for reasonable tolerances. A polarizing post is provided near pin 1 to ensure that the module is properly inserted during final assembly. When laying out traces, two issues are of primary importance: current carrying capacity and voltage clearance. Many techniques may be used to maximize both, including using traces on both sides of the PCB to double total copper thickness, providing cut–outs in high–current traces near high–voltage pins, and even removing portions of the board to increase “over–the–surface” creapage distance. Some additional advantage may be gained by potting the entire board assembly in a good dielectric. Consult appropriate regulatory standards, such as UL 840, for more details on high–voltage creapage and clearance.

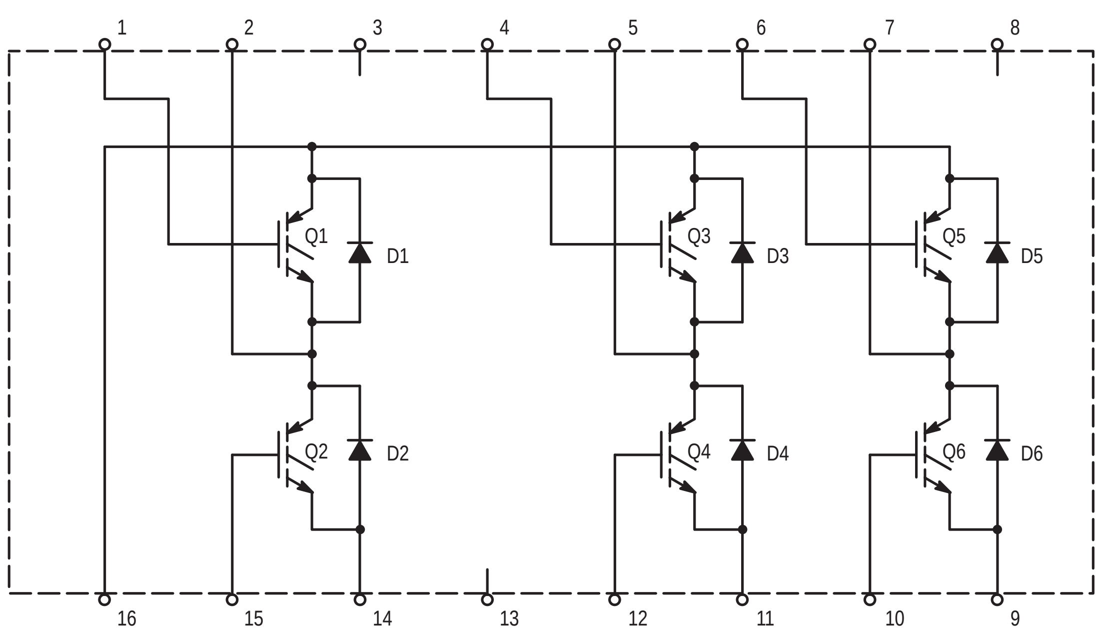


Figure 18. Schematic of Internal Circuit, Showing Package Pin–Out

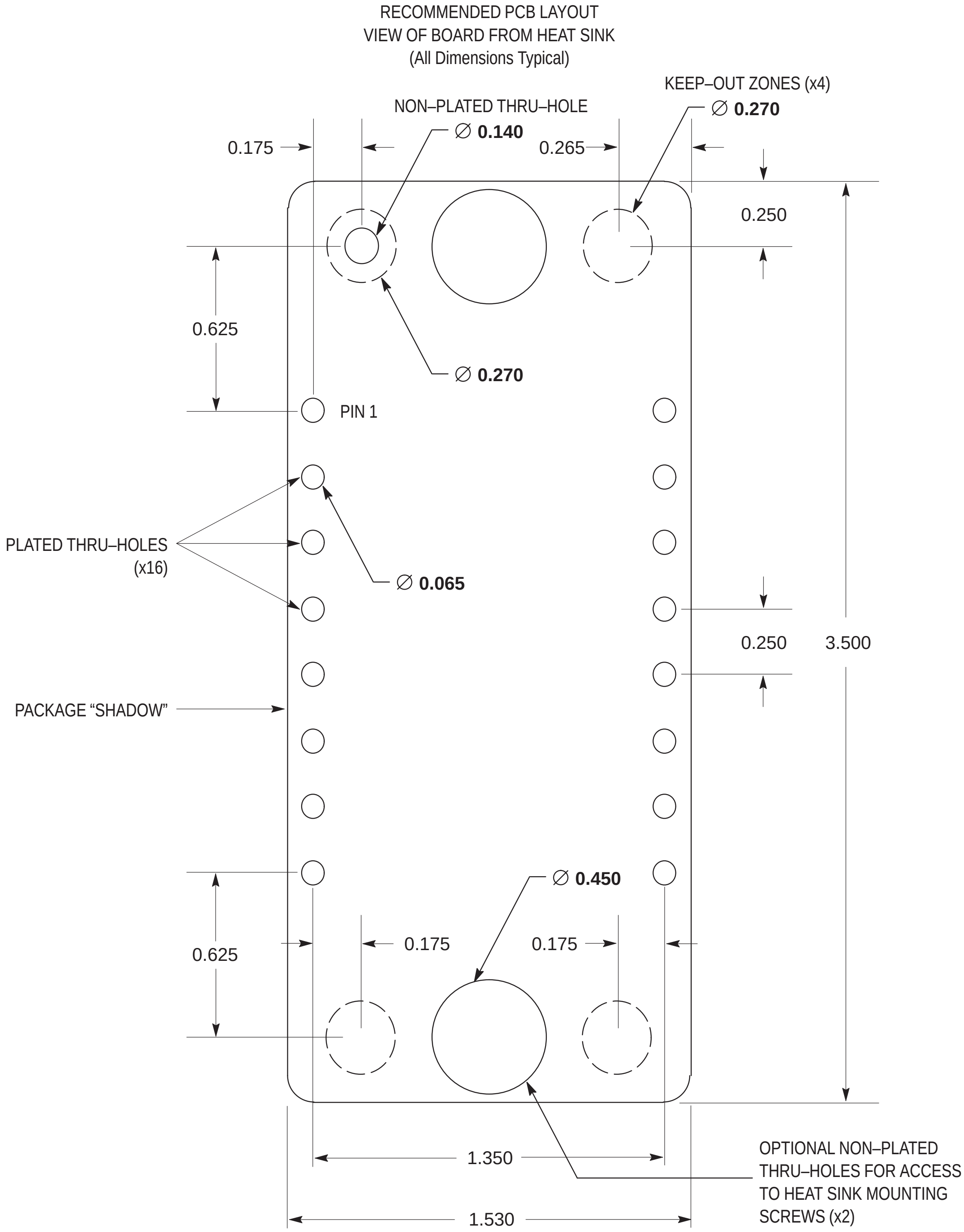


Figure 19. Package Footprint

NOTE:
1. Package is symmetrical, except for a polarizing plastic post near pin 1, indicated by a non–plated thru–hole in the footprint.
2. Dimension of plated thru–holes indicates net size after plating.
3. Access holes for mounting screws may or may not be necessary depending on assembly plan for finished product.

Hybrid Power Module

Integrated Power Stage for 460 VAC Motor Drives

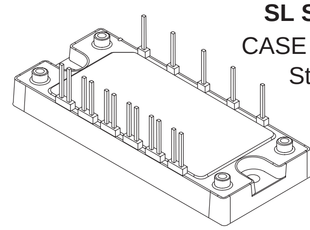
MHPM6B10N120
MHPM6B15N120
MHPM6B25N120
SERIES

Motorola Preferred Devices

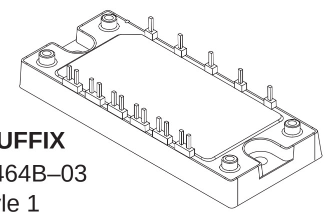
10, 15, 25 A, 1200 V
HYBRID POWER MODULES

These E–POWER™ modules integrate a 3–phase inverter in a single convenient package. They are designed for 2.0, 3.0, and 5.0 hp motor drive applications. The inverter incorporates advanced insulated gate bipolar transistors (IGBT) matched with fast soft free–wheeling diodes to give optimum performance. The top connector pins are designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 125°C, 720 V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Compact Package Outline
- Access to Positive and Negative DC Bus
- UL Recognized
- Visit our website at http://www.mot–sps.com/tsg/



SL SUFFIX
CASE 464A–02
Style 1



SS SUFFIX
CASE 464B–03
Style 1

ORDERING INFORMATION

Device	Current Rating	Package
MHPM6B10N120SL MHPM6B15N120SL MHPM6B25N120SL	10 15 25	464A–01 Style 1
MHPM6B10N120SS MHPM6B15N120SS MHPM6B25N120SS	10 15 25	464B–02 Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
IGBT Reverse Voltage		V_{CES}	1200	V
Gate-Emitter Voltage		V_{GES}	± 20	V
Continuous IGBT Collector Current (T_C = 80°C)	10A120 15A120 25A120	I_{Cmax}	10 15 25	A
Repetitive Peak IGBT Collector Current (1)	10A120 15A120 25A120	$I_{C(pk)}$	20 30 50	A
Continuous Diode Current (T_C = 25°C)	10A120 15A120 25A120	I_{Fmax}	10 15 25	A
Continuous Diode Current (T_C = 80°C)	10A120 15A120 25A120	I_{F80}	8.3 11 14	A
Repetitive Peak Diode Current (1)	10A120 15A120 25A120	$I_{F(pk)}$	20 30 50	A
IGBT Power Dissipation per die (T_C = 95°C)	10A120 15A120 25A120	P_D	41 50 65	W
Diode Power Dissipation per die (T_C = 95°C)	10A120 15A120 25A120	P_D	16 22 27	W

(1) 1.0 ms = 1.0% duty cycle
Preferred devices are Motorola recommended choices for future use and best overall value.

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Junction Temperature Range	T_J	– 40 to +150	°C
Short Circuit Duration (V_{CE} = 720 V, T_J = 125°C)	t_{sc}	10	µs
Isolation Voltage, Pin to Baseplate	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to +95	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque — Heat Sink Mounting Holes	—	1.4	Nm

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DC AND SMALL SIGNAL CHARACTERISTICS						
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)		I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V)		I_{CES}	—	5.0	100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)		$V_{GE(th)}$	5.0	6.0	7.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0 V)		$V_{(BR)CES}$	1200	—	—	V
Collector-Emitter Saturation Voltage (I_C = I_{Cmax}, V_{GE} = 15 V)		$V_{CE(SAT)}$	1.7	2.35	2.9	V
T_J = 125°C			—	2.69	—	
Forward Transconductance	10A120	g_{fe}	—	8.3	—	mho
	15A120		—	14	—	
	25A120		—	19	—	
Diode Forward Voltage (I_F = I_{Fmax}, V_{GE} = 0 V)		V_F	1.7	2.35	3.1	V
T_J = 125°C			—	1.9	—	
Input Capacitance (V_{CE} = 10 V, V_{GE} = 0 V, f = 1.0 MHz)	10A120	C_{ies}	—	1880	—	pF
	15A120		—	2620	—	
	25A120		—	4770	—	
Input Gate Charge (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120	Q_T	—	65	—	nC
	15A120		—	87	—	
	25A120		—	150	—	
INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 25°C)						
Recommended Gate Resistor ($R_{G(on)}$ = $R_{G(off)}$)		R_G				Ω
	10A120		—	82	—	
	15A120		—	82	—	
	25A120		—	68	—	
Turn-On Delay Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)		$t_{d(on)}$				ns
	10A120		—	174	—	
	15A120		—	240	—	
	25A120		—	330	—	
Rise Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)		t_r				ns
	10A120		—	84	—	
	15A120		—	105	—	
	25A120		—	150	—	
Turn–Off Delay Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)		$t_{d(off)}$				ns
	10A120		—	640	—	
	15A120		—	780	—	
	25A120		—	1060	—	
Fall Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)		t_f				ns
	10A120		—	39	47	
	15A120		—	48	58	
	25A120		—	70	84	
Turn-On Energy (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)		E_{on}				mJ
	10A120		—	1.5	1.8	
	15A120		—	2.7	3.3	
	25A120		—	4.6	5.6	

INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 25°C) – continued

Characteristic		Symbol	Min	Typ	Max	Unit
Turn-Off Energy (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	E_{off}	— — —	1.1 1.7 3.0	1.4 2.1 3.5	mJ
Diode Reverse Recovery Time (I_F = I_{Fmax}, V = 600 V)	10A120 15A120 25A120	t_{rr}	— — —	95 110 124	— — —	ns
Peak Reverse Recovery Current (I_F = I_{Fmax}, V = 600 V)	10A120 15A120 25A120	I_{rrm}	— — —	8.0 9.7 11.5	— — —	A
Diode Stored Charge (I_F = I_{Fmax}, V = 600 V)	10A120 15A120 25A120	Q_{rr}	— — —	550 600 740	— — —	nC

INDUCTIVE SWITCHING CHARACTERISTICS (T_J = 125°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Turn–On Delay Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	$t_{d(on)}$	— — —	160 220 310	— — —	ns
Rise Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	t_r	— — —	93 110 160	— — —	ns
Turn–Off Delay Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	$t_{d(off)}$	— — —	680 850 1140	— — —	ns
Fall Time (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	t_f	— — —	51 60 76	— — —	ns
Turn–On Energy (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	E_{on}	— — —	2.0 3.6 6.1	— — —	mJ
Turn–Off Energy (V_{CE} = 600 V, I_C = I_{Cmax}, V_{GE} = 15 V)	10A120 15A120 25A120	E_{off}	— — —	1.5 2.4 4.2	— — —	mJ
Diode Reverse Recovery Time (I_F = I_{Fmax}, V = 600 V)	10A120 15A120 25A120	t_{rr}	— — —	160 210 250	— — —	ns
Peak Reverse Recovery Current (I_F = I_{Fmax}, V = 600 V)	10A120 15A120 25A120	I_{rrm}	— — —	11.0 14.1 17.4	— — —	A
Diode Stored Charge (I_F = I_{Fmax}, V = 600 V)	10A120 15A120 25A120	Q_{rr}	— — —	995 1770 2460	— — —	nC

THERMAL CHARACTERISTICS (Each Die)

Characteristic		Symbol	Min	Typ	Max	Unit
Thermal Resistance — IGBT	10A120 15A120 25A120	$R_{\theta JC}$	— — —	1.1 0.89 0.68	1.3 1.1 0.85	°C/W
Thermal Resistance — Diode	10A120 15A120 25A120	$R_{\theta JC}$	— — —	2.8 2.0 1.6	3.5 2.5 2.0	°C/W

TYPICAL CHARACTERISTICS

(see also application information)

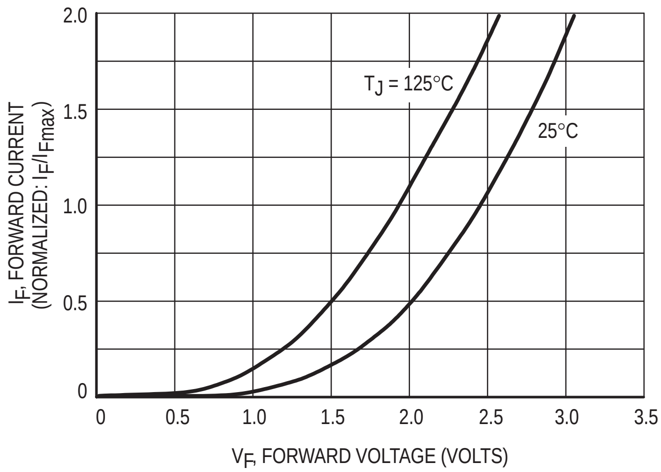


Figure 1. Forward Characteristics — Free–Wheeling Diode

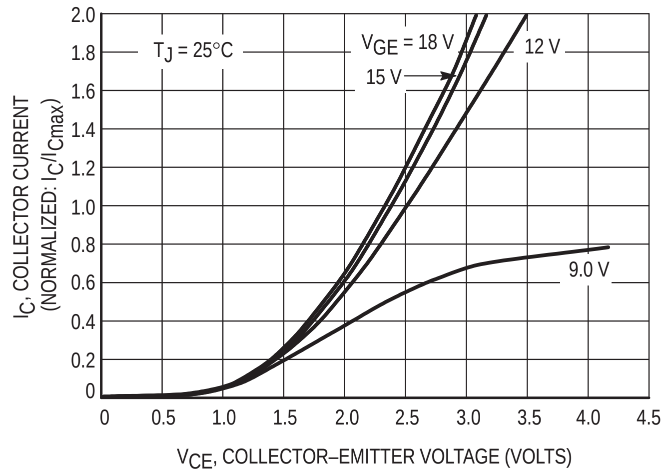


Figure 2. Forward Characteristics, T_J = 25°C

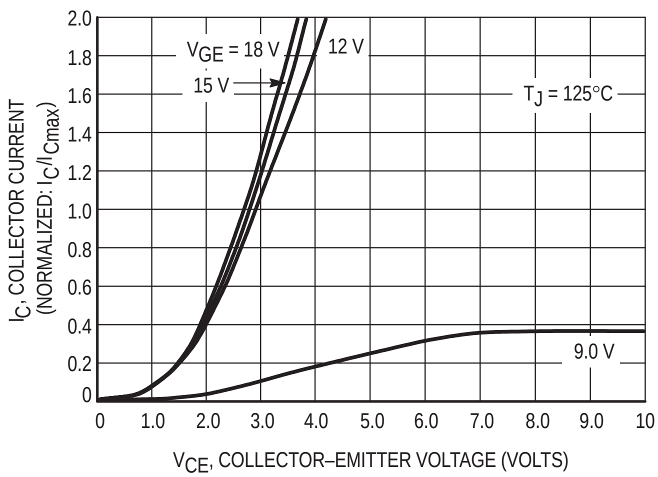


Figure 3. Forward Characteristics, T_J = 125°C

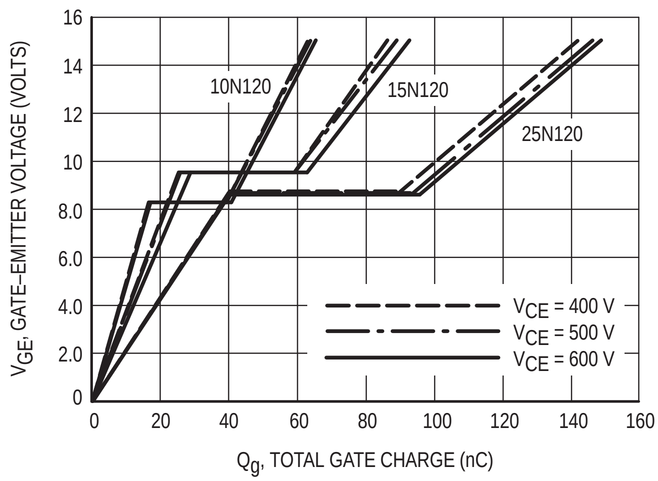


Figure 4. Gate–Emitter Voltage versus Total Gate Charge

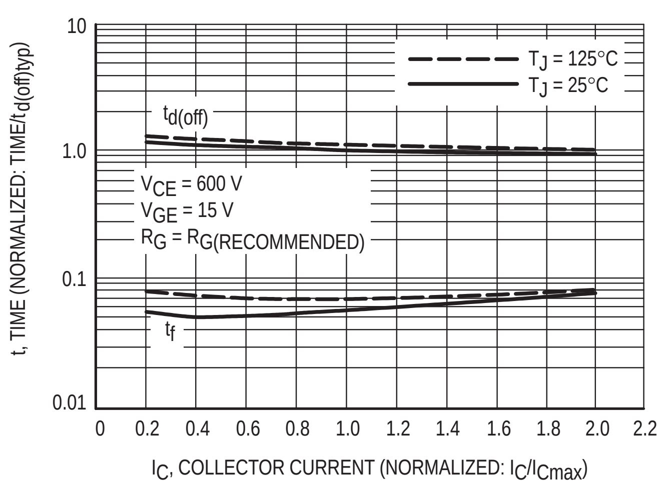


Figure 5. Inductive Switching Times versus Collector Current

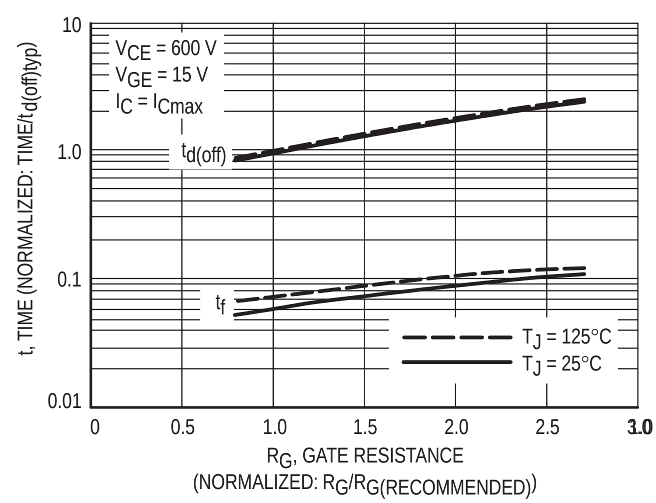


Figure 6. Inductive Switching Times versus Gate Resistance

TYPICAL CHARACTERISTICS

(see also application information)

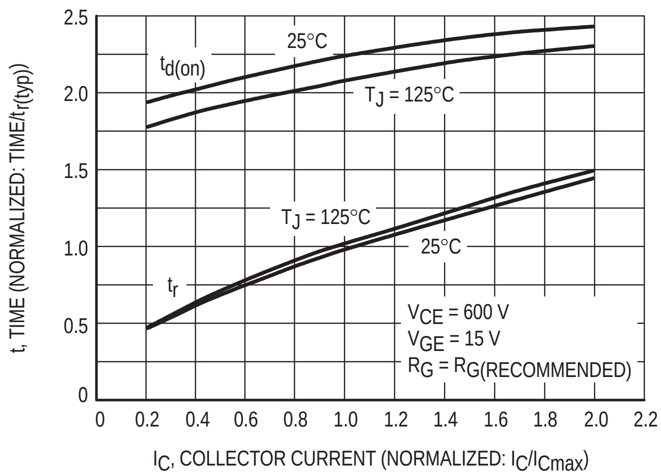


Figure 7. Inductive Switching Times versus Collector Current

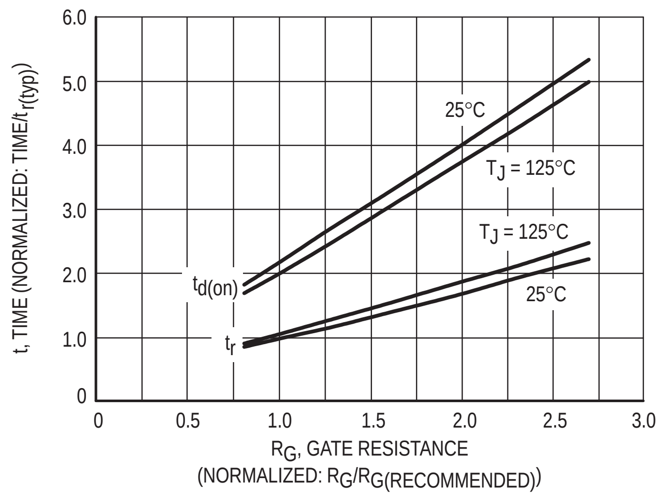


Figure 8. Inductive Switching Times versus Gate Resistance

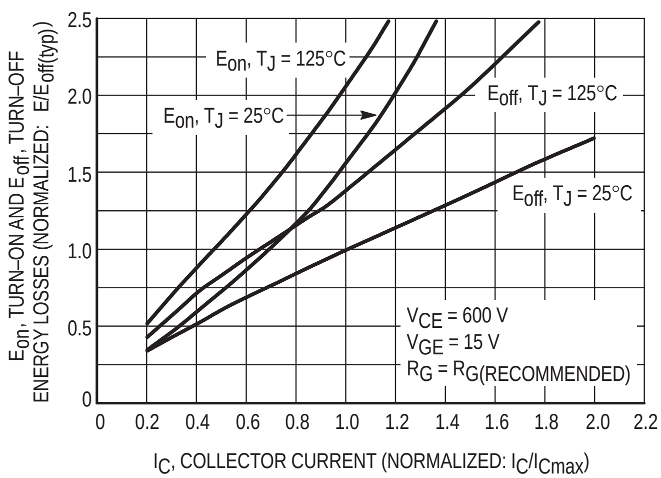


Figure 9. Turn–On and Turn–Off Energy Losses versus Collector Current

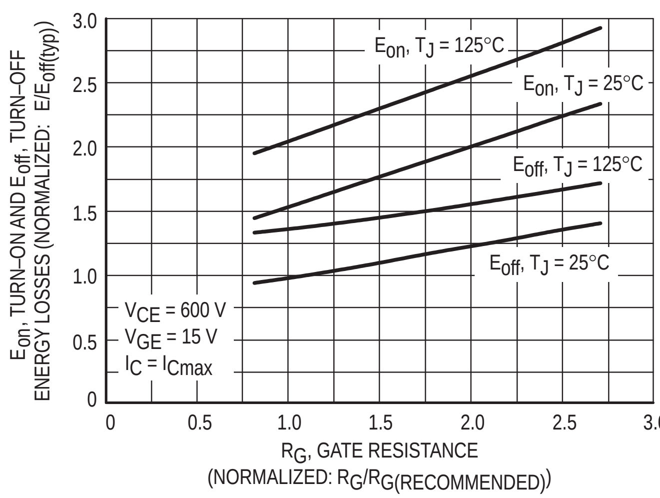


Figure 10. Turn–On and Turn–Off Energy Losses versus Gate Resistance

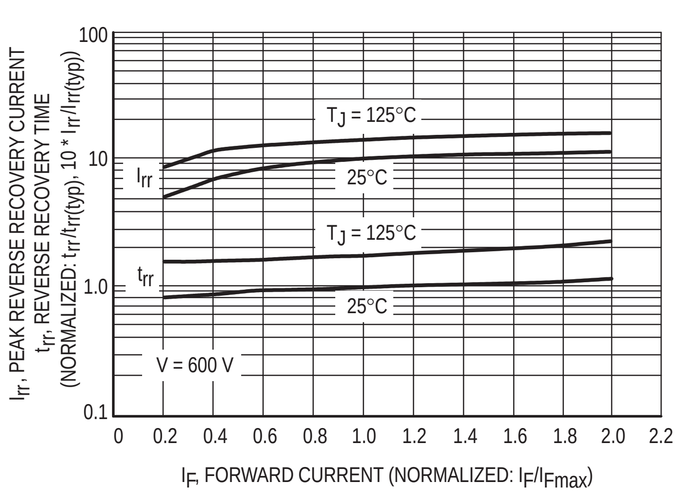


Figure 11. Reverse Recovery Characteristics — Free–Wheeling Diode

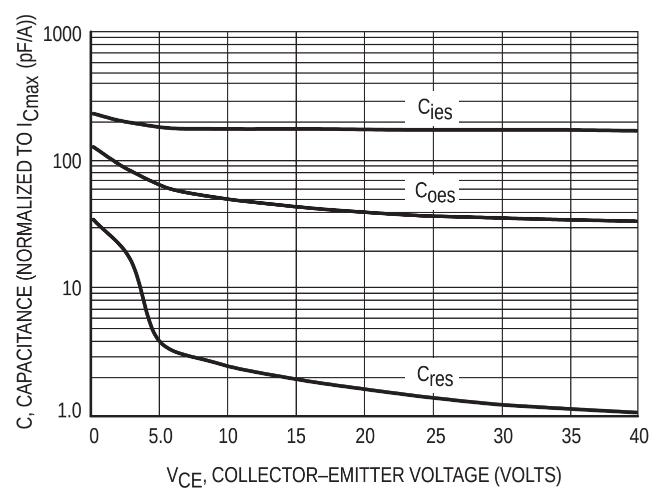


Figure 12. Capacitance Variation

TYPICAL CHARACTERISTICS

(see also application information)

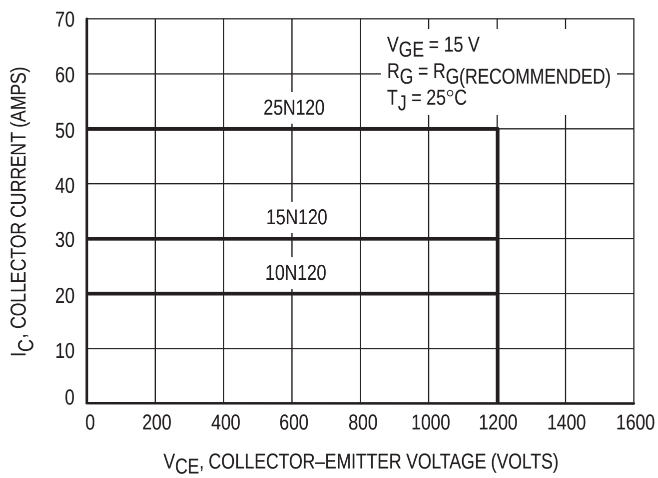


Figure 13. Reverse Biased Safe Operating Area (RBSOA)

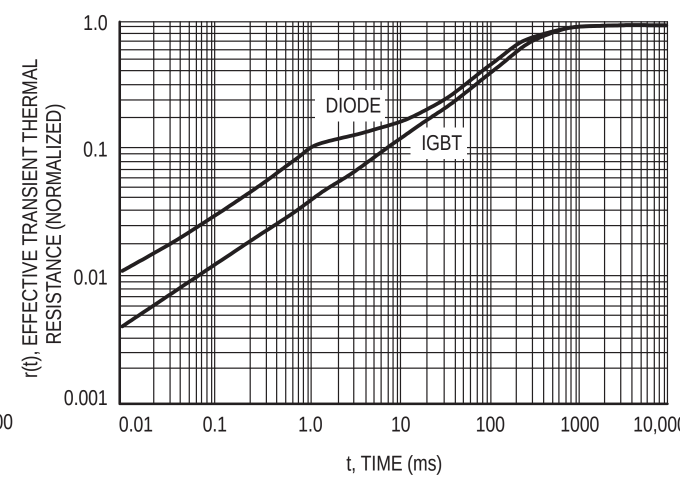


Figure 14. Thermal Response

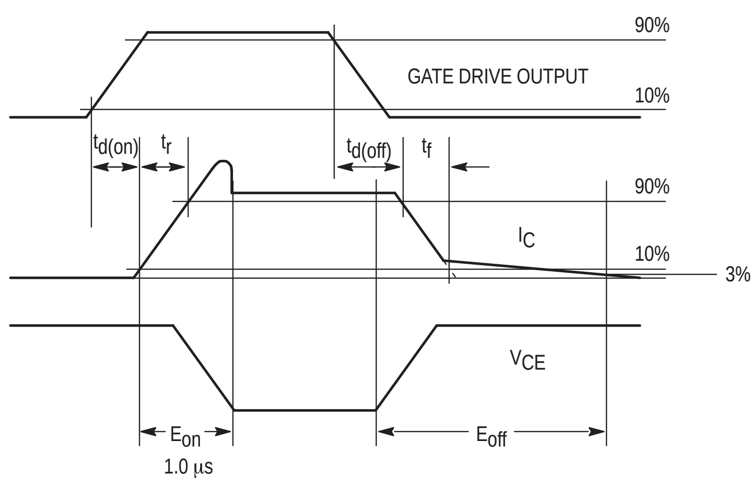


Figure 15. Timing Definitions

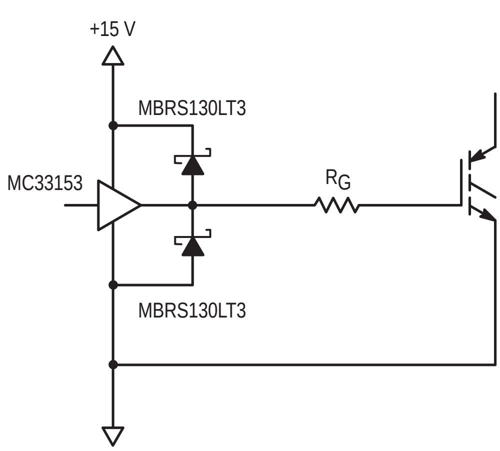


Figure 16. Common Gate Drive Circuit

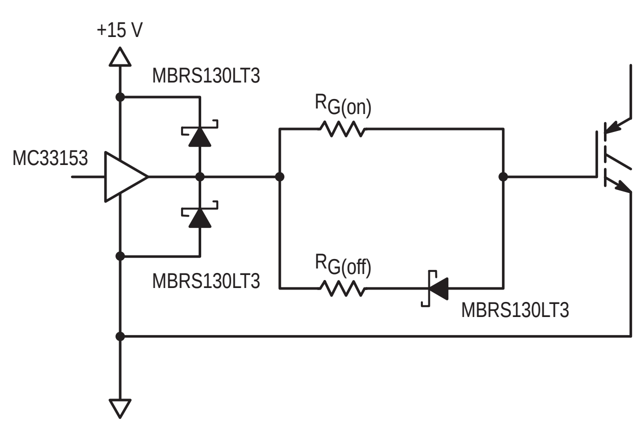


Figure 17. Recommended Gate Drive Circuit

APPLICATION INFORMATION

These modules are designed to be used as the power stage of a three–phase AC induction motor drive. They may be used for up to 460 VAC applications. Switching frequencies up to 15 kHz were considered in the design.

Gate resistance recommendations have been listed. These choices were based on the common gate drive circuit shown in Figure 16. However, significant improvements in E_{off} may be gained by either of two methods: use of a negative gate bias, or use of the gate drive shown in Figure 17. Separate turn–on and turn–off gate resistors give the best results; in this case, $R_{G(off)}$ should be chosen as small as possible while limiting current to prevent damage to the gate drive IC. Designers should also note that turn–on and turn–off delay times are measured from the rising and falling edges of the gate drive output, not the gate voltage waveform.

Since all three modules use similar technology, most of the graphs showing typical performance have been normalized. Actual values are listed for each size in the table, “Electrical Characteristics.” Data on the graphs reflect performance using the common gate drive circuit shown in Figure 16.

The first three curves, showing DC characteristics, are normalized for I_{Cmax}. The devices all perform similarly at rated current. The curves extend to $I_{C(pk)}$, the maximum allowable instantaneous current.

The next two graphs, turn–off and turn–on times versus I_C, are also normalized for I_{Cmax}. In addition, the time scales are normalized. Turn–off times are normalized to $t_{d(off)}$ at 25°C at rated current with recommended R_G, while turn–on times are normalized to t_r at 25°C at rated current with recommended R_G.

The graphs showing switching times as a function of R_G are similarly normalized. R_G has been normalized to the recommended value listed under “Electrical Characteristics.” The time axes are normalized exactly as for the corresponding graphs showing variation with I_C.

Similar transformations have been made for the next two figures, showing E_{on} and E_{off}. Energies have been normalized to E_{off} at 25°C at I_{Cmax} with the recommended R_G. I_C has been normalized to I_{Cmax}, and R_G has been normalized to the recommended value.

Reverse recovery characteristics are also normalized. I_C has again been normalized to I_{Cmax}. Reverse recovery time t_{rr} has been normalized to t_{rr} at 25°C at I_{Cmax}. Peak reverse recovery current I_{rrm} has been normalized to I_{rrm} at 25°C at I_{Cmax}, then multiplied by 10.

Capacitance has been normalized to device rated I_{Cmax}. Since all modules are rated for the same voltage, the voltage scale on Figure 11 does not need to be normalized.

Typical transient thermal impedance is shown for a diode and for an IGBT. All diodes behave quite similarly, as do all IGBTs.

The last two graphs, V_{GE} versus Q_G and RBSOA, are not normalized.

Many issues beyond the ratings must be considered in a system design. Dynamic characteristics can all be affected by external circuit parameters. For example, excessive bus inductance can dramatically increase voltage overshoot during switching, increasing the switching energy. The choice of gate drive IC can have quite a large effect on rise and fall times, corresponding to differences in switching energies. In many cases, this can be compensated by simply changing the gate resistor accordingly — a gate driver with a lower drive capability requires a smaller gate resistor. Ultimately, the module must be tested in the final system to characterize its performance.

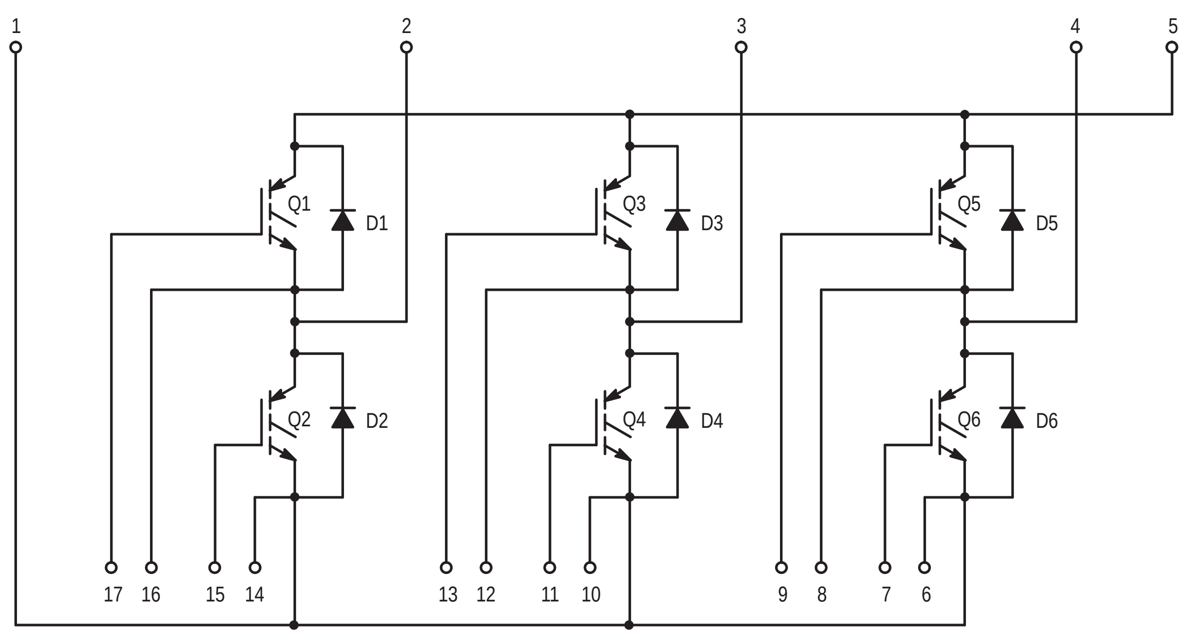


Figure 18. Schematic of Module, Showing Pin–Out

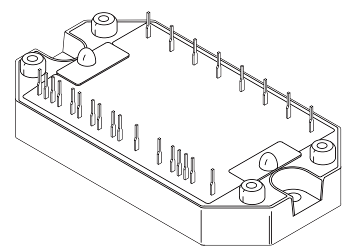
Hybrid Power Module

Integrated Power Stage for 1.0 hp Motor Drives

(This device is not recommended for new designs)
(This device is replaced by MHPM7A10E60DC3)

MHPM7A15A60A

15 AMP, 600 VOLT
HYBRID POWER MODULE



PLASTIC PACKAGE
CASE 440-02, Style 1

The MHPM7A15A60A module integrates a 3-phase input rectifier bridge, 3-phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package.The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free-wheeling diodes to give optimal dynamic performance. It has been configured for use as a three-phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 300 V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Average Output Rectified Current	I_O	15	A
Peak Non-repetitive Surge Current (1/2 Cycle) (1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	15	A
Peak Repetitive IGBT Collector Current (2)	$I_{C(pk)}$	30	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	15	A
Peak Repetitive Free-Wheeling Diode Current (2)	$I_{F(pk)}$	30	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	55	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	30	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 300 V, T_J = 25°C)	t_{sc}	10	µs

NOTE:
4. 1 cycle = 50 or 60 Hz
5. 1.0 ms = 1.0% duty cycle

REV 3

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	15	A
Peak Repetitive IGBT Collector Current (2)	$I_{C(pk)}$	30	A
IGBT Power Dissipation (T_C = 95°C)	PD	55	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Continuous Output Diode Current	I_{Fmax}	15	A
Peak Output Diode Current (2)	$I_{F(pk)}$	30	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	—	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 600 V)	I_R	—	5.0	50	μA
Forward Voltage (I_F = 15 A)	V_F	—	1.05	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	—	—	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	μA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 — —	 6.0 2000	 100 —	μA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 15 A)	$V_{CE(SAT)}$	—	2.7	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	2300	—	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V)	Q_T	—	75	—	nC
Fall Time — Inductive Load (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	1.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	1.0	mJ
Free–Wheeling Diode Forward Voltage (I_F = 15 A, V_{GE} = 0 V)	V_F	—	1.3	2.0	V
Free–Wheeling Diode Reverse Recovery Time (I_F = 15 A, V = 300 V, di/dt = 100 A/μs)	t_{rr}	—	140	200	ns
Free–Wheeling Diode Stored Charge (I_F = 15 A, V = 300 V, di/dt = 100 A/μs)	Q_{rr}	—	—	900	nC
Thermal Resistance — IGBT (Each Die)	$R_{\theta JC}$	—	—	1.9	°C/W
Thermal Resistance — Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	—	—	3.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 — —	 6.0 2000	 100 —	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 15 A)	$V_{CE(SAT)}$	—	2.7	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	2300	—	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V)	Q_T	—	75	—	nC
Fall Time — Inductive Load (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	1.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	1.0	mJ
Output Diode Forward Voltage (I_F = 15 A)	V_F	—	1.3	2.0	V
Output Diode Reverse Leakage Current	I_R	—	—	50	µA
Thermal Resistance — IGBT	$R_{\theta JC}$	—	—	1.9	°C/W
Thermal Resistance — Output Diode	$R_{\theta JC}$	—	—	3.7	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	—	10	—	mΩ
Resistance Tolerance	R_{tol}	–1.0	—	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	—	0.660	—	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–1.95	—	mV/°C

Typical Characteristics

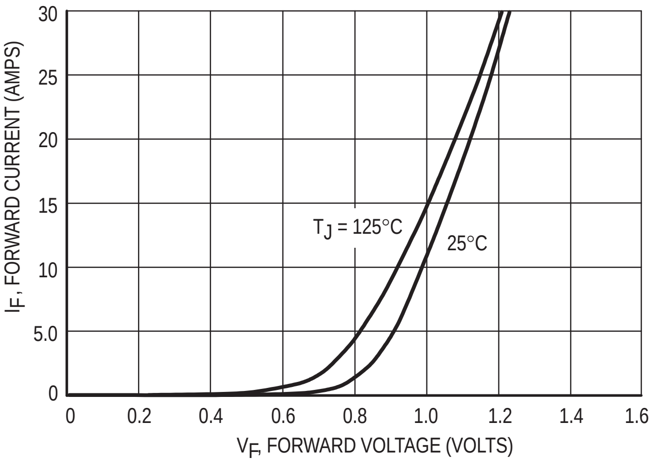


Figure 1. Forward Characteristics — Input Rectifier

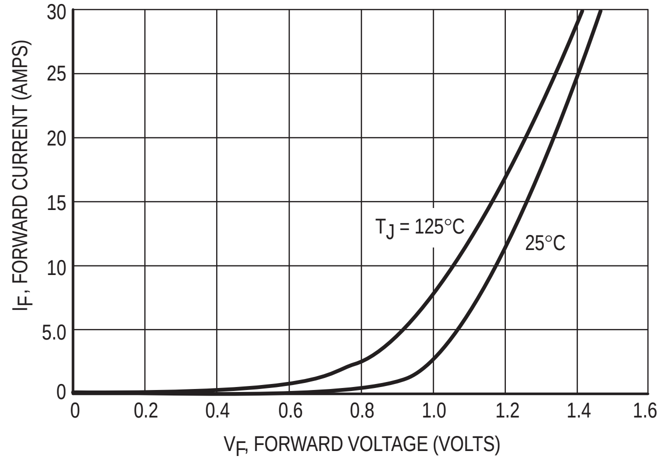


Figure 2. Forward Charactristics — Free–Wheeling Diode

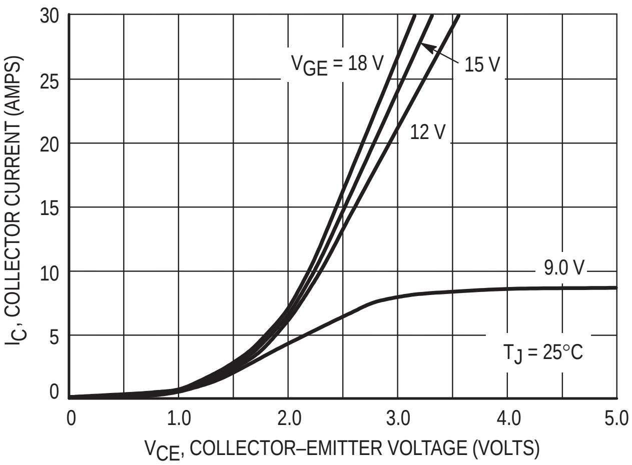


Figure 3. Forward Characteristics, T_J = 25°C

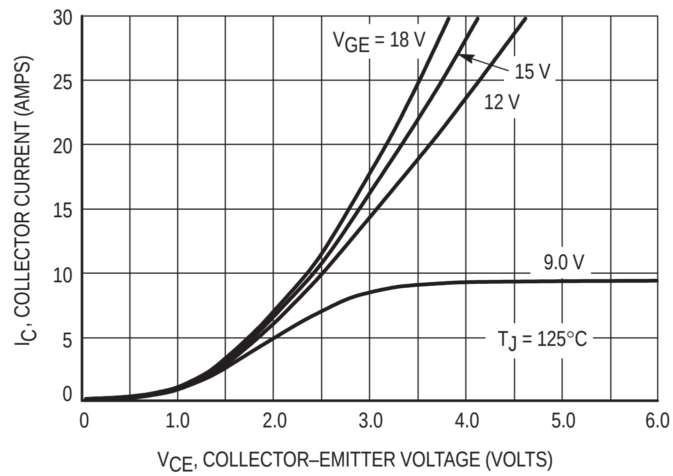


Figure 4. Forward Characteristics, T_J = 125°C

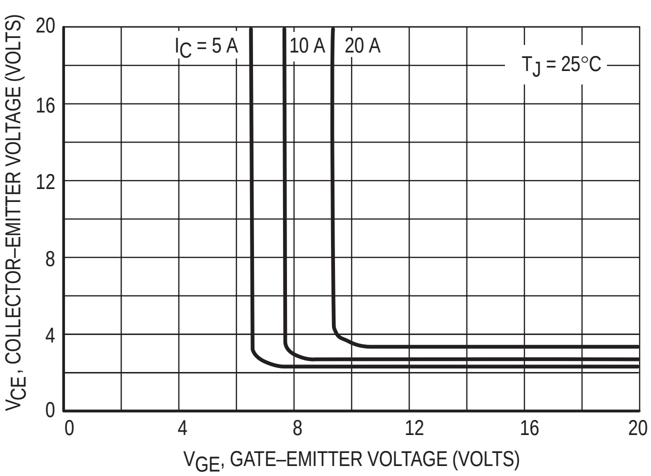


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

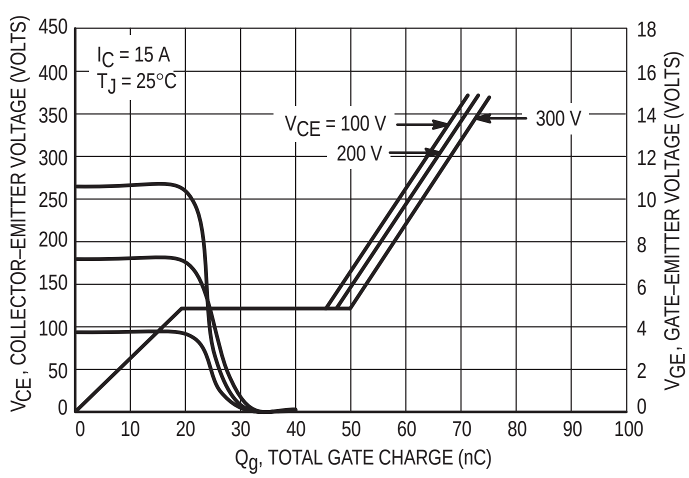


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

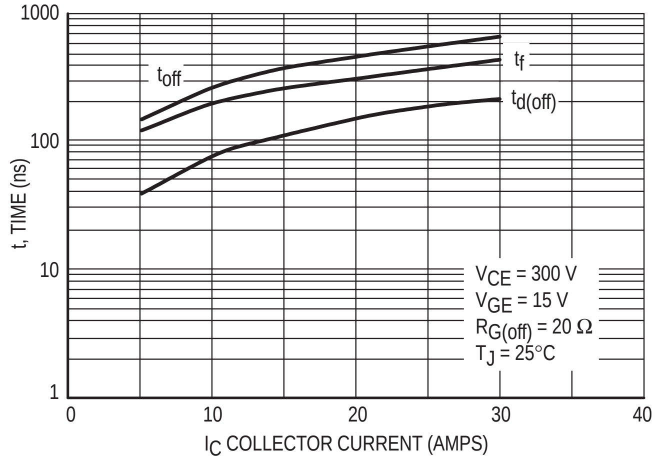


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

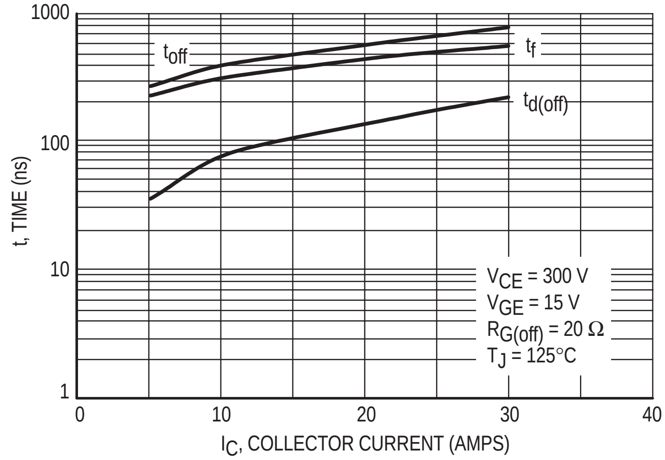


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

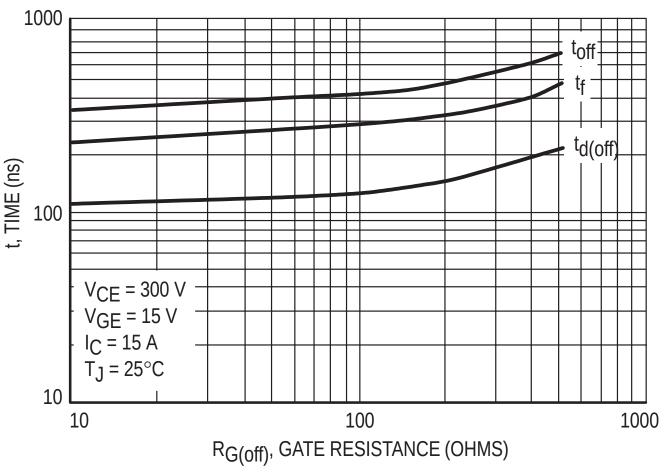


Figure 9. Inductive Switching Times versus Gate Resistance

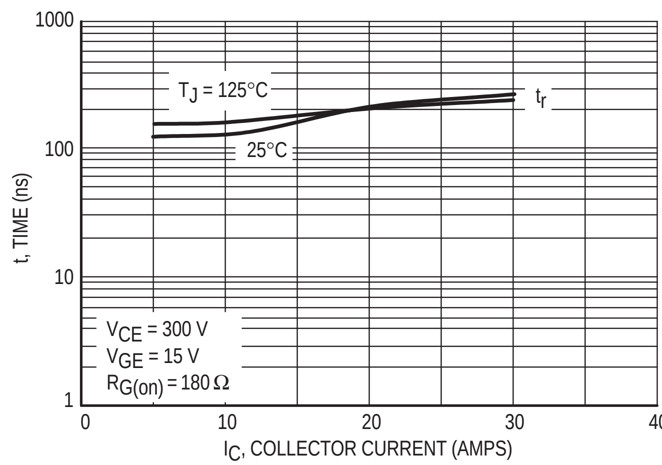


Figure 10. Inductive Switching Times versus Collector Current

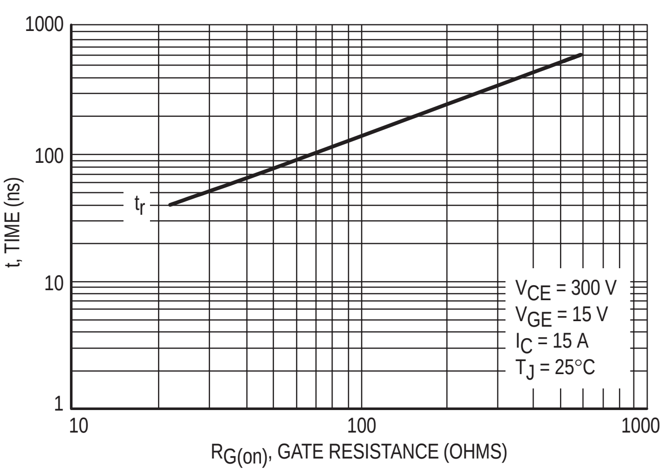


Figure 11. Inductive Switching Times versus Gate Resistance

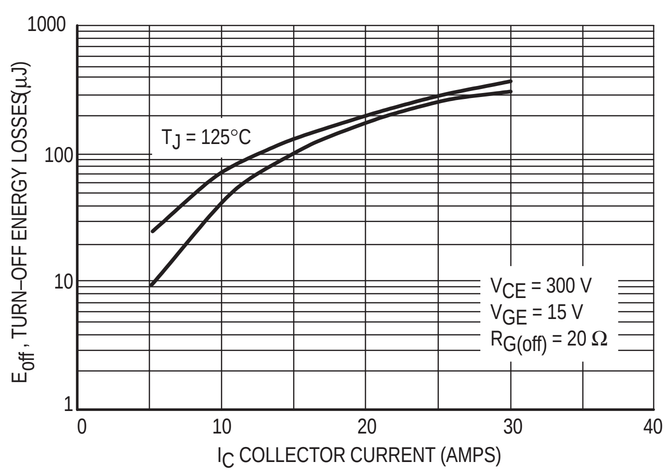


Figure 12. Turn–Off Energy Losses versus Collector Current

Typical Characteristics

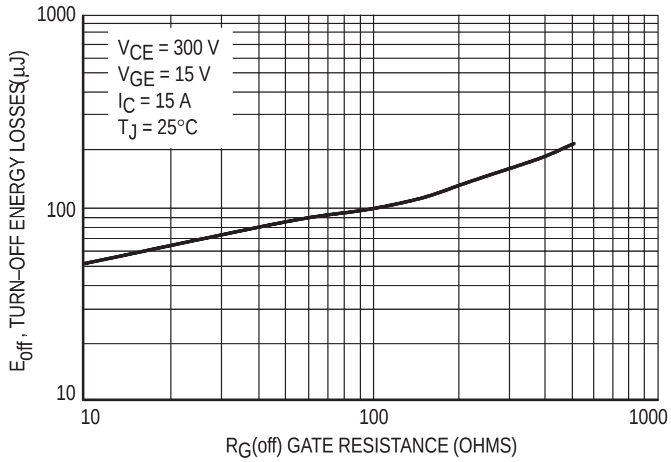


Figure 13. Turn–Off Energy Losses versus Gate Resistance

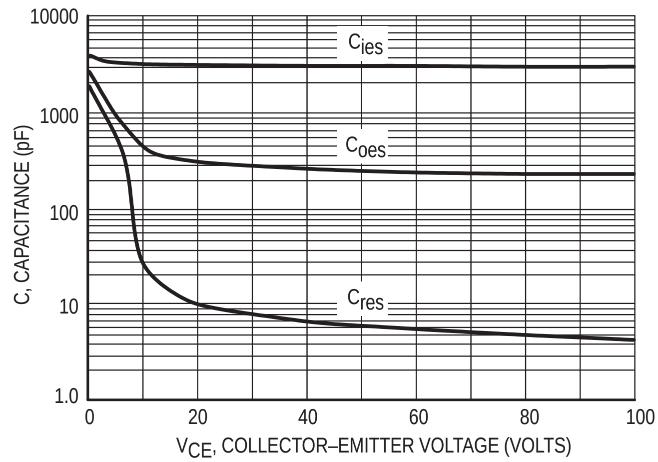


Figure 14. Capacitance Variation

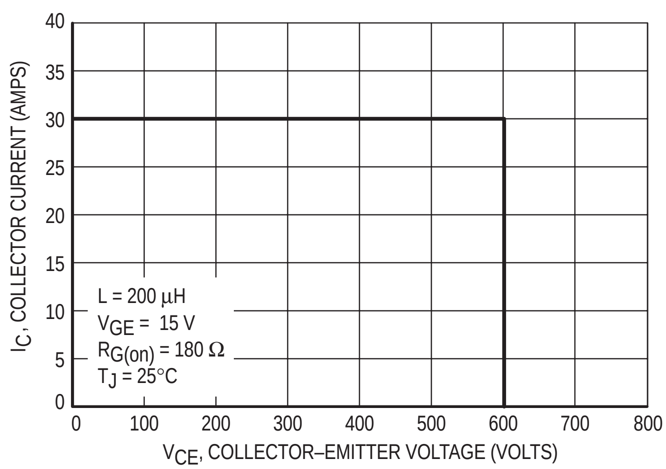


Figure 15. Reverse Biased Safe Operating Area (RBSOA)

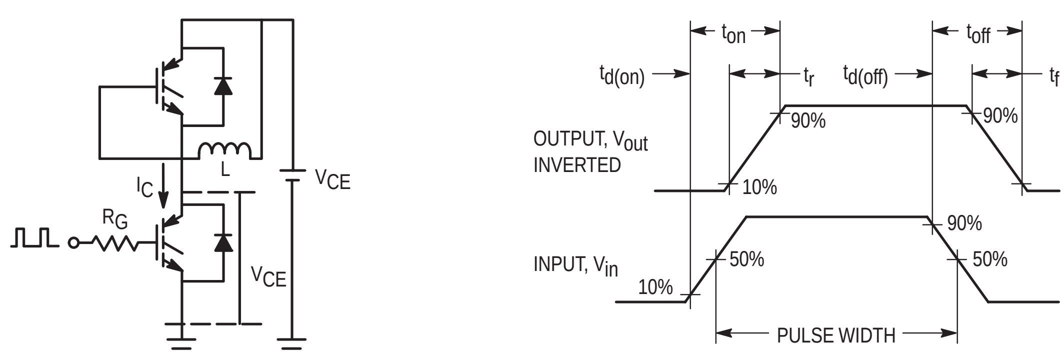


Figure 16. Inductive Switching Time Test Circuit and Timing Chart

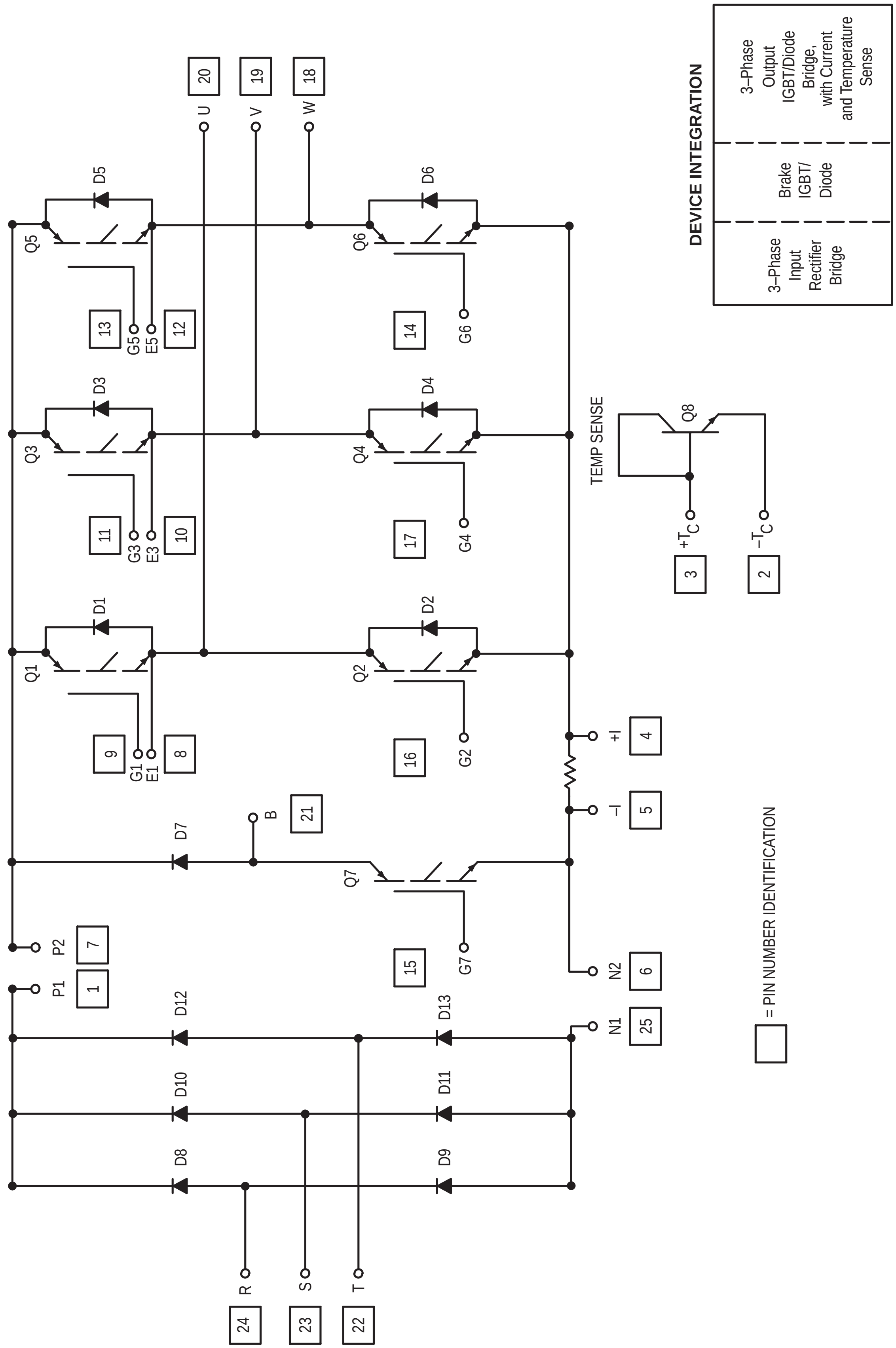


Figure 17. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 1.0 hp Motor Drives

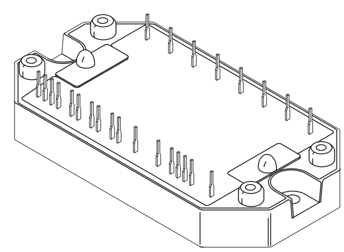
(This device is not recommended for new designs)
(This device is replaced by MHPM7A10E60DC3)

MHPM7B15A60A

15 AMP, 600 VOLT
HYBRID POWER MODULE

This module integrates a 3-phase input rectifier bridge, 3-phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free-wheeling diodes to give optimal dynamic performance. It has been configured for use as a three-phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 300V
- Pin-to-Baseplate Isolation exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440-02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Average Output Rectified Current	I_O	15	A
Peak Non-repetitive Surge Current — (1/2 Cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	15	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	30	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	15	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	30	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	55	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	30	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 300V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1.0 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	15	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	30	A
IGBT Power Dissipation (T_C = 95°C)	PD	55	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Continuous Output Diode Current	I_{Fmax}	15	A
Peak Output Diode Current(2)	$I_{F(pk)}$	30	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	—	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 600 V)	I_R	—	5.0	50	µA
Forward Voltage (I_F = 15 A)	V_F	—	1.05	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	—	—	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 — —	 6.0 2000	 100 —	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 15 A)	$V_{CE(SAT)}$	—	2.7	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	2300	—	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V)	Q_T	—	75	—	nC
Fall Time — Inductive Load (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	1.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	1.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 15 A, V_{GE} = 0 V)	V_F	—	1.3	2.0	V
Free Wheeling Diode Reverse Recovery Time (I_F = 15 A, V = 300 V, di/dt = 100 A/µs)	t_{rr}	—	140	200	ns
Free Wheeling Diode Stored Charge (I_F = 15 A, V = 300 V, di/dt = 100 A/µs)	Q_{rr}	—	—	900	nC
Thermal Resistance — IGBT (Each Die)	$R_{\theta JC}$	—	—	1.9	°C/W
Thermal Resistance — Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	—	—	3.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	— —	6.0 2000	100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 15 A)	$V_{CE(SAT)}$	—	2.7	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	2300	—	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V)	Q_T	—	75	—	nC
Fall Time — Inductive Load (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(on)}$ = 180 Ω)	$E_{(on)}$	—	—	1.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 15 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	$E_{(off)}$	—	—	1.0	mJ
Output Diode Forward Voltage (I_F = 15 A)	V_F	—	1.3	2.0	V
Output Diode Reverse Leakage Current	I_R	—	—	50	µA
Thermal Resistance — IGBT	$R_{\theta JC}$	—	—	1.9	°C/W
Thermal Resistance — Output Diode	$R_{\theta JC}$	—	—	3.7	°C/W

Typical Characteristics

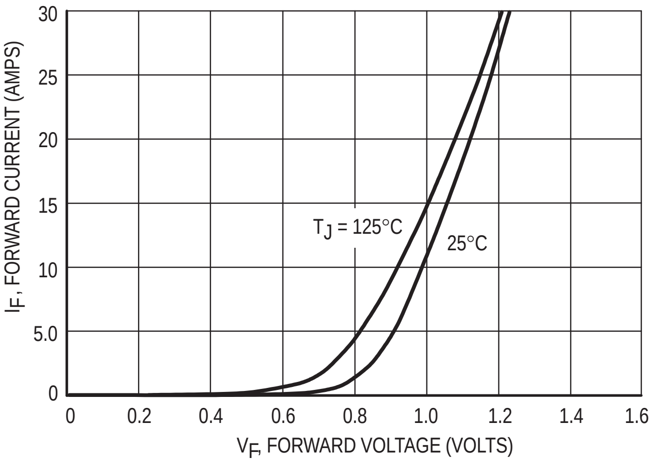


Figure 1. Forward Characteristics — Input Rectifier

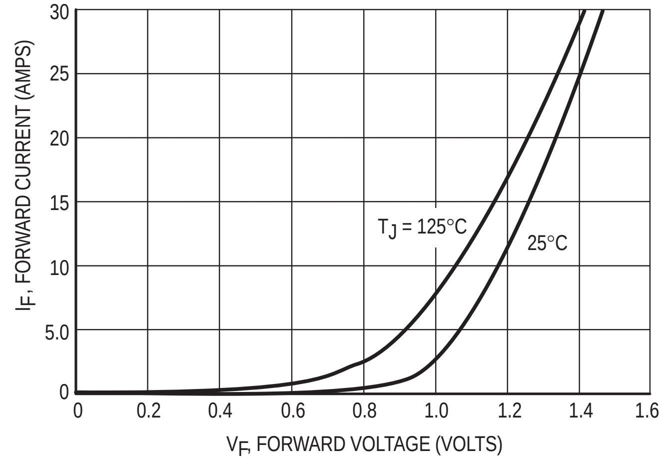


Figure 2. Forward Charactristics — Free–Wheeling Diode

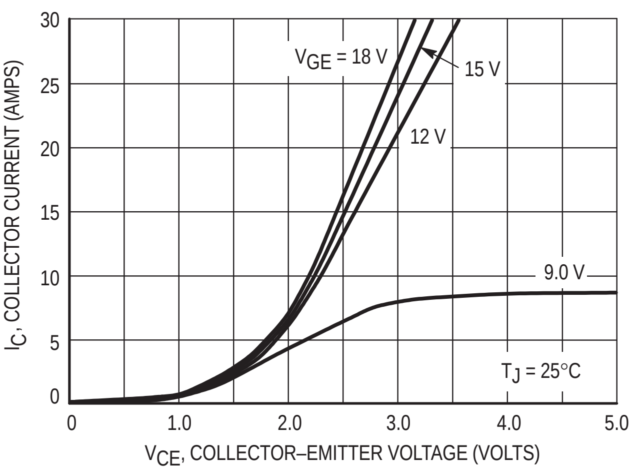


Figure 3. Forward Characteristics, T_J = 25°C

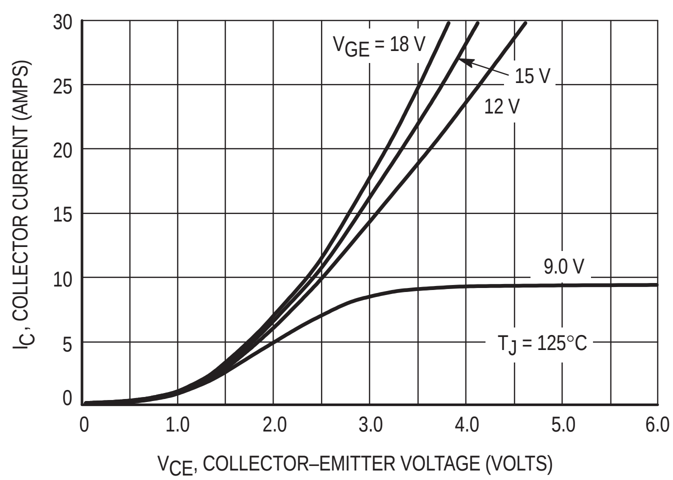


Figure 4. Forward Characteristics, T_J = 125°C

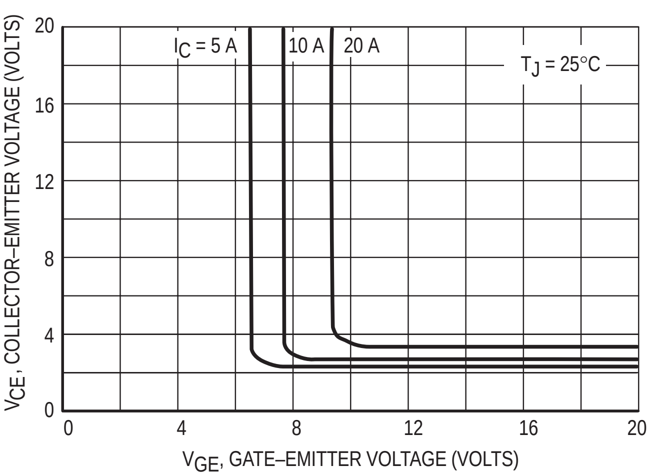


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

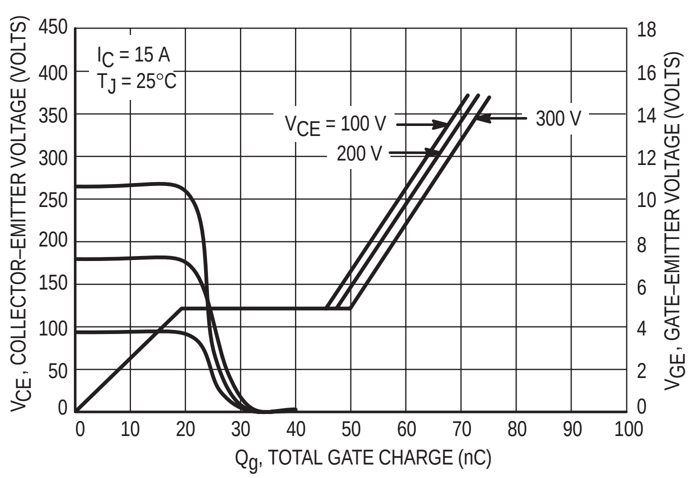


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

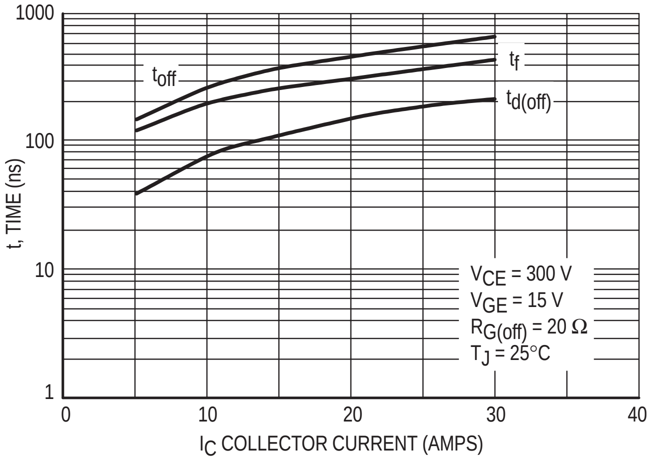


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

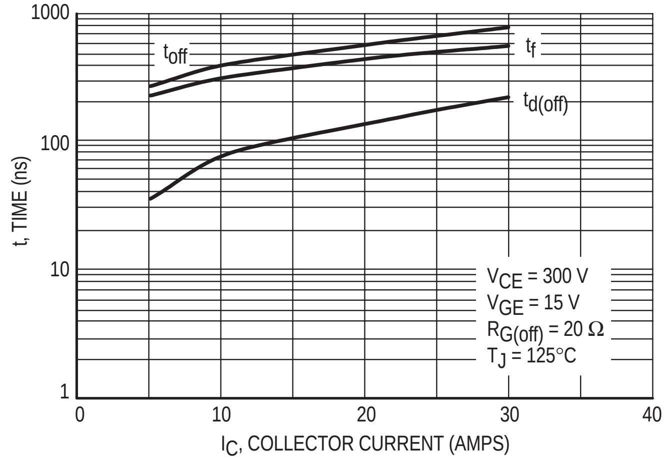


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

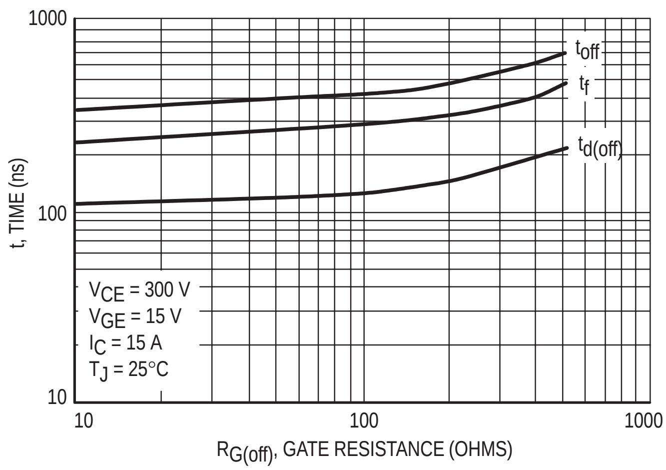


Figure 9. Inductive Switching Times versus Gate Resistance

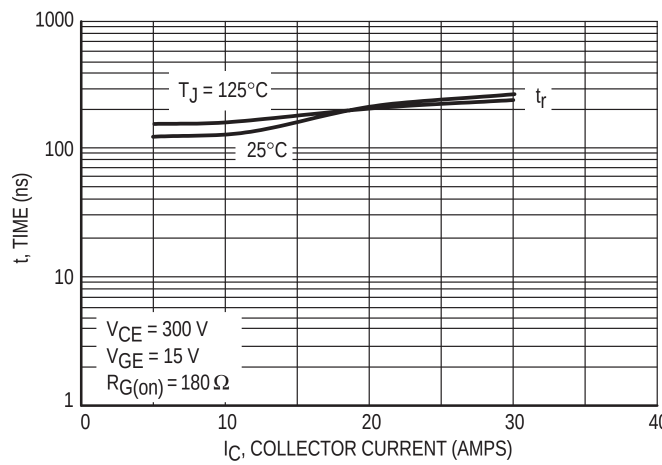


Figure 10. Inductive Switching Times versus Collector Current

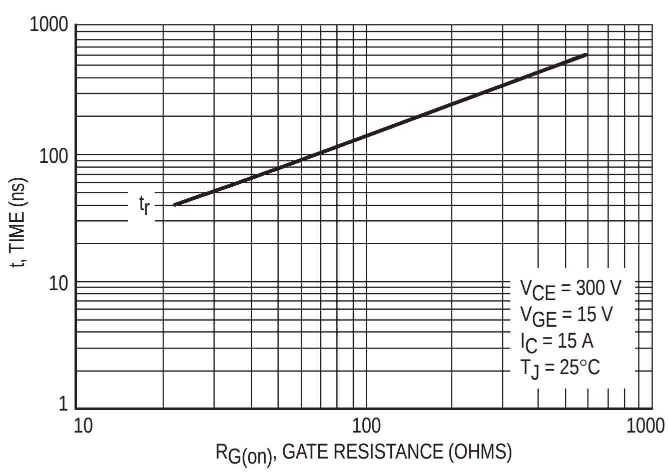


Figure 11. Inductive Switching Times versus Gate Resistance

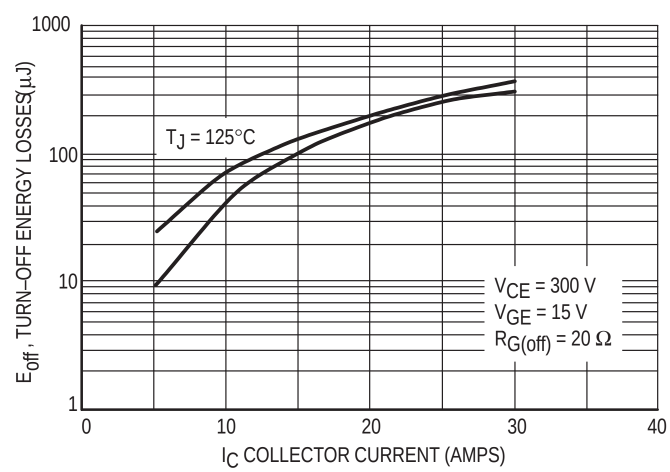


Figure 12. Turn–Off Energy Losses versus Collector Current

Typical Characteristics

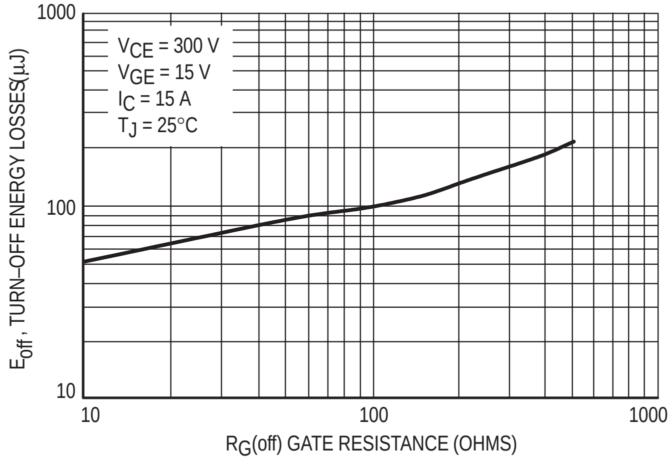


Figure 13. Turn–Off Energy Losses versus Gate Resistance

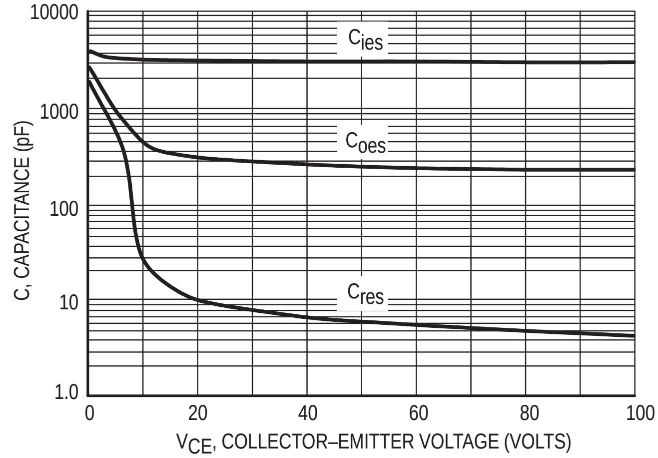


Figure 14. Capacitance Variation

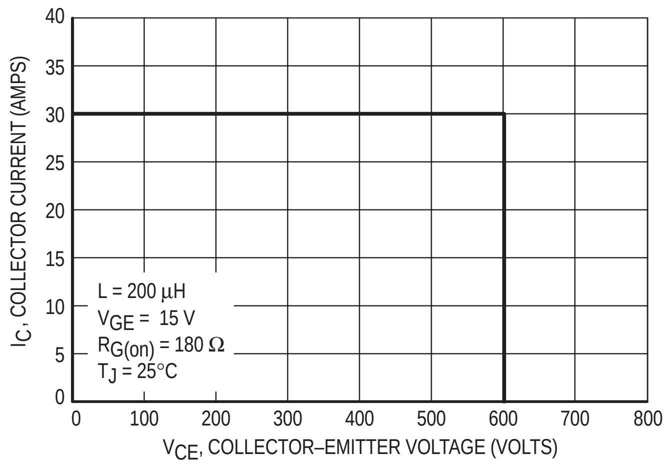


Figure 15. Reverse Biased Safe Operating Area (RBSOA)

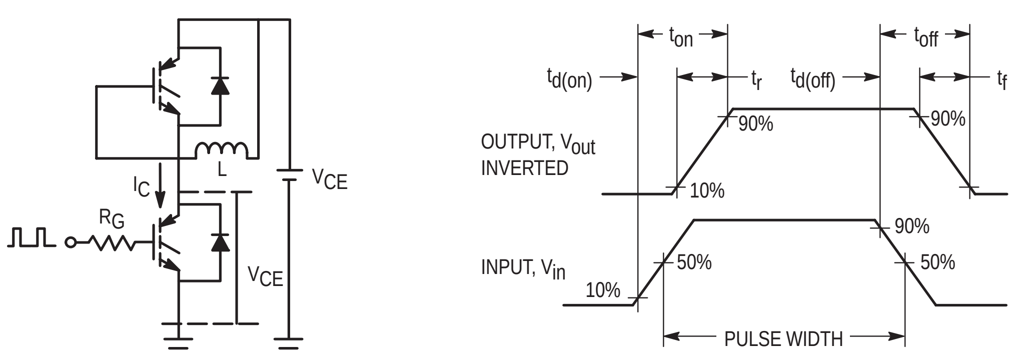


Figure 16. Inductive Switching Time Test Circuit and Timing Chart

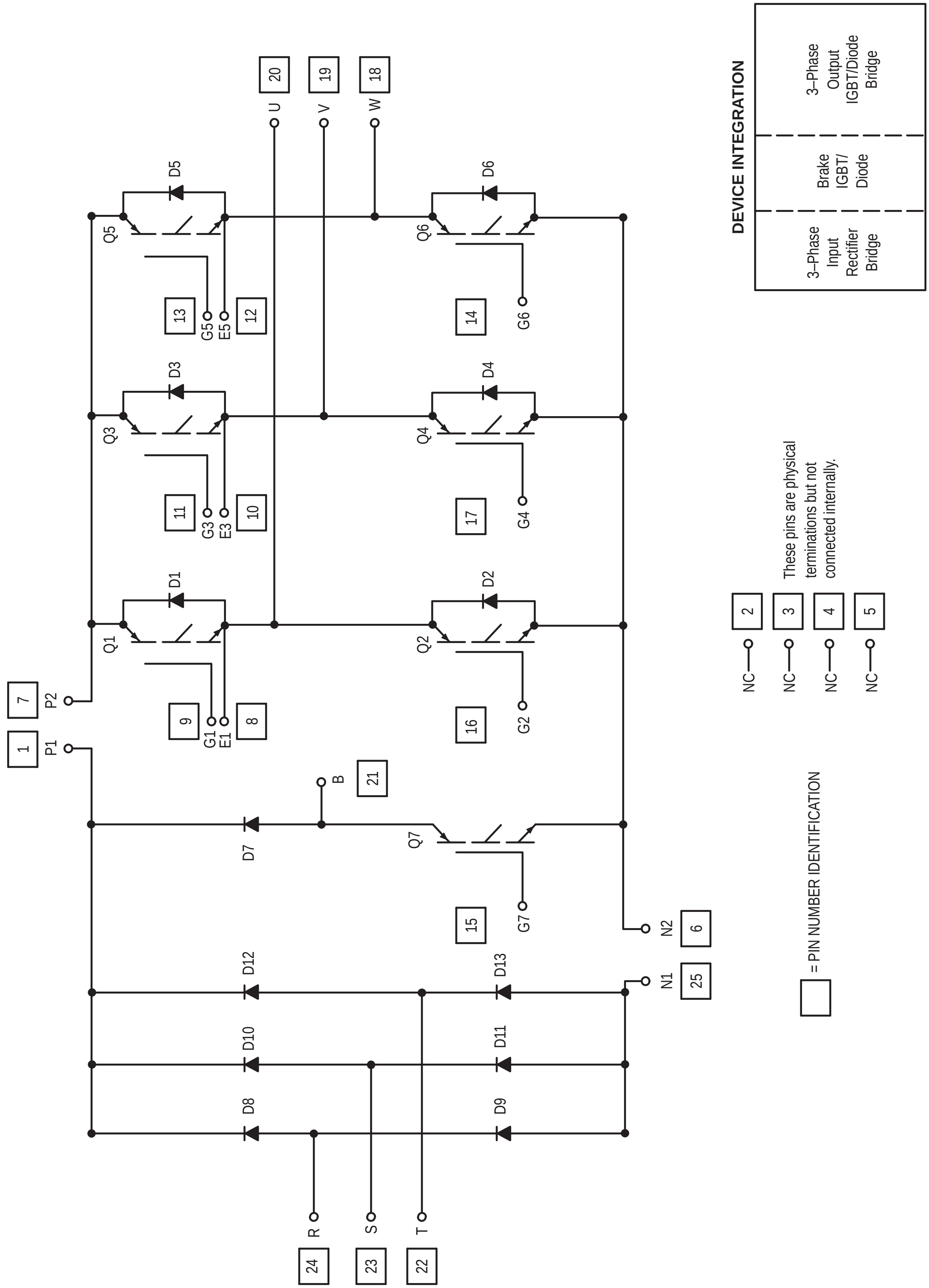


Figure 17. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 2.0 hp Motor Drives

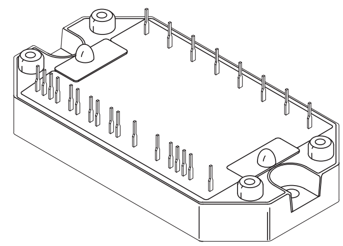
(This device is not recommended for new designs)
(This device is replaced by MHPM7A20E60DC3)

MHPM7A20A60A

20 AMP, 600 VOLT
HYBRID POWER MODULE

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 300V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440-02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 25°C)	V_{RRM}	600	V
Average Output Rectified Current	I_O	20	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	240	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	20	A
Peak Repetitive IGBT Collector Current – (PW = 1.0 ms)(2)	$I_{C(pk)}$	40	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	20	A
Peak Repetitive Free-Wheeling Diode Current – (PW = 1.0 ms)(2)	$I_{F(pk)}$	40	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	78	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	39	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 300V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	20	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	40	A
IGBT Power Dissipation (T_C = 95°C)	PD	78	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Continuous Output Diode Current	I_{Fmax}	20	A
Peak Output Diode Current(2)	$I_{F(pk)}$	40	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 600 V)	I_R	–	5.0	50	µA
Forward Voltage (I_F = 20 A)	V_F	–	1.1	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (I_C = 20 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	4400	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V)	Q_T	–	145	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(on)}$ = 47 Ω)	E_{on}	–	–	2.5	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.5	mJ
Free Wheeling Diode Forward Voltage (I_F = 20 A, V_{GE} = 0 V)	V_F	–	1.3	2.0	V
Free Wheeling Diode Reverse Recovery Time (I_F = 20 A, V = 300 V, di/dt = 100 A/µs)	t_{rr}	–	170	200	ns
Free Wheeling Diode Stored Charge (I_F = 20 A, V = 300 V, di/dt = 100 A/µs)	Q_{rr}	–	1060	1600	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.5	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100 –	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 20 A)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	–	4400	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V)	Q_T	–	145	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(on)}$ = 47 Ω)	E_{on}	–	–	2.5	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.5	mJ
Output Diode Forward Voltage (I_F = 20 A)	V_F	–	1.3	2.0	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.5	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.9	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	–	5.0	–	mΩ
Resistance Tolerance	R_{tol}	–1.0	–	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	–	0.660	–	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	–	–1.95	–	mV/°C

Typical Characteristics

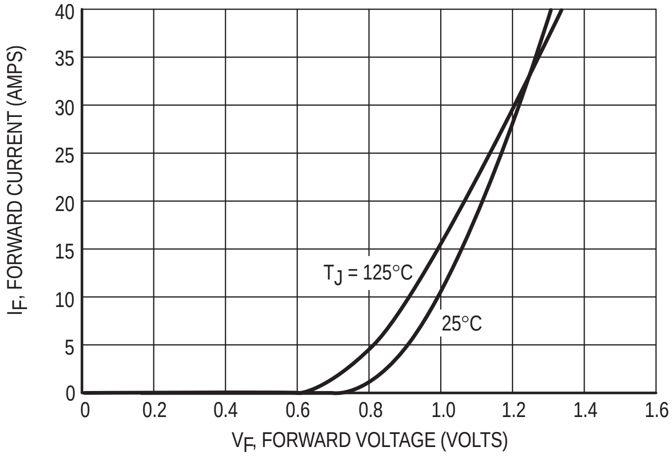


Figure 1. Forward Characteristics — Input Rectifier

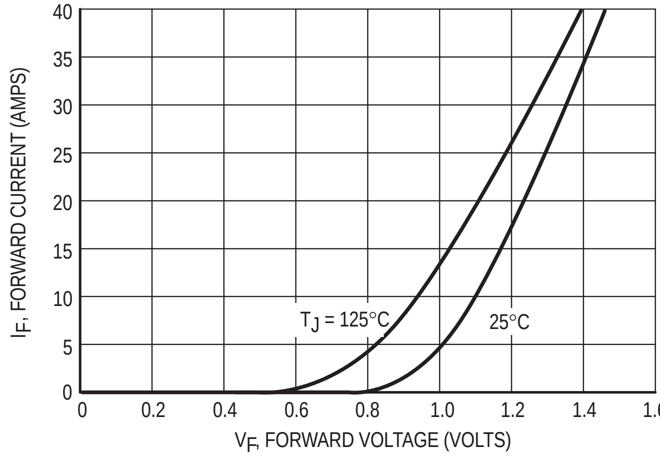


Figure 2. Forward Characteristics — Free–Wheeling Diode

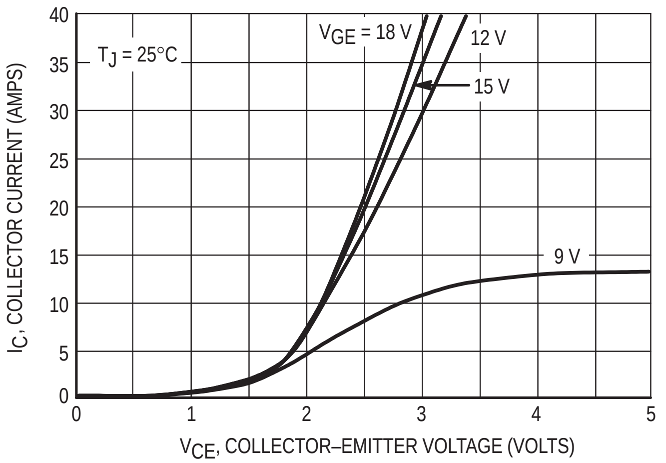


Figure 3. Forward Characteristics, T_J = 25°C

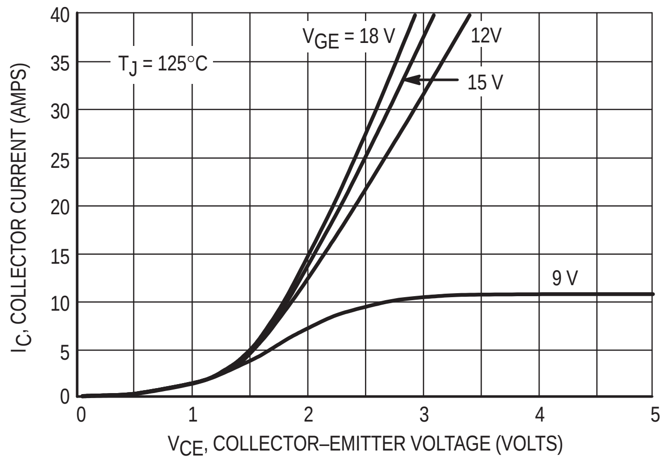


Figure 4. Forward Characteristics, T_J = 125°C

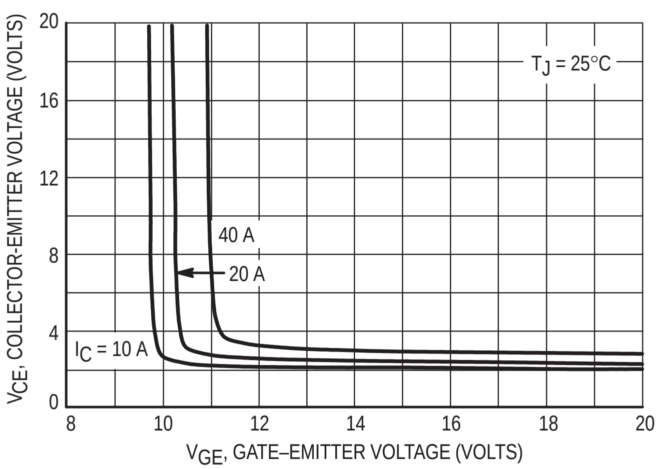


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

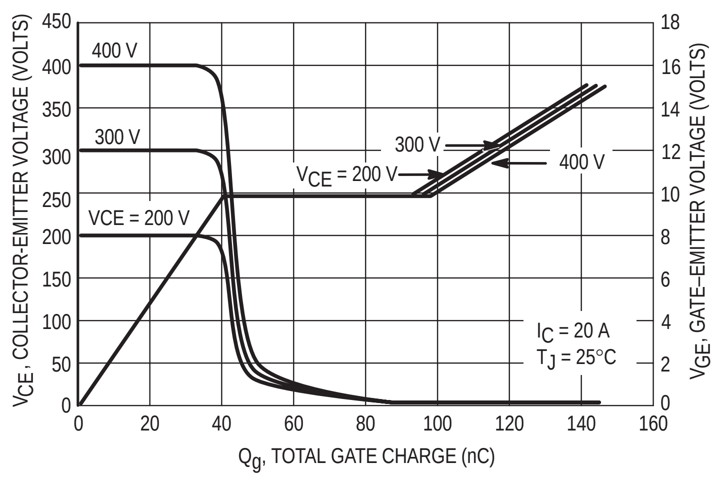


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

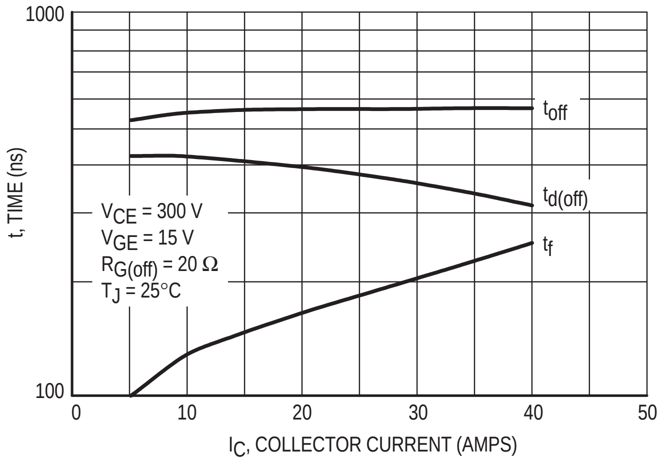


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

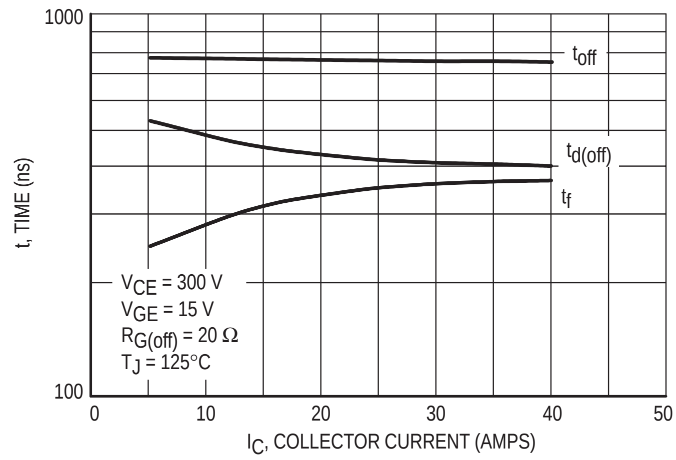


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

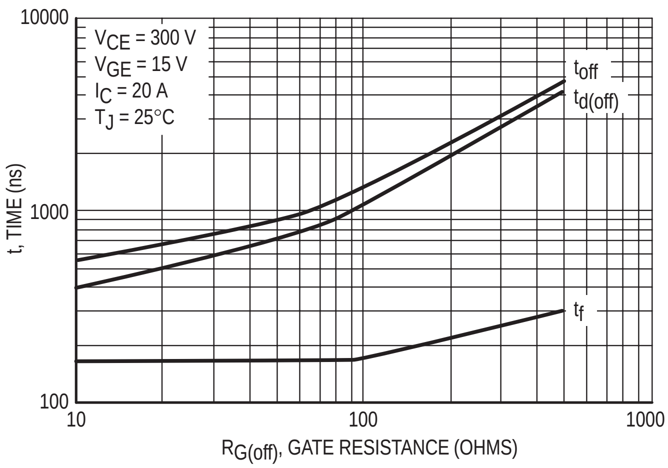


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

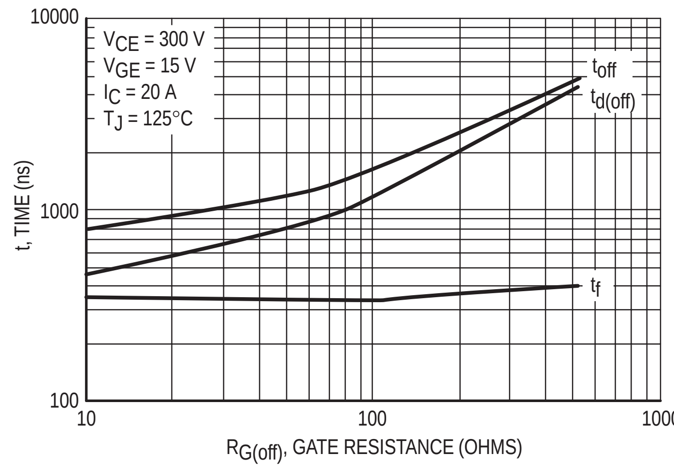


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

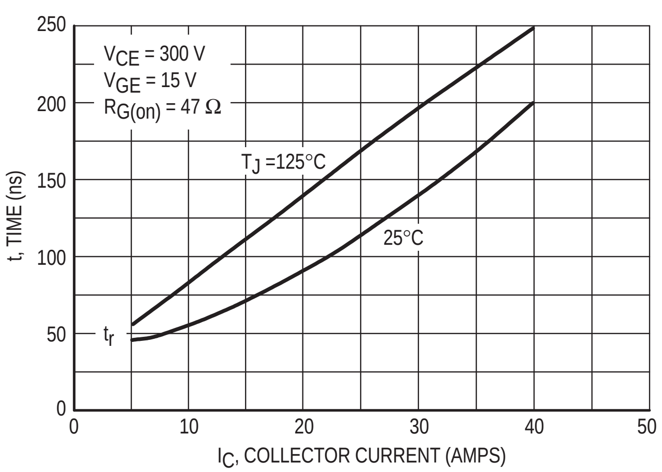


Figure 11. Inductive Switching Times versus Collector Current

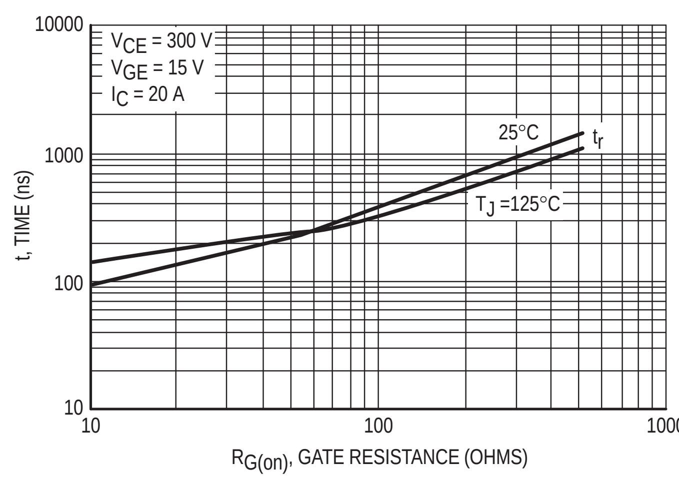


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

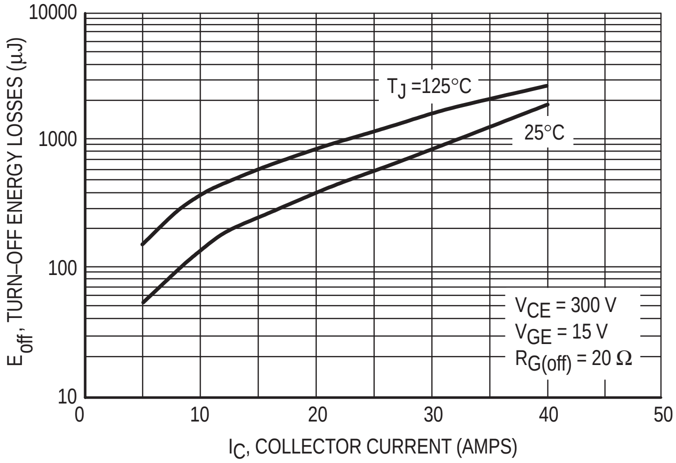


Figure 13. Turn–Off Energy Losses versus Collector Current

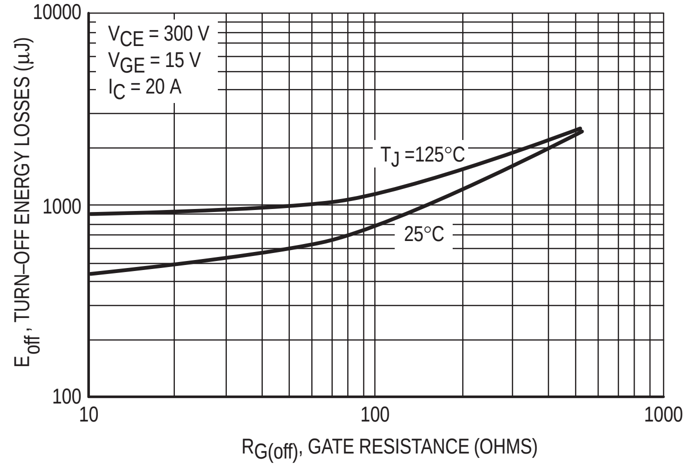


Figure 14. Turn–Off Energy Losses versus Gate Resistance

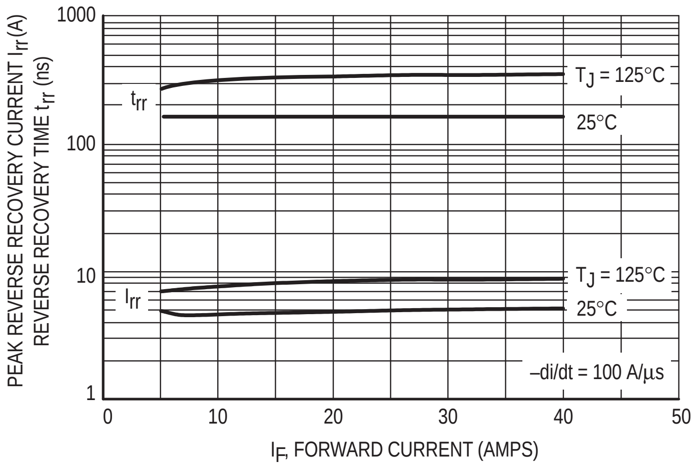


Figure 15. Reverse Recovery Characteristics — Free–Wheeling Diode

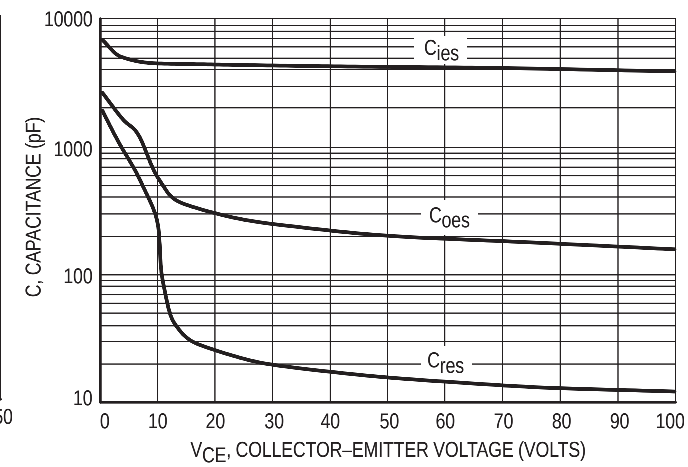


Figure 16. Capacitance Variation

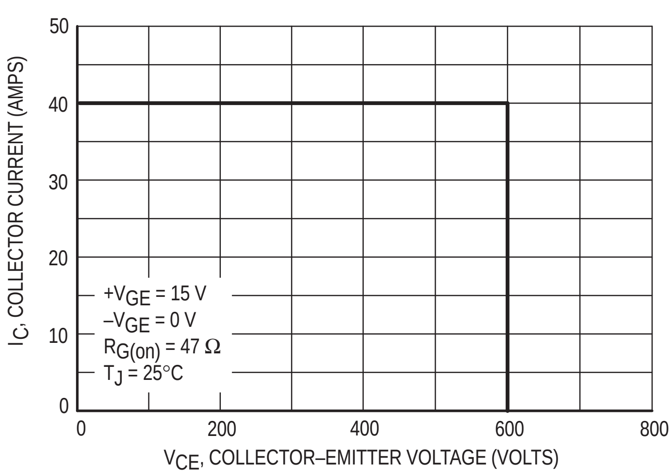


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

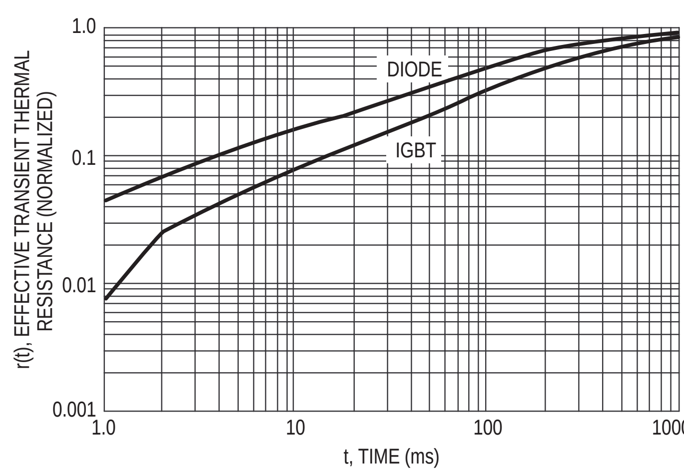


Figure 18. Thermal Response

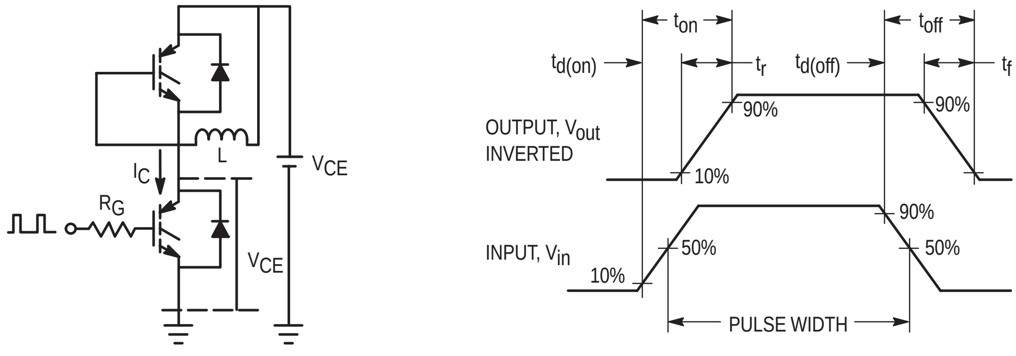


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

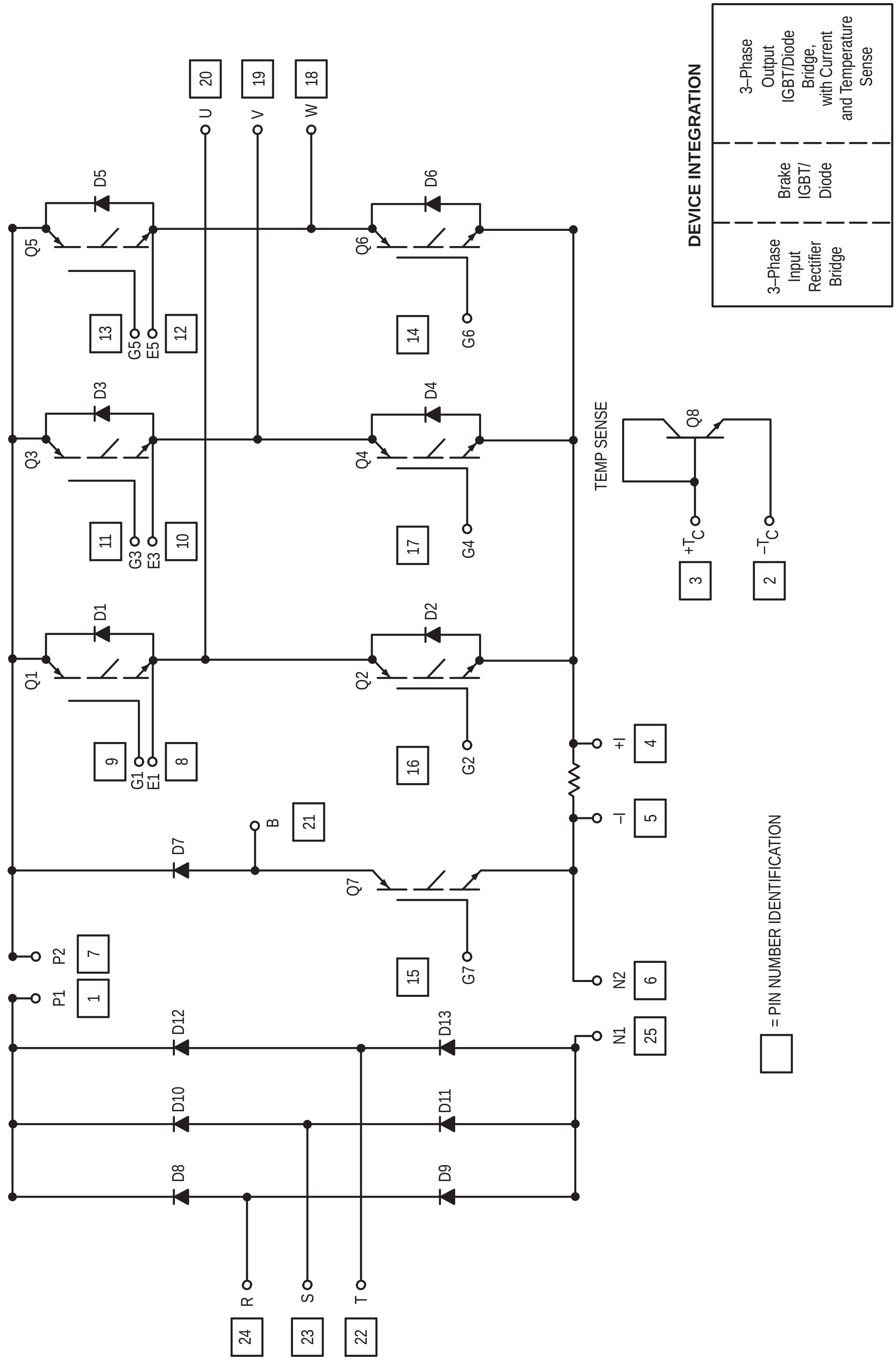


Figure 20. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 2.0 hp Motor Drives

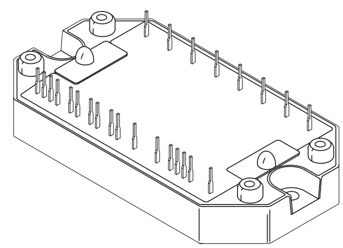
(This device is not recommended for new designs)
(This device is replaced by MHPM7A20E60DC3)

MHPM7B20A60A

20 AMP, 600 VOLT
HYBRID POWER MODULE

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 300V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440-02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Average Output Rectified Current	I_O	20	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	240	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	20	A
Peak Repetitive IGBT Collector Current – (PW = 1.0 ms)(2)	$I_{C(pk)}$	40	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	20	A
Peak Repetitive Free-Wheeling Diode Current – (PW = 1.0 ms)(2)	$I_{F(pk)}$	40	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	78	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	39	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 300 V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	20	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	40	A
IGBT Power Dissipation (T_C = 95°C)	PD	78	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Continuous Output Diode Current	I_{Fmax}	20	A
Peak Output Diode Current(2)	$I_{F(pk)}$	40	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 600 V)	I_R	–	5.0	50	μA
Forward Voltage (I_F = 20 A)	V_F	–	1.1	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	μA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	μA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (I_C = 20 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	4400	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V)	Q_T	–	145	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(on)}$ = 47 Ω)	E_{on}	–	–	2.5	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.5	mJ
Free Wheeling Diode Forward Voltage (I_F = 20 A, V_{GE} = 0 V)	V_F	–	1.3	2.0	V
Free Wheeling Diode Reverse Recovery Time (I_F = 20 A, V = 300 V, di/dt = 100 A/μs)	t_{rr}	–	170	200	ns
Free Wheeling Diode Stored Charge (I_F = 20 A, V = 300 V, di/dt = 100 A/μs)	Q_{rr}	–	1060	1600	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.5	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100 –	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 20 A)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	–	4400	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V)	Q_T	–	145	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	210	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(on)}$ = 47 Ω)	E_{on}	–	–	2.5	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 20 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.5	mJ
Output Diode Forward Voltage (I_F = 20 A)	V_F	–	1.3	2.0	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.5	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.9	°C/W

Typical Characteristics

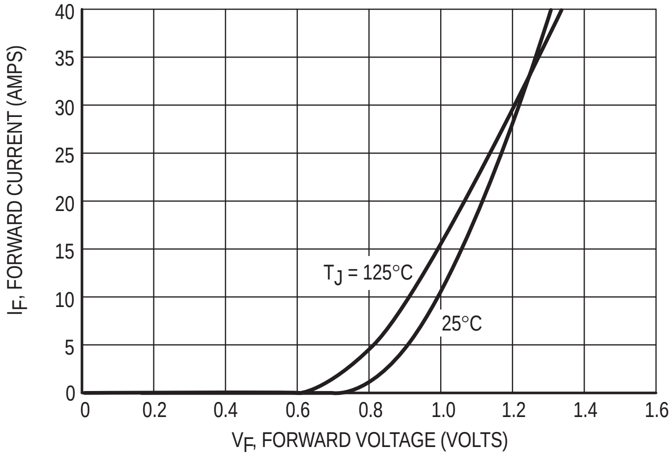


Figure 1. Forward Characteristics — Input Rectifier

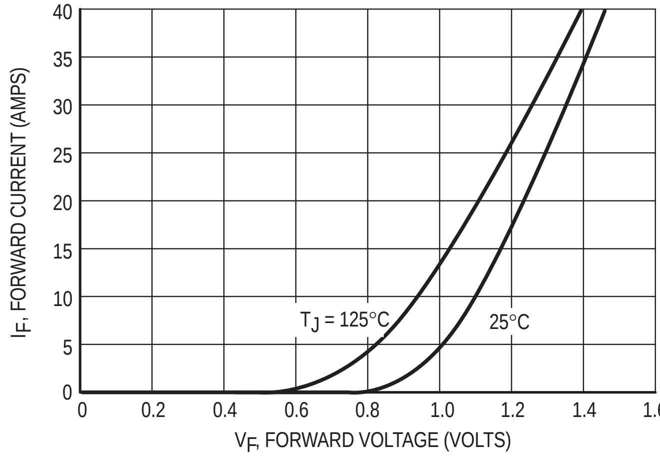


Figure 2. Forward Characteristics — Free–Wheeling Diode

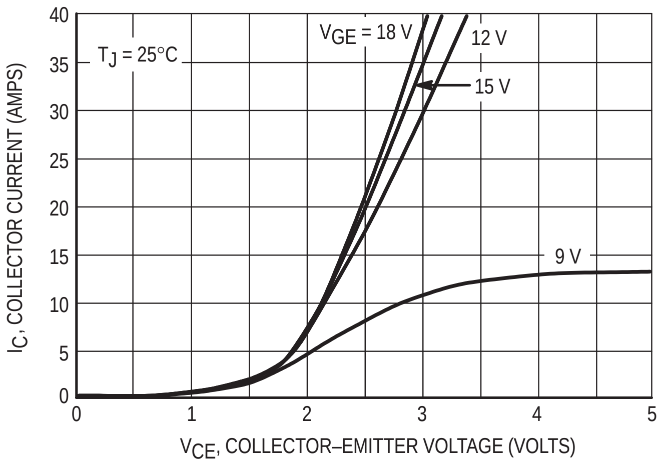


Figure 3. Forward Characteristics, T_J = 25°C

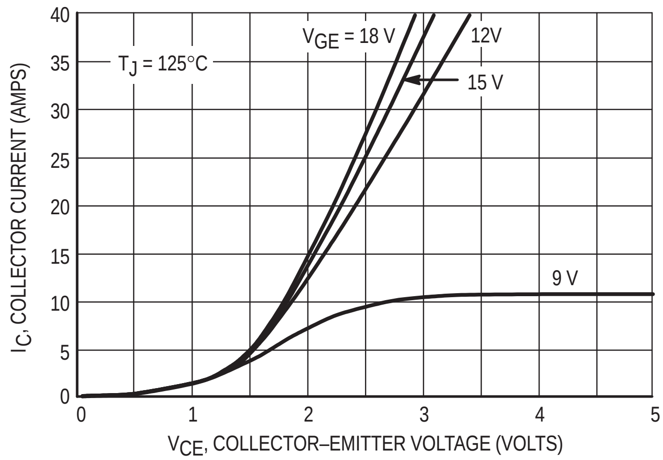


Figure 4. Forward Characteristics, T_J = 125°C

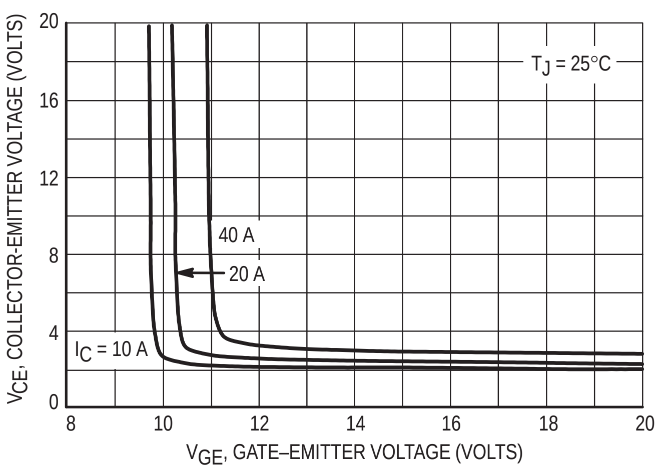


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

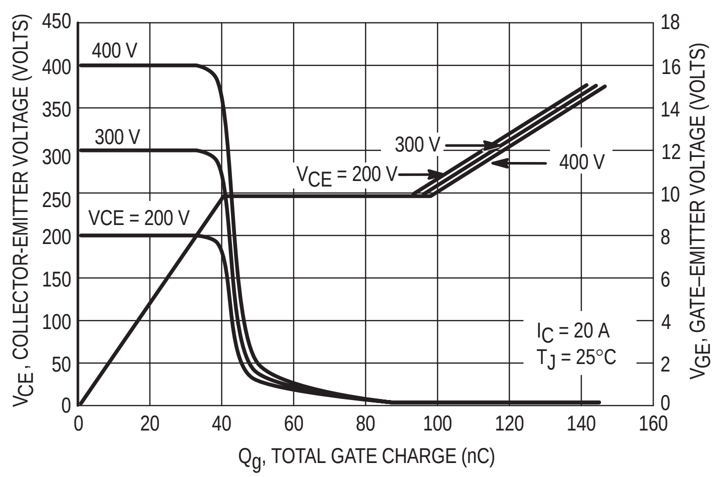


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

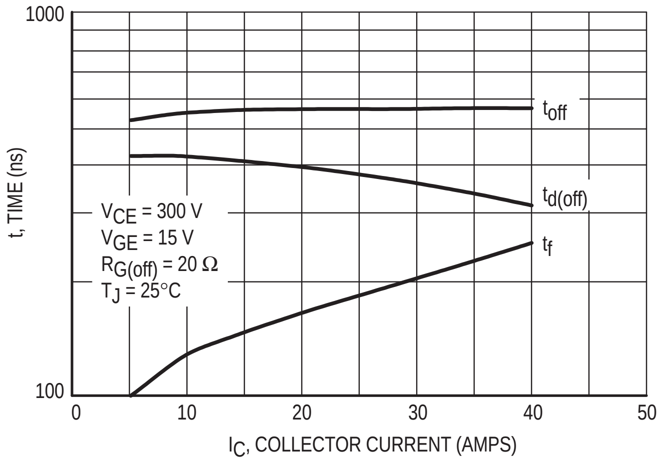


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

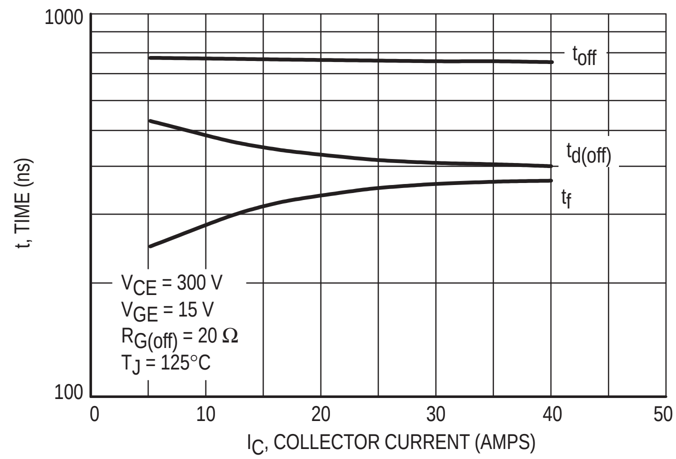


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

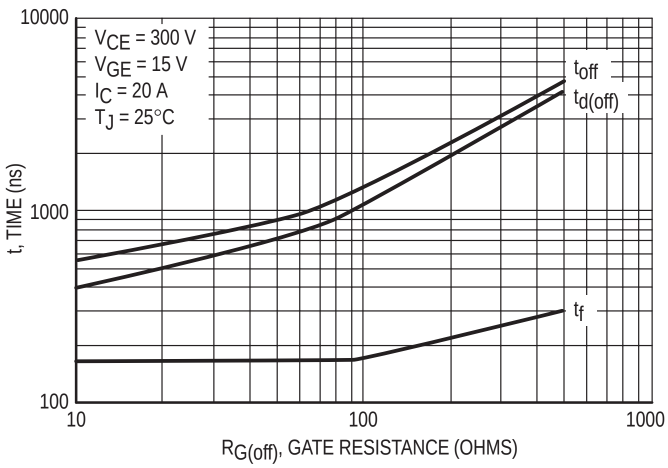


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

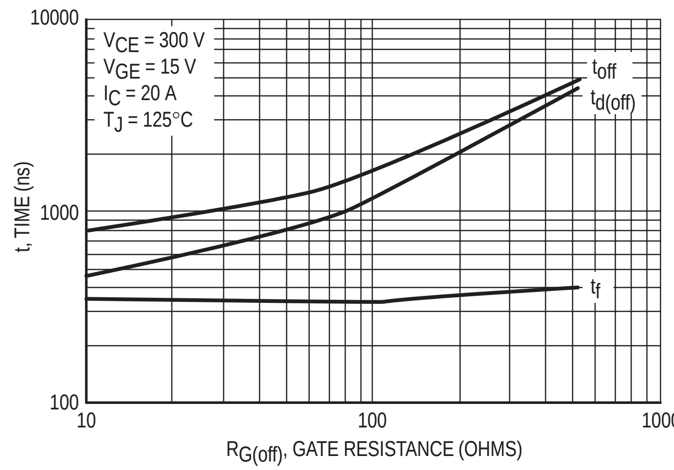


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

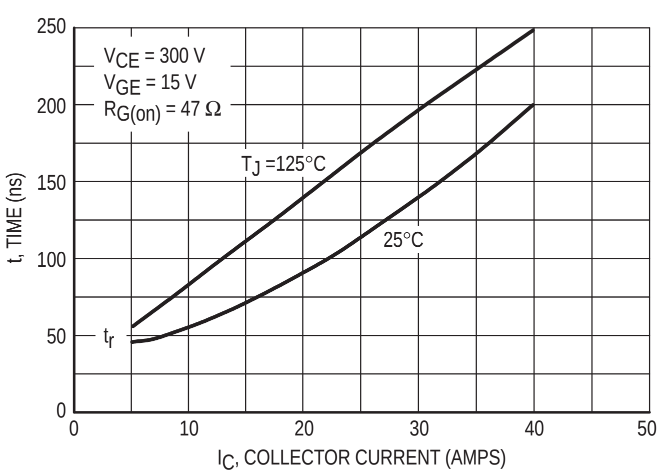


Figure 11. Inductive Switching Times versus Collector Current

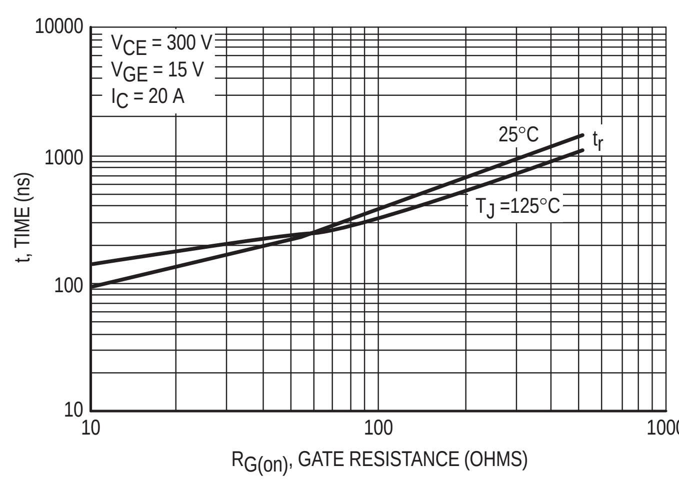


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

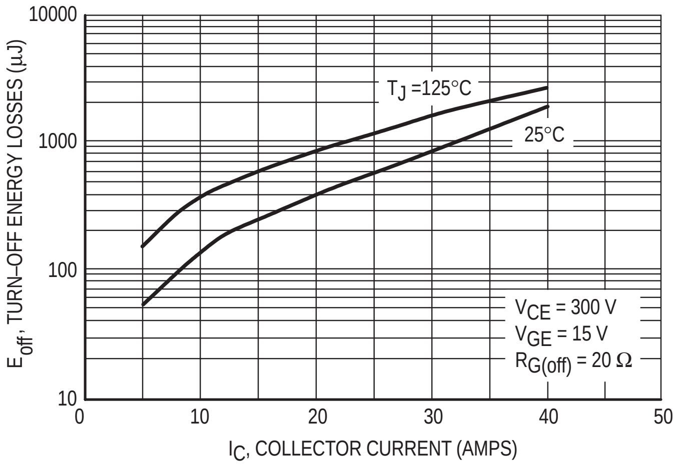


Figure 13. Turn–Off Energy Losses versus Collector Current

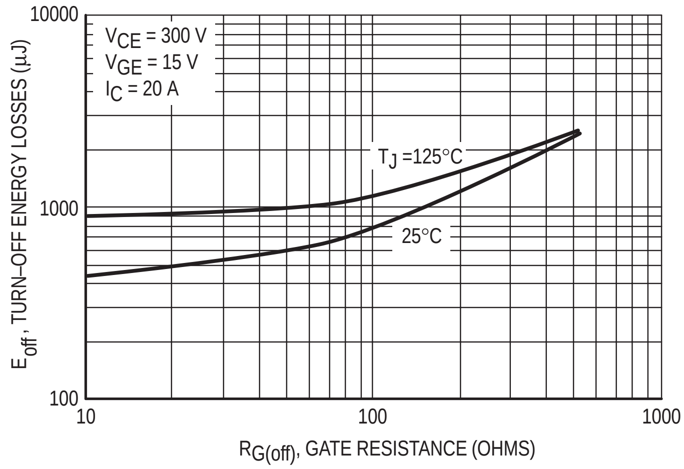


Figure 14. Turn–Off Energy Losses versus Gate Resistance

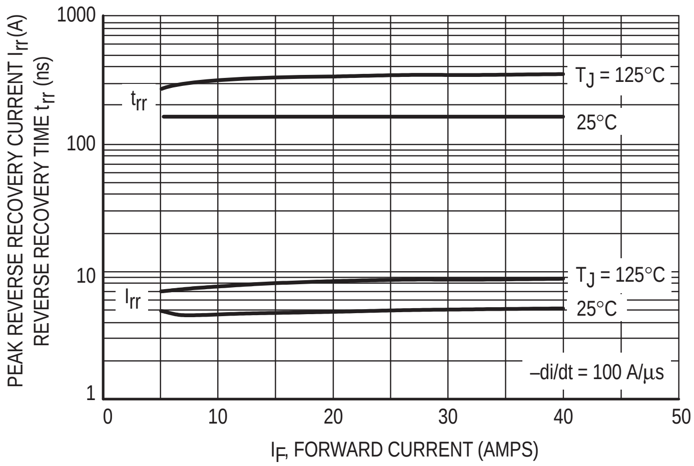


Figure 15. Reverse Recovery Characteristics — Free–Wheeling Diode

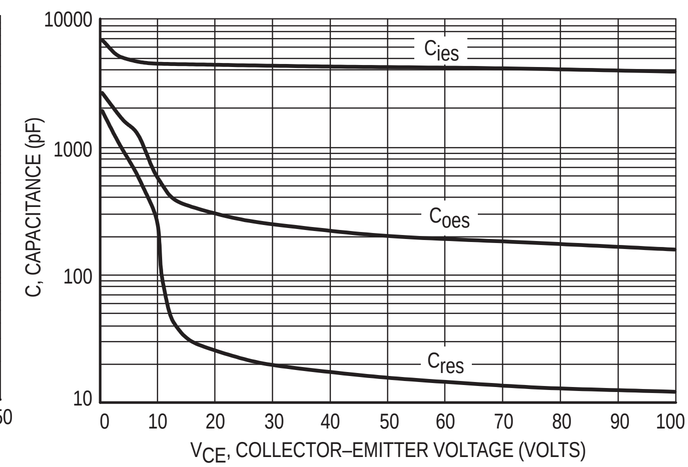


Figure 16. Capacitance Variation

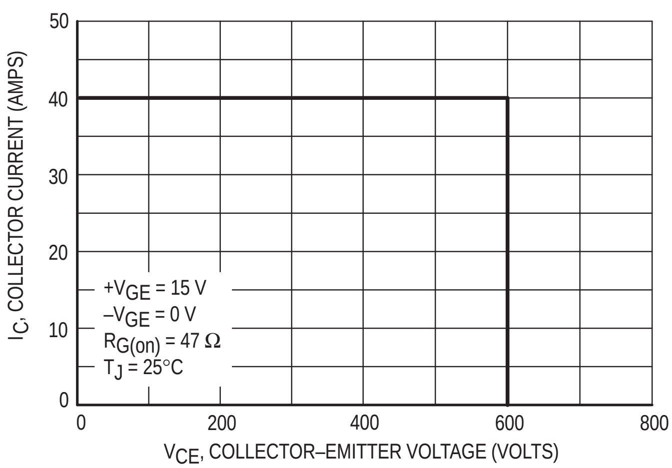


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

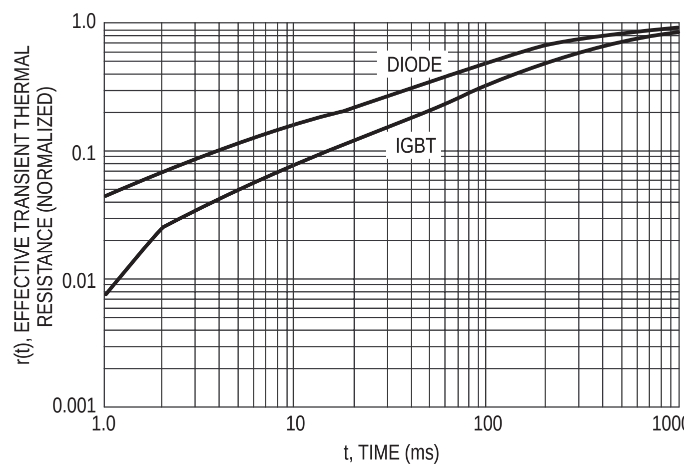


Figure 18. Thermal Response

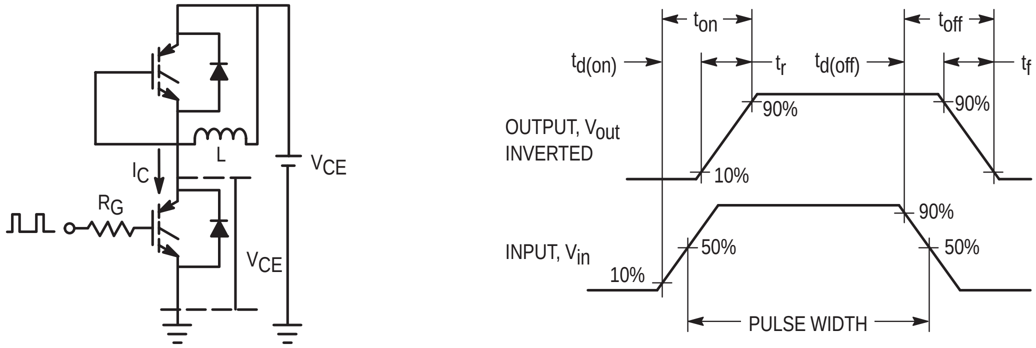


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

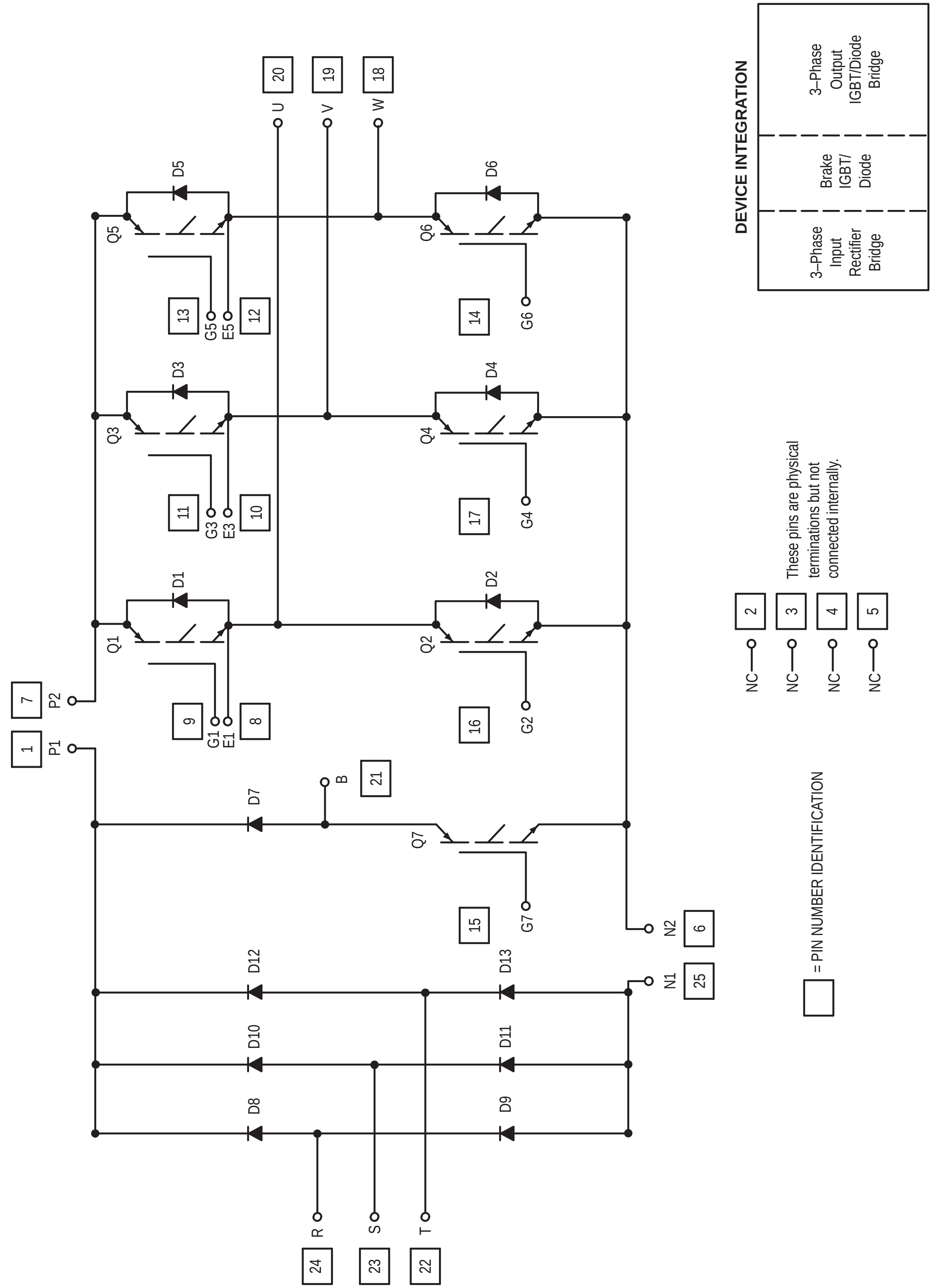


Figure 20. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 3.0 hp Motor Drives

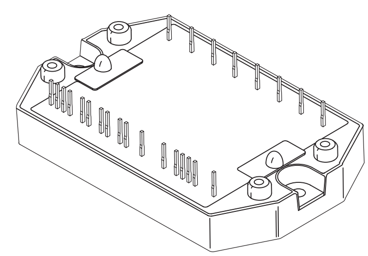
(This device is not recommended for new designs)
(This device is replaced by MHPM7A30E60DC3)

MHPM7A30A60B

**30 AMP, 600 VOLT
HYBRID POWER MODULE**

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 300V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440A–02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Average Output Rectified Current	I_O	30	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	360	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	30	A
Peak Repetitive IGBT Collector Current – (PW = 1.0 ms)(2)	$I_{C(pk)}$	60	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	30	A
Peak Repetitive Free-Wheeling Diode Current – (PW = 1.0 ms)(2)	$I_{F(pk)}$	60	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	85	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 300V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	30	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	60	A
IGBT Power Dissipation (T_C = 95°C)	PD	85	W
Peak Repetitive Output Diode Reverse Voltage (T_C = 95°C)	V_{RRM}	600	V
Continuous Output Diode Current	I_{Fmax}	30	A
Peak Output Diode Current (PW = 1.0 ms) (2)	$I_{F(pk)}$	60	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 600 V)	I_R	–	5.0	50	µA
Forward Voltage (I_F = 30 A)	V_F	–	1.16	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100 –	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (I_C = 30 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.3	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	6600	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V)	Q_T	–	220	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(on)}$ = 39 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 30 A, V_{GE} = 0 V)	V_F	–	1.3	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 30 A, V = 300 V, di/dt = 150 A/µs)	t_{rr}	–	150	200	ns
Free Wheeling Diode Stored Charge (I_F = 30 A, V = 300 V, di/dt = 150 A/µs)	Q_{rr}	–	1580	2300	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.2	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100 –	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 30 A)	$V_{CE(SAT)}$	–	2.3	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	6600	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V)	Q_T	–	220	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(on)}$ = 39 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Output Diode Forward Voltage (I_F = 30 A)	V_F	–	1.3	2.0	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.2	°C/W
Thermal Resistance – Diode	$R_{\theta JC}$	–	–	2.7	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	–	5.0	–	mΩ
Resistance Tolerance	R_{tol}	–1.0	–	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	–	0.660	–	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	–	–1.95	–	mV/°C

Typical Characteristics

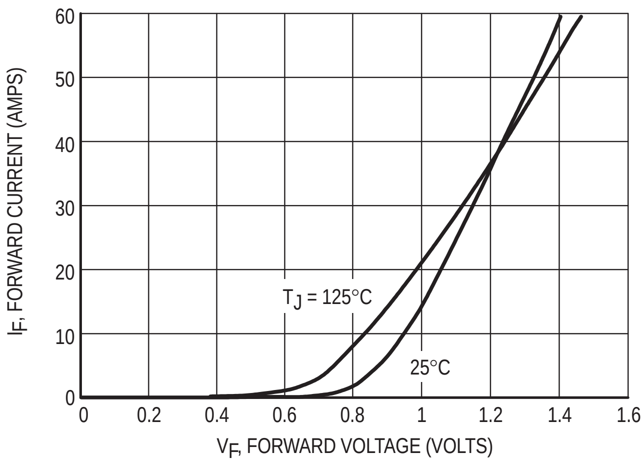


Figure 1. Forward Characteristics — Input Rectifier

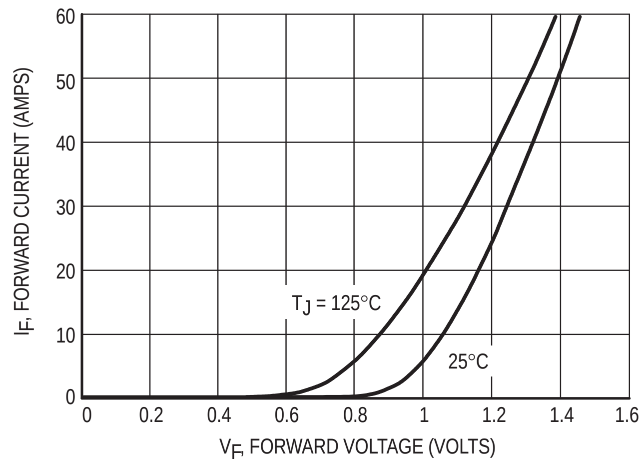


Figure 2. Forward Characteristics — Free–Wheeling Diode

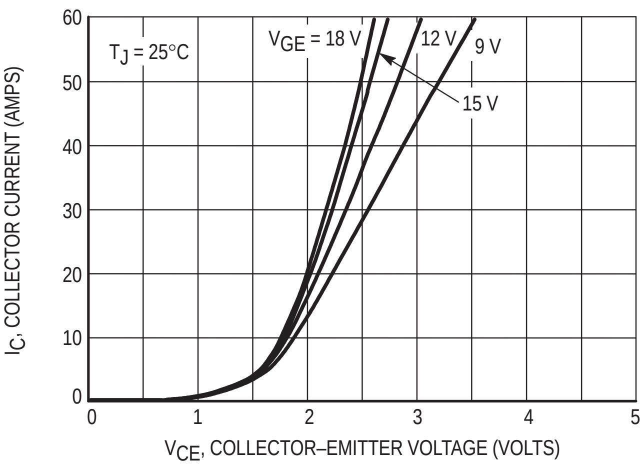


Figure 3. Forward Characteristics, T_J = 25°C

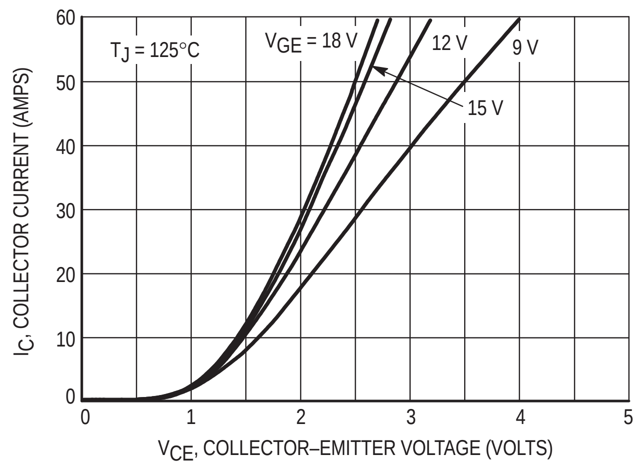


Figure 4. Forward Characteristics, T_J = 125°C

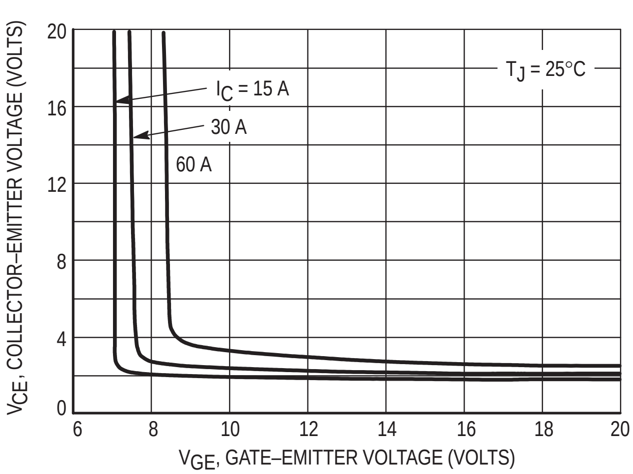


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

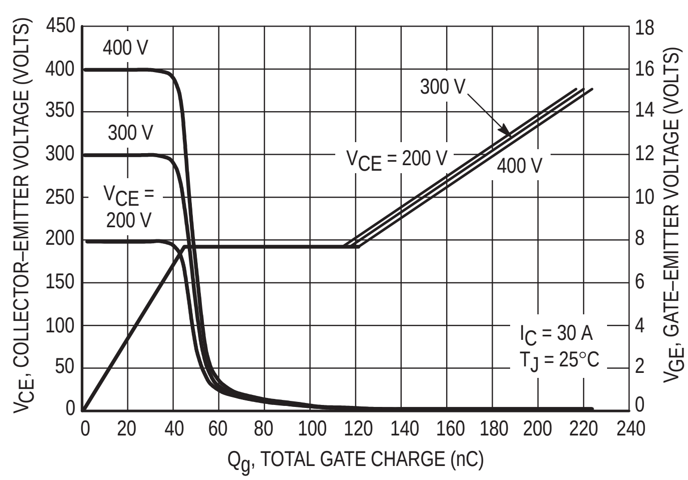


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

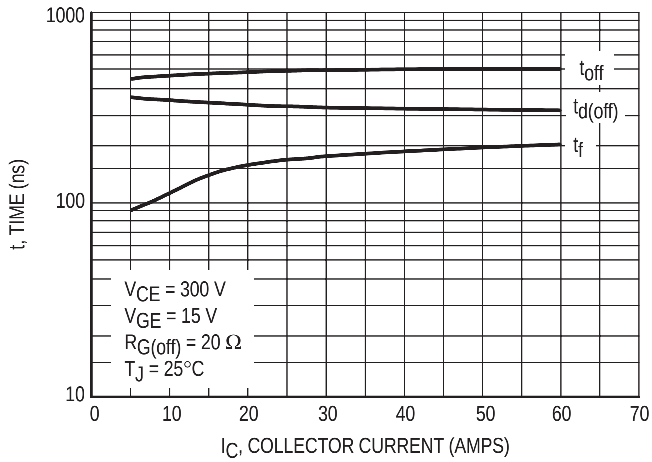


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

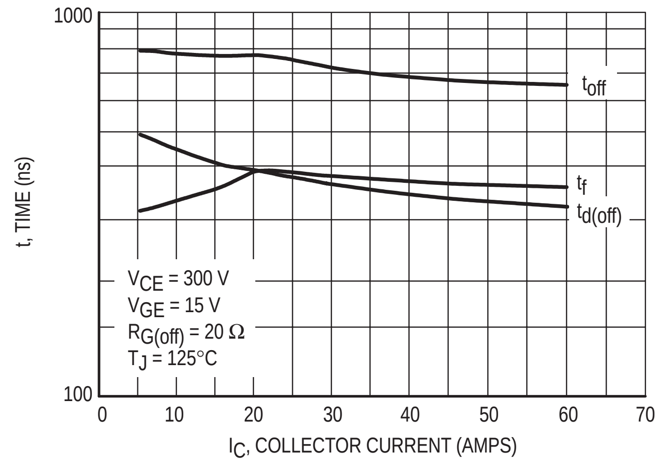


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

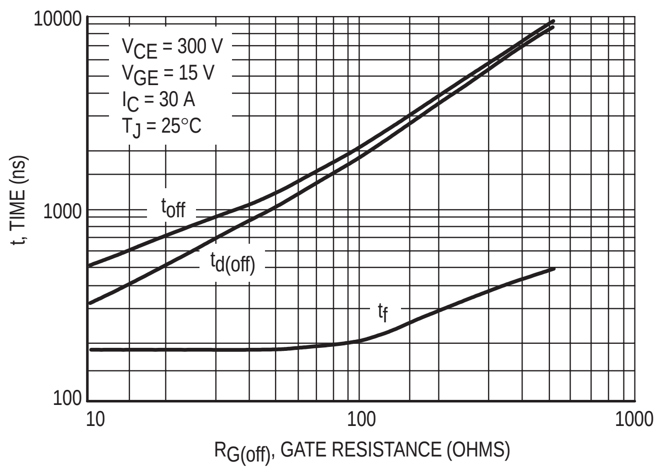


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

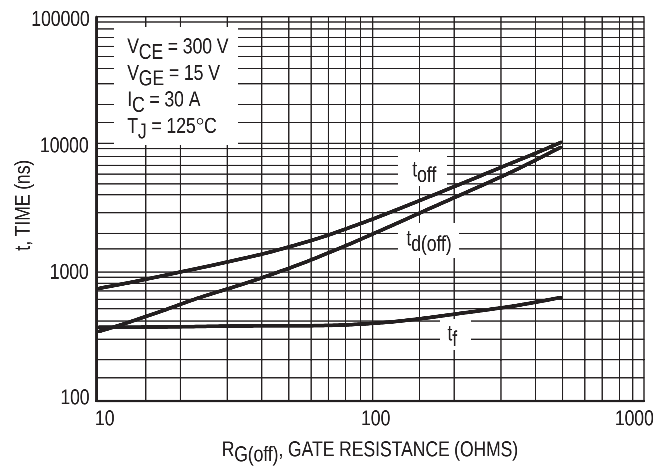


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

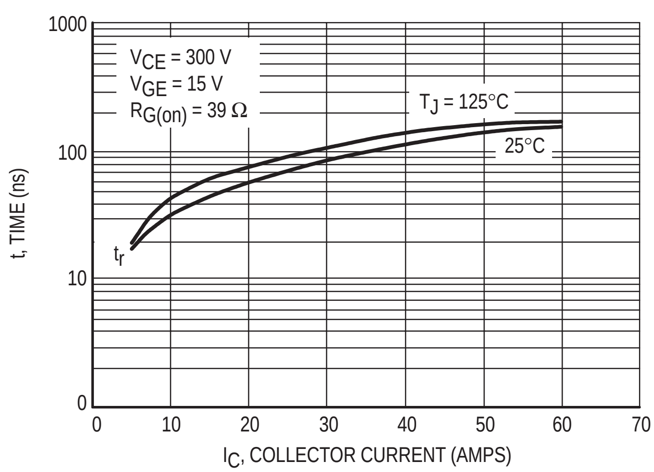


Figure 11. Inductive Switching Times versus Collector Current

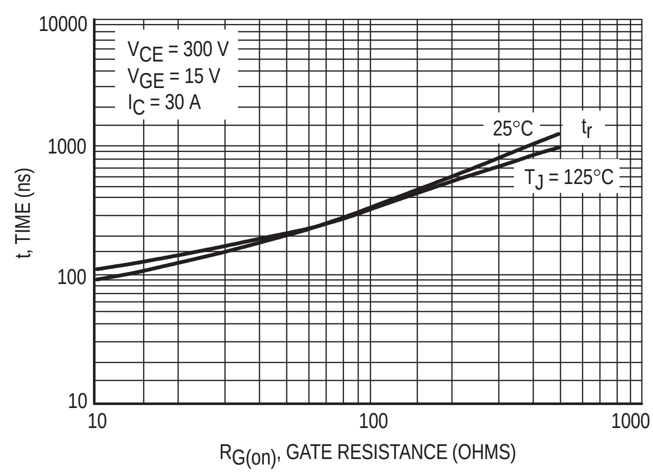


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

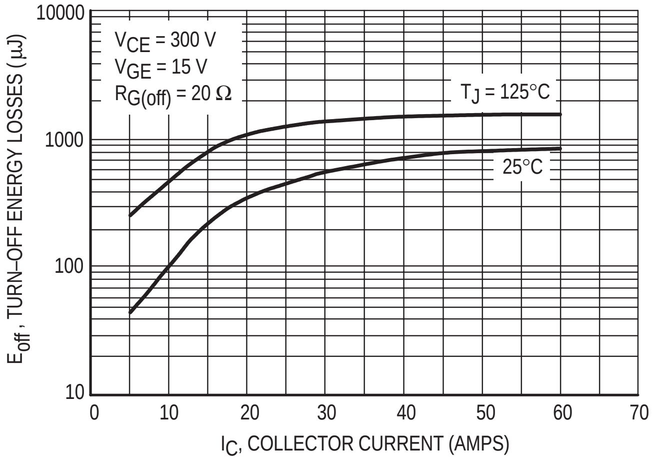


Figure 13. Turn–Off Energy Losses versus Collector Current

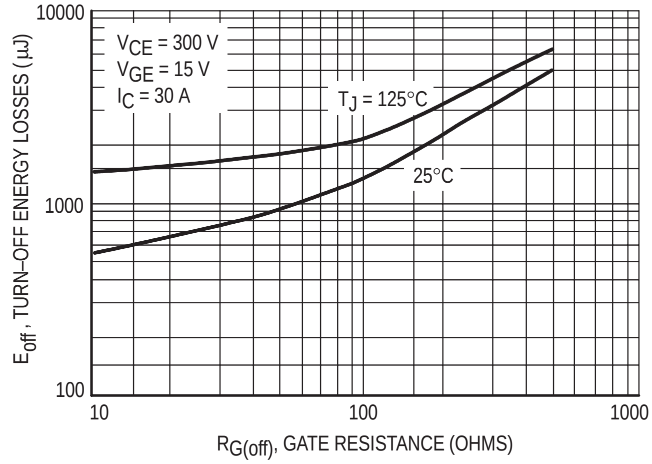


Figure 14. Turn–Off Energy Losses versus Gate Resistance

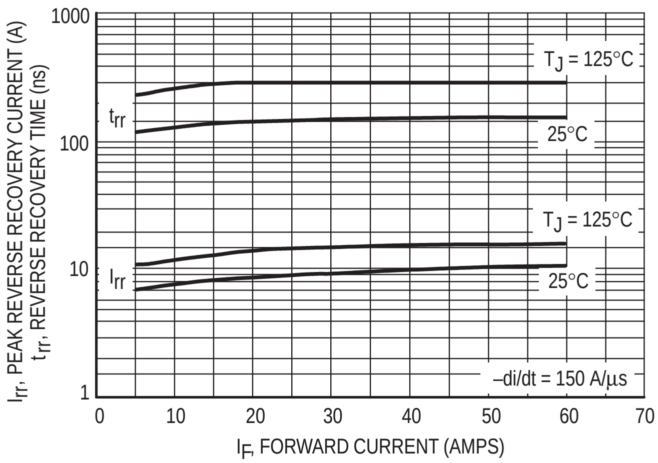


Figure 15. Reverse Recovery Characteristics — Free–Wheeling Diode

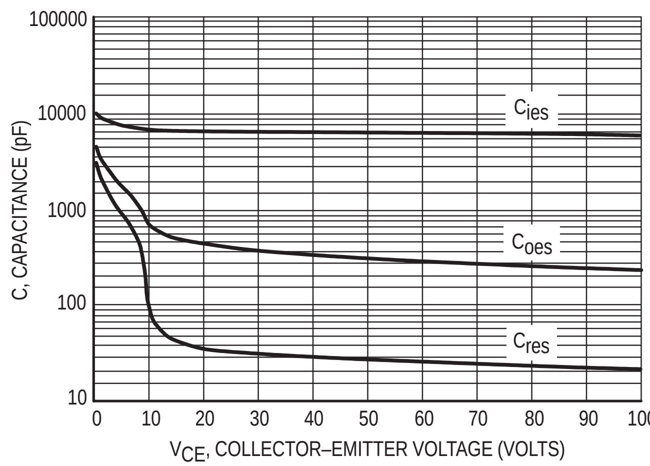


Figure 16. Capacitance Variation

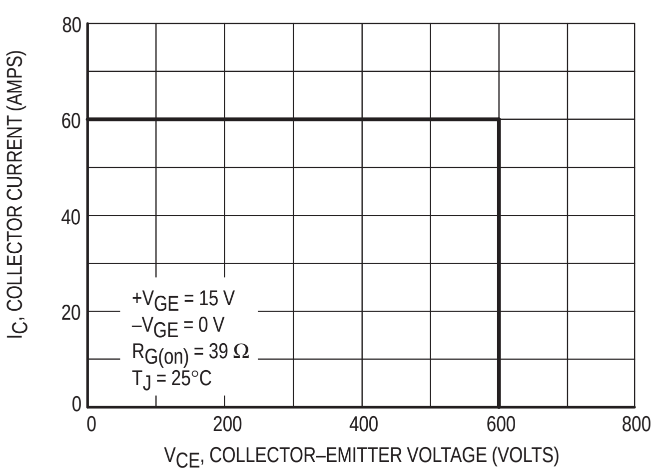


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

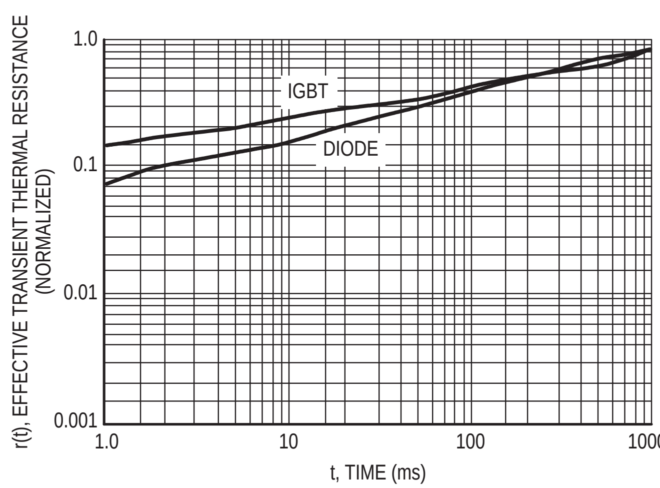


Figure 18. Thermal Response

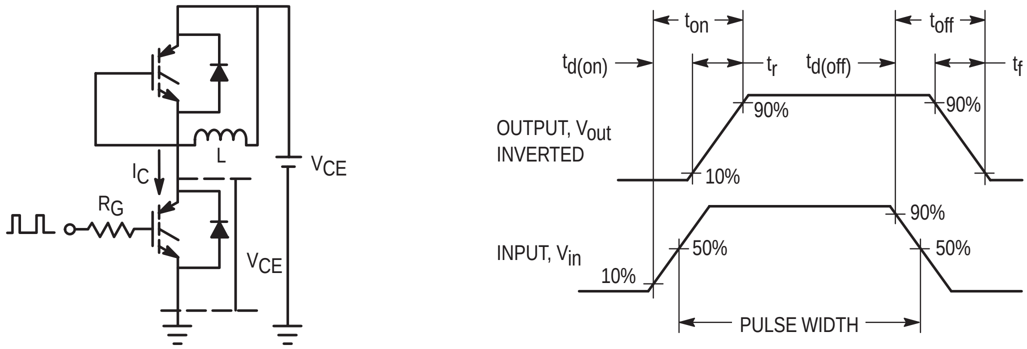


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

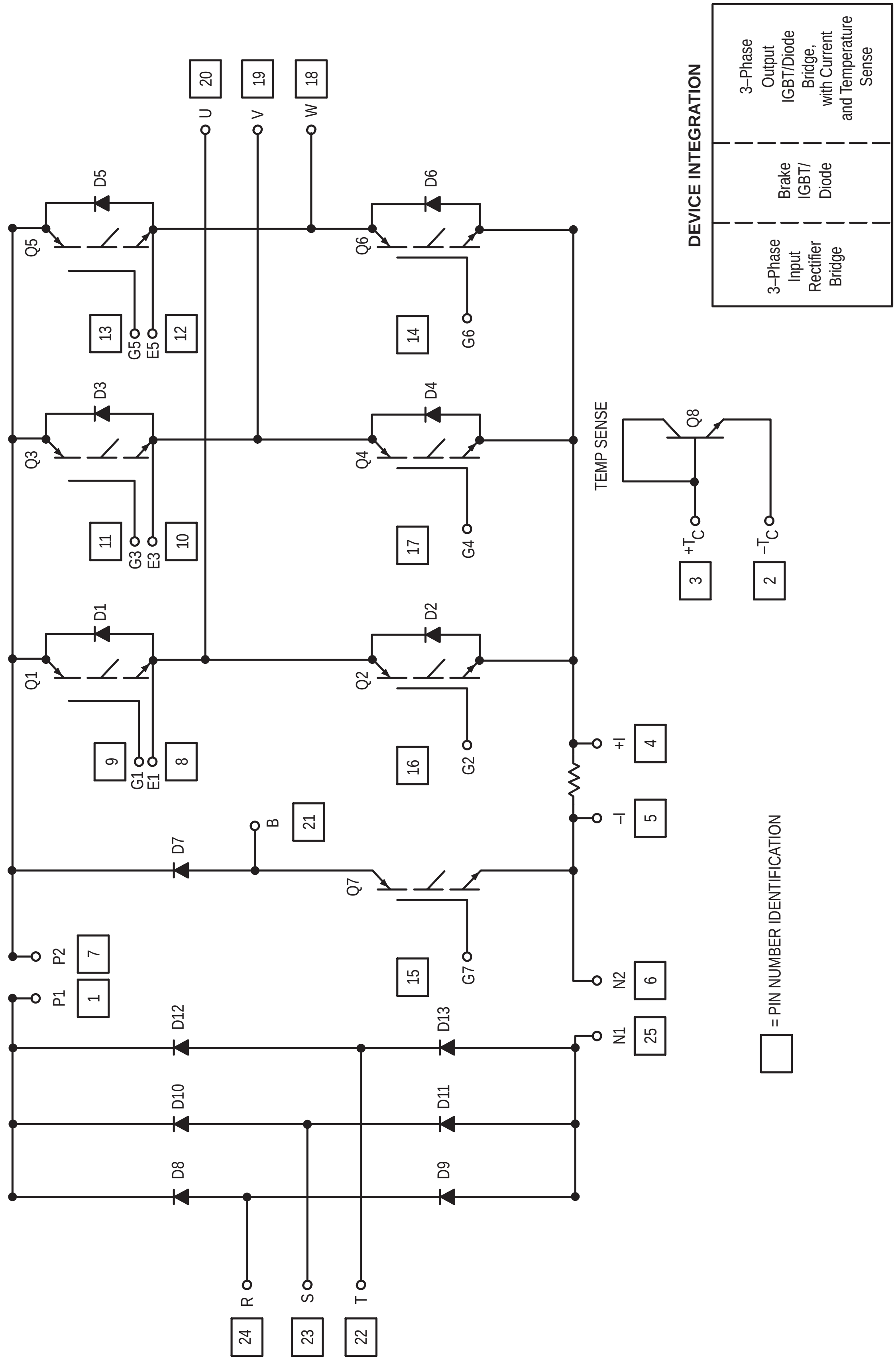


Figure 20. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 3.0 hp Motor Drives

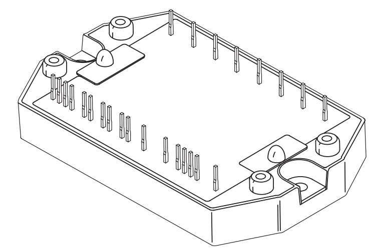
(This device is not recommended for new designs)
(This device is replaced by MHPM7A30E60DC3)

MHPM7B30A60B

30 AMP, 600 VOLT
HYBRID POWER MODULE

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 300V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440A–02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	600	V
Average Output Rectified Current	I_O	30	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	360	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	30	A
Peak Repetitive IGBT Collector Current – (PW = 1.0 ms)(2)	$I_{C(pk)}$	60	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	30	A
Peak Free-Wheeling Diode Current – (PW = 1.0 ms) (2)	$I_{F(pk)}$	60	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	85	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 300V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	600	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	30	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	60	A
IGBT Power Dissipation (T_C = 95°C)	PD	85	W
Peak Repetitive Output Diode Reverse Voltage (T_C = 95°C)	V_{RRM}	600	V
Continuous Output Diode Current	I_{Fmax}	30	A
Peak Output Diode Current (PW = 1.0 ms)(2)	$I_{F(pk)}$	60	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 600 V)	I_R	–	5.0	50	µA
Forward Voltage (I_F = 30 A)	V_F	–	1.16	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100 –	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (I_C = 30 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.3	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	6600	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V)	Q_T	–	220	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(on)}$ = 39 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 30 A, V_{GE} = 0 V)	V_F	–	1.3	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 30 A, V = 300 V, di/dt = 150 A/µs)	t_{rr}	–	150	200	ns
Free Wheeling Diode Stored Charge (I_F = 30 A, V = 300 V, di/dt = 150 A/µs)	Q_{rr}	–	1580	2300	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.2	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 600 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100 –	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	600	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 30 A)	$V_{CE(SAT)}$	–	2.3	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	6600	–	pF
Input Gate Charge (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V)	Q_T	–	220	–	nC
Fall Time – Inductive Load (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(on)}$ = 39 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 300 V, I_C = 30 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Output Diode Forward Voltage (I_F = 30 A)	V_F	–	1.3	2.0	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.2	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.7	°C/W

Typical Characteristics

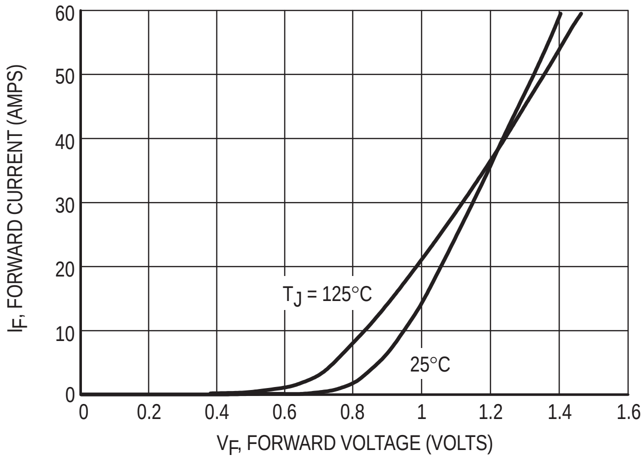


Figure 1. Forward Characteristics — Input Rectifier

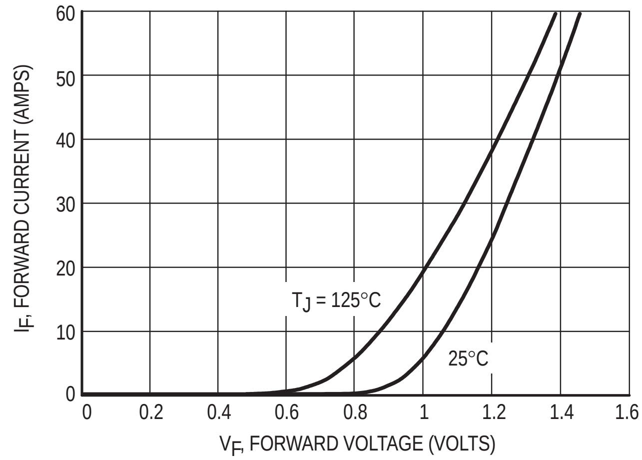


Figure 2. Forward Characteristics — Free–Wheeling Diode

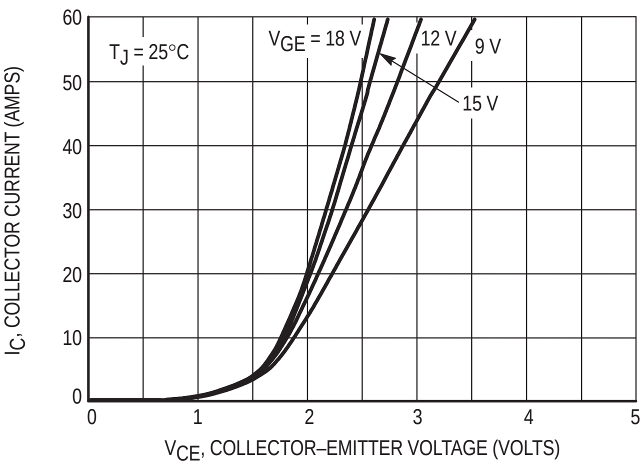


Figure 3. Forward Characteristics, T_J = 25°C

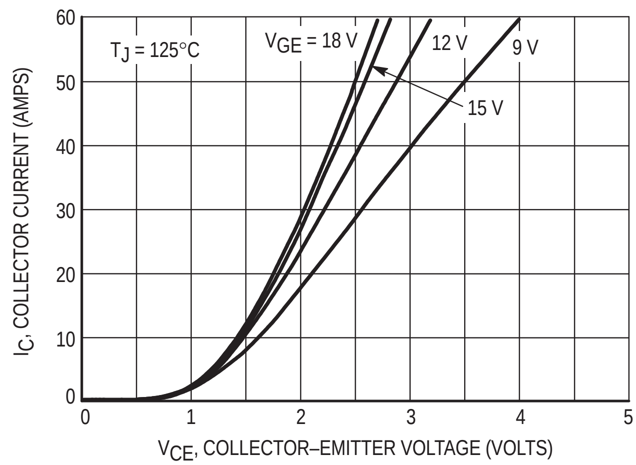


Figure 4. Forward Characteristics, T_J = 125°C

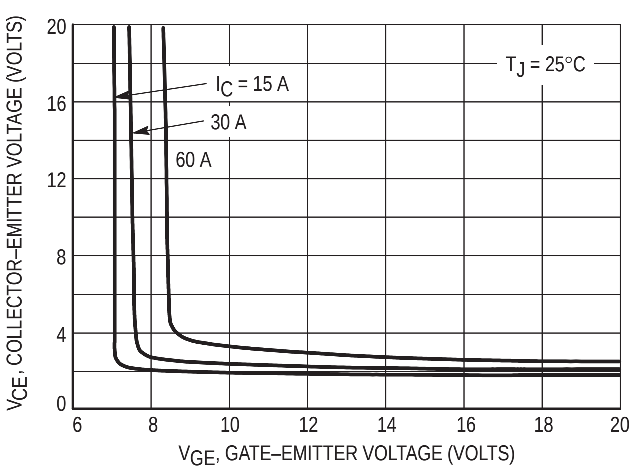


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

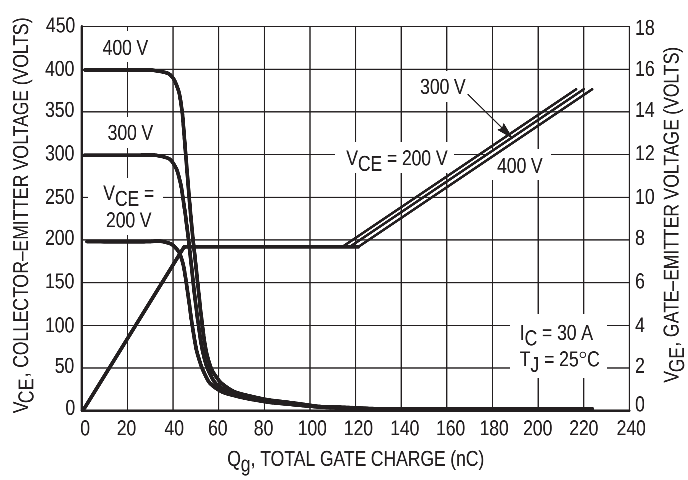


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

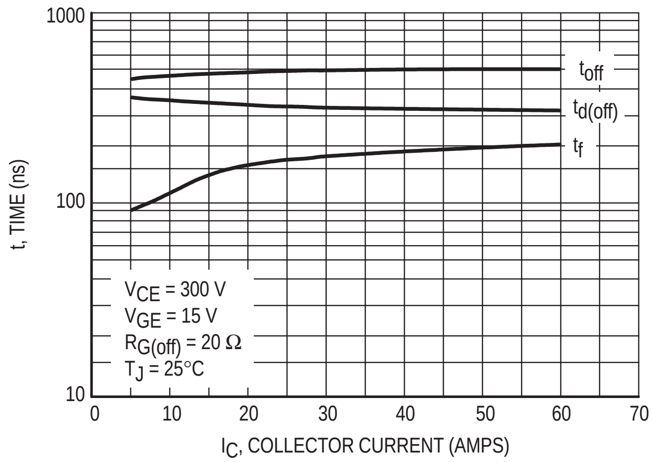


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

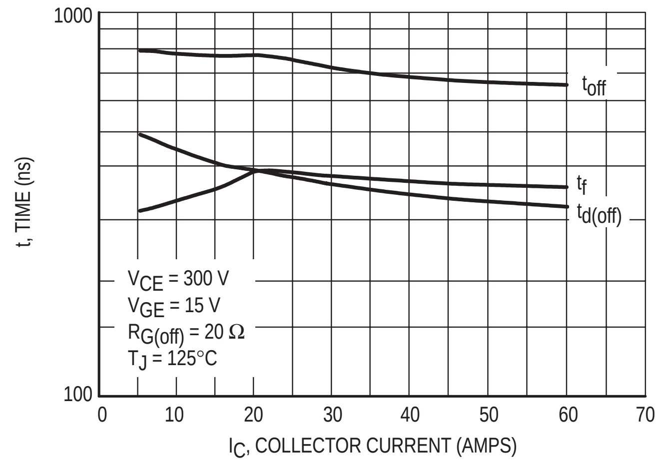


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

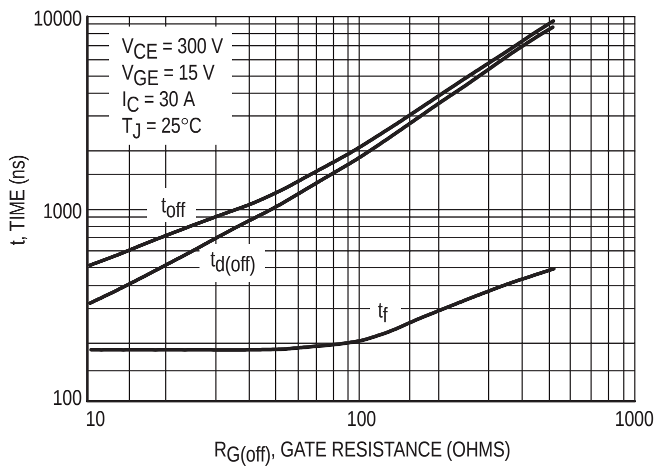


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

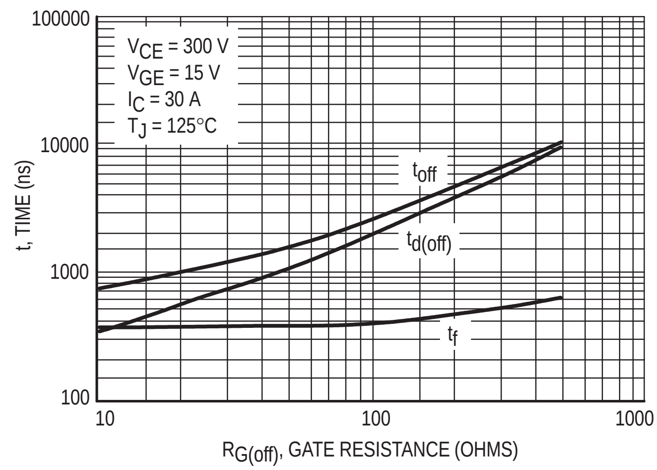


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

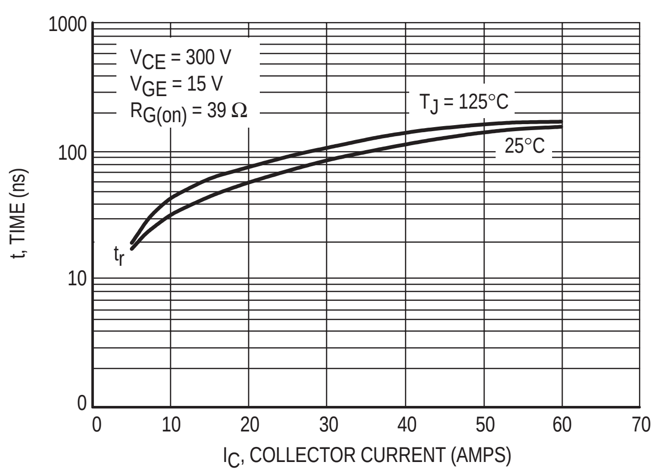


Figure 11. Inductive Switching Times versus Collector Current

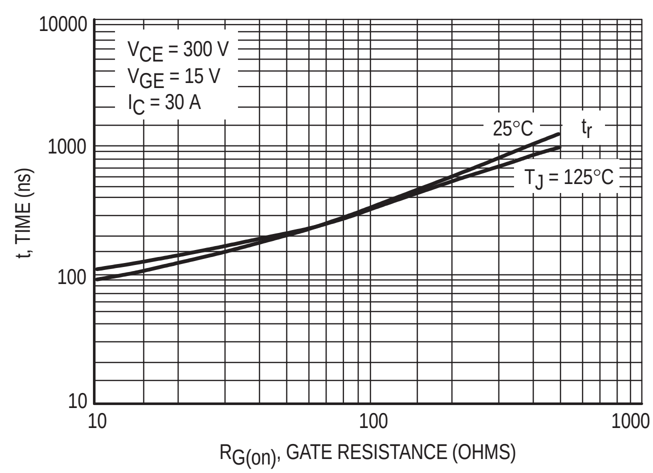


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

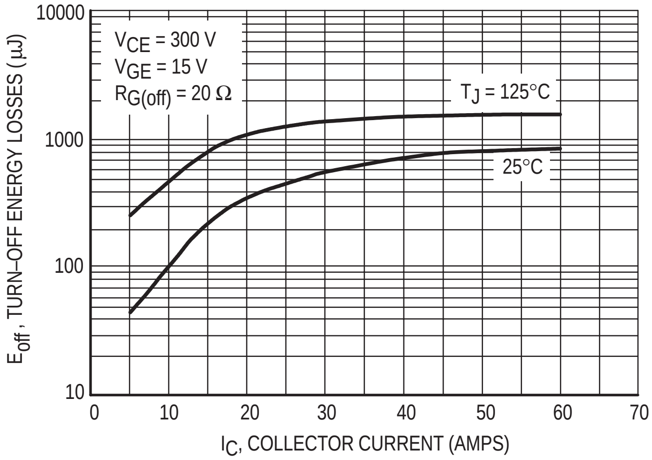


Figure 13. Turn–Off Energy Losses versus Collector Current

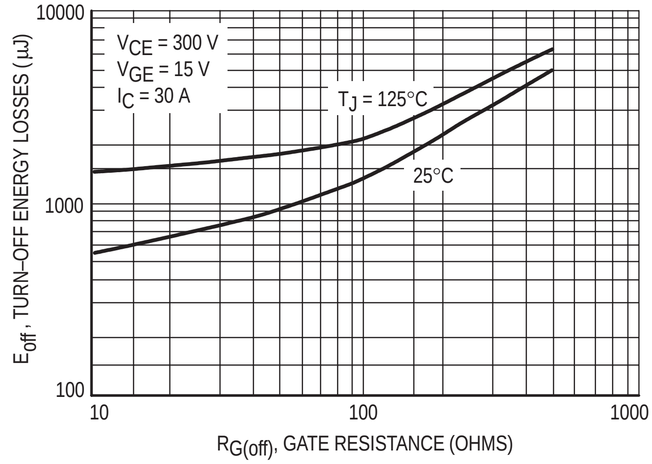


Figure 14. Turn–Off Energy Losses versus Gate Resistance

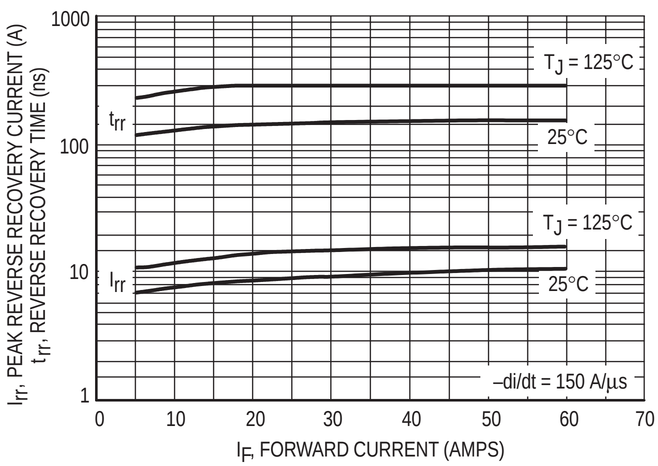


Figure 15. Reverse Recovery Characteristics — Free–Wheeling Diode

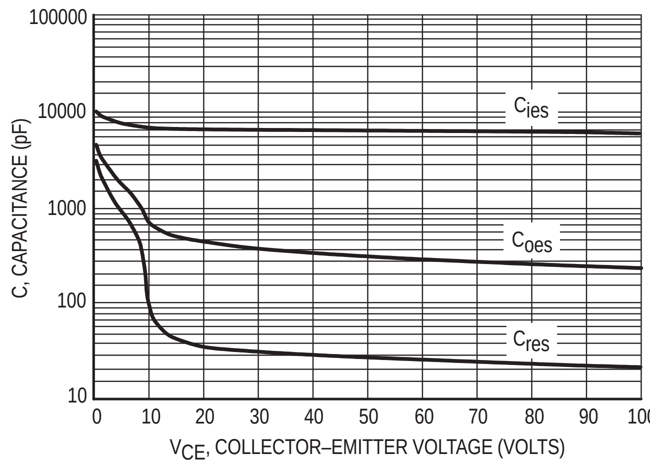


Figure 16. Capacitance Variation

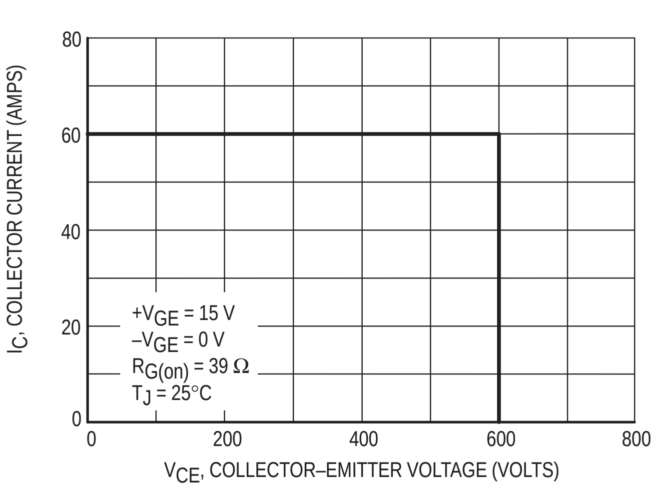


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

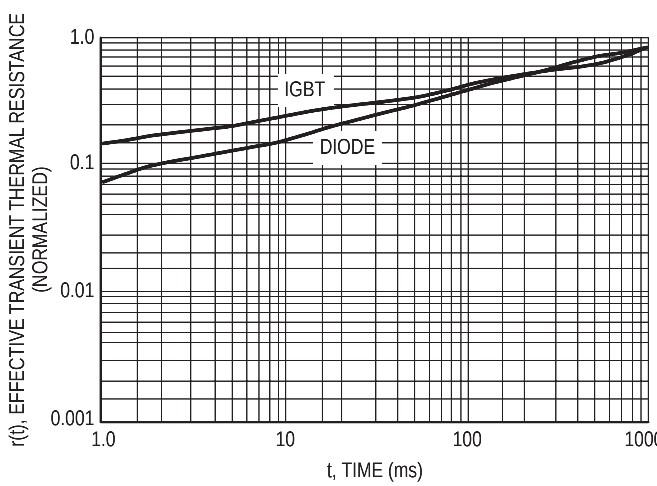


Figure 18. Thermal Response

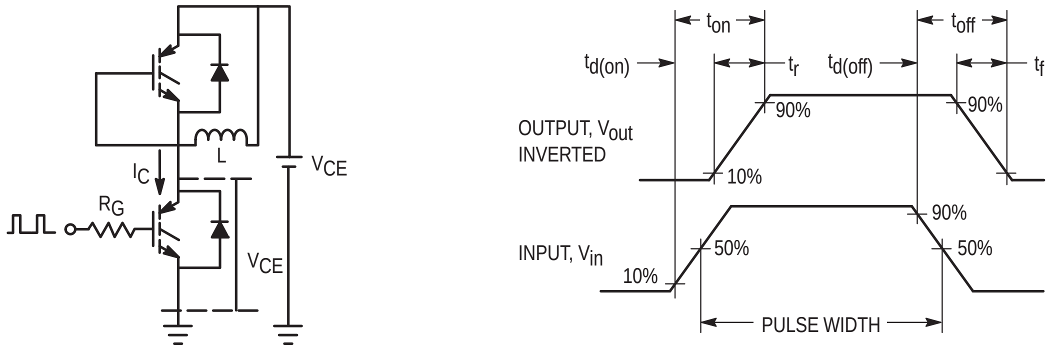


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

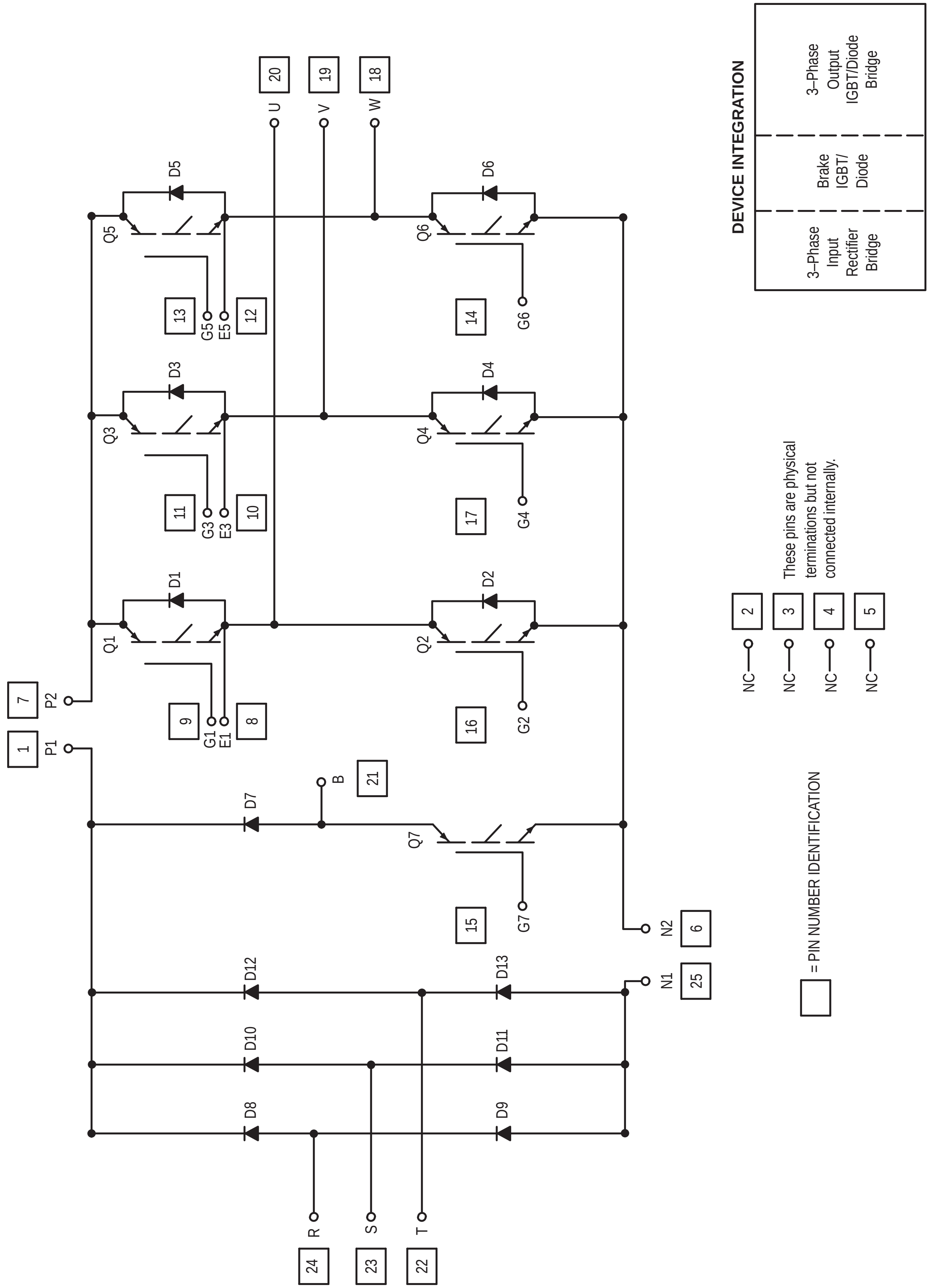


Figure 20. Integrated Power Stage Schematic

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

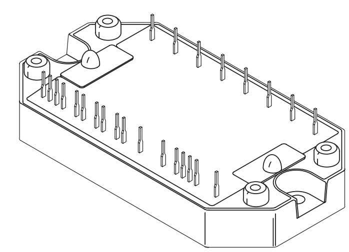
Hybrid Power Module

Integrated Power Stage for 1.0 hp Motor Drives

(This device is not recommended for new designs)
(This device is replaced by MHPM7A5S120DC3)

MHPM7A8A120A

8.0 AMP, 1200 VOLT
HYBRID POWER MODULE



PLASTIC PACKAGE
CASE 440-02, Style 1

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 600V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	8.0	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	8.0	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	16	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	8.0	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	16	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	50	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	30	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz

(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	8.0	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	16	A
IGBT Power Dissipation (T_C = 95°C)	PD	50	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	8.0	A
Peak Output Diode Current(2)	$I_{F(pk)}$	16	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	–	5.0	50	µA
Forward Voltage (I_F = 8.0 A)	V_F	–	0.95	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 8.0 A)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	–	930	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V)	Q_T	–	35	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	290	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(on)}$ = 270 Ω)	E_{on}	–	–	1.5	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	1.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 8.0 A, V_{GE} = 0 V)	V_F	–	1.8	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 8.0 A, V = 600 V, di/dt = 100 A/µs)	t_{rr}	–	130	200	ns
Free Wheeling Diode Stored Charge (I_F = 8.0 A, V = 600 V, di/dt = 100 A/µs)	Q_{rr}	–	–	900	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	2.2	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	3.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 8.0 A)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	930	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V)	Q_T	–	35	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	290	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(on)}$ = 270 Ω)	E_{on}	–	–	1.5	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	1.0	mJ
Output Diode Forward Voltage (I_F = 8.0 A)	V_F	–	1.8	2.2	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	2.2	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	3.7	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	–	10	–	mΩ
Resistance Tolerance	R_{tol}	–1.0	–	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	–	0.660	–	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	–	–1.95	–	mV/°C

Typical Characteristics

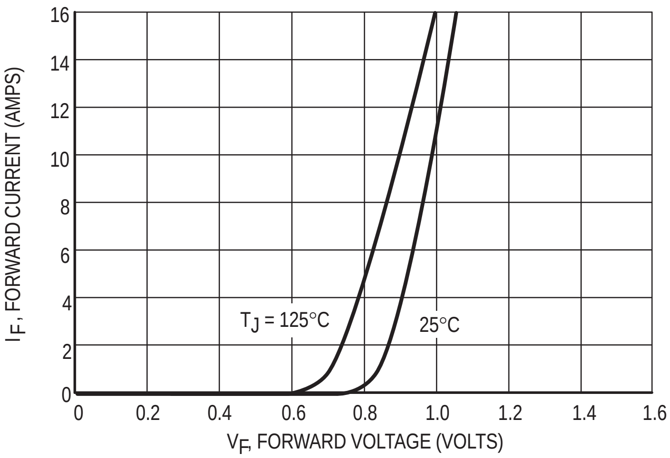


Figure 1. Forward Characteristics – Input Rectifier

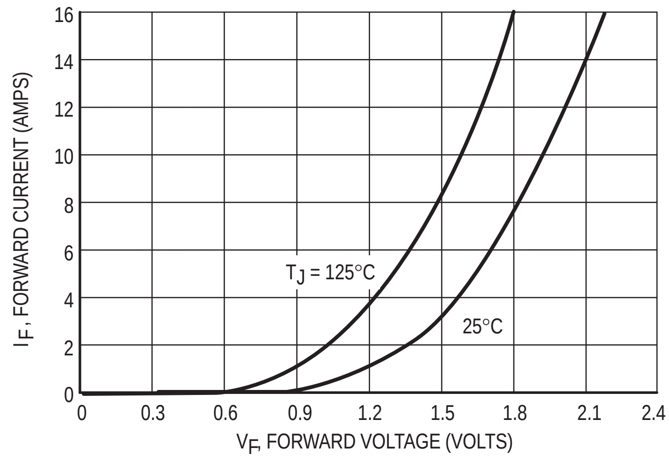


Figure 2. Forward Characteristics – Free–Wheeling Diode

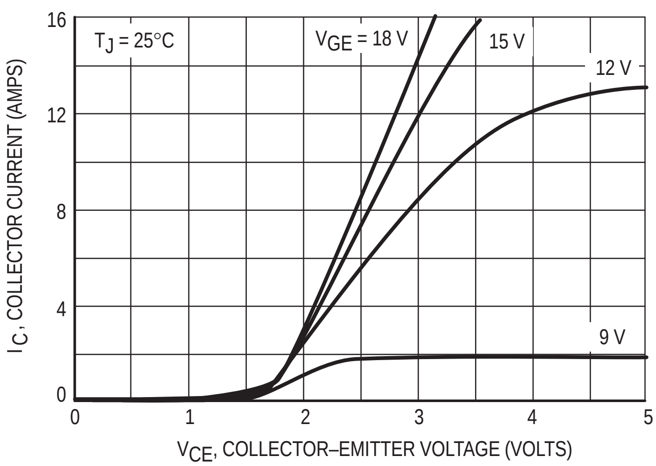


Figure 3. Forward Characteristcs, T_J = 25°C

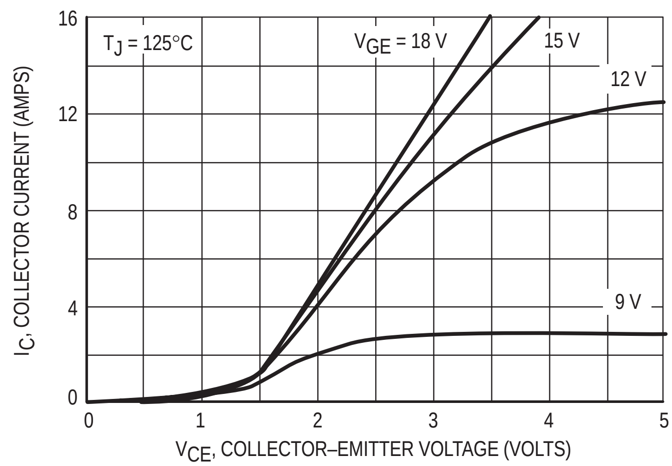


Figure 4. Forward Characteristcs, T_J = 125°C

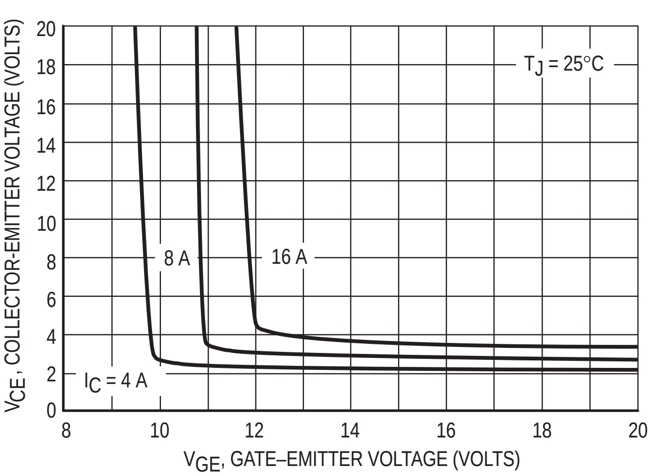


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

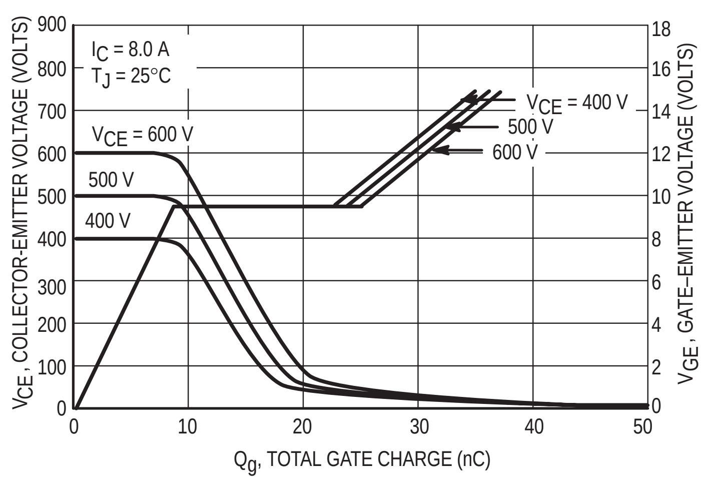


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

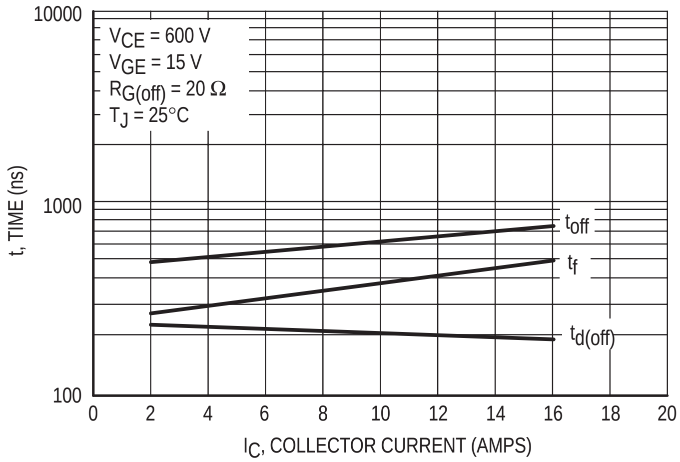


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

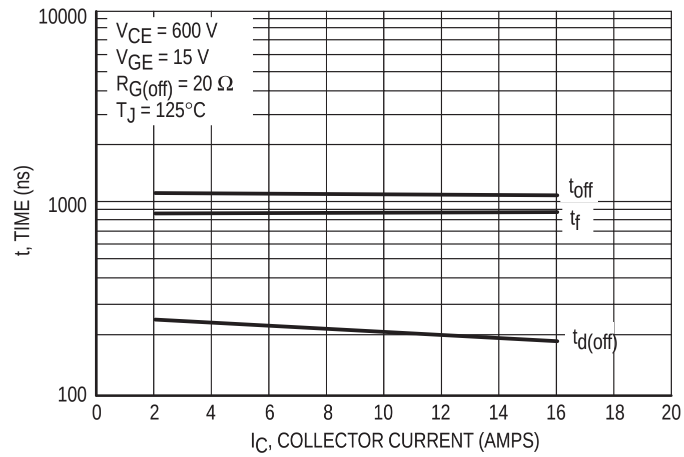


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

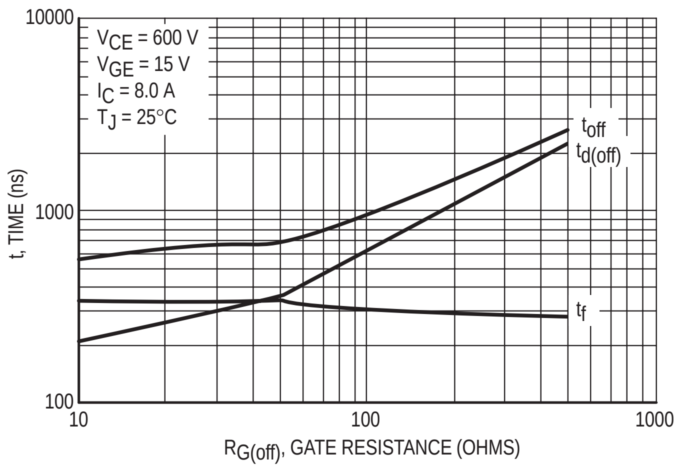


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

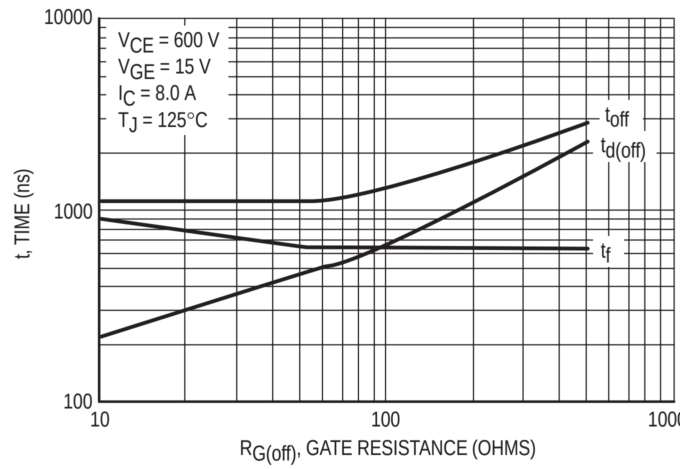


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

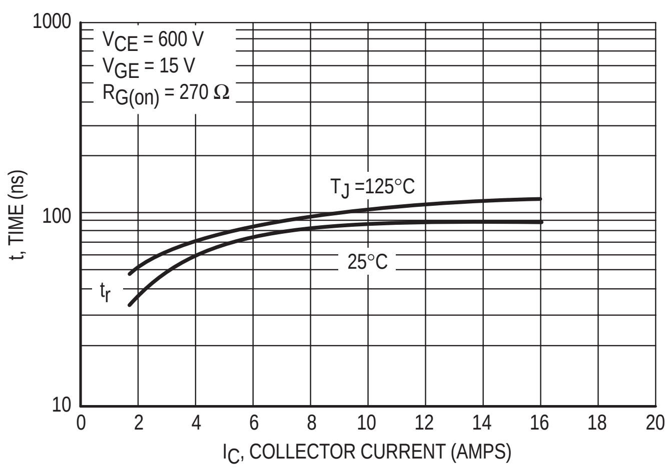


Figure 11. Inductive Switching Times versus Collector Current

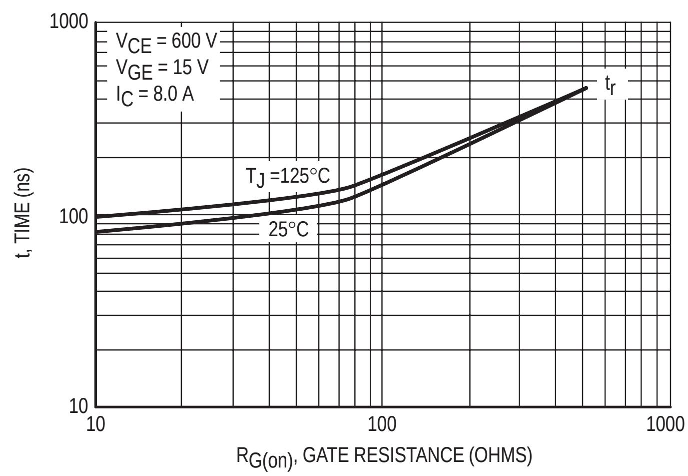


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

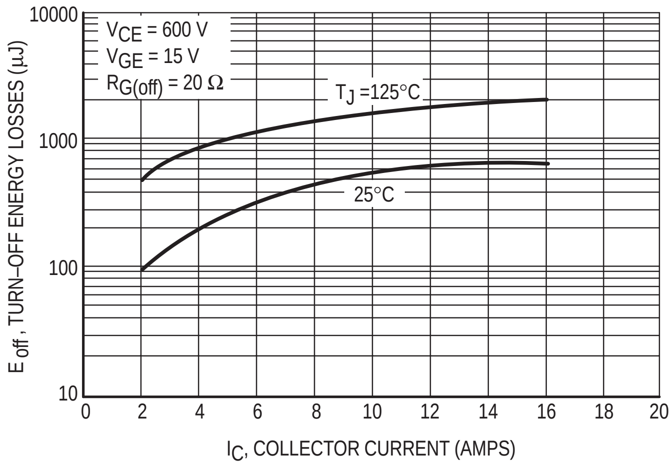


Figure 13. Turn–Off Energy Losses versus Collector Current

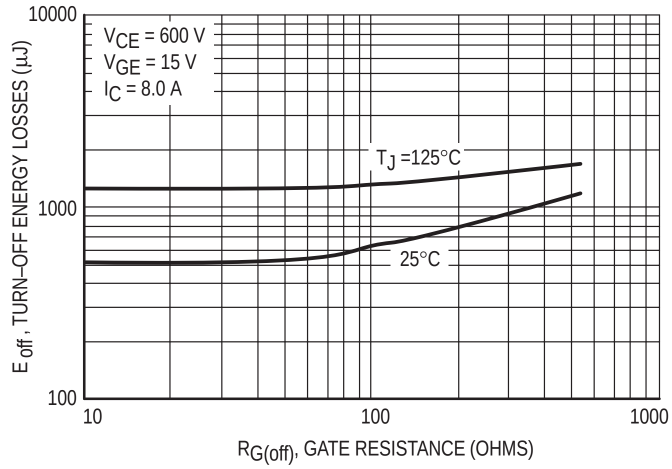


Figure 14. Turn–Off Energy Losses versus Gate Resistance

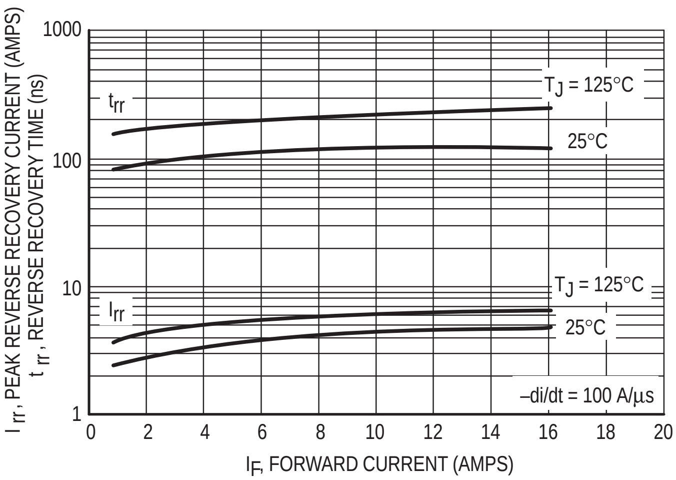


Figure 15. Reverse Recovery Characteristics – Free–Wheeling Diode

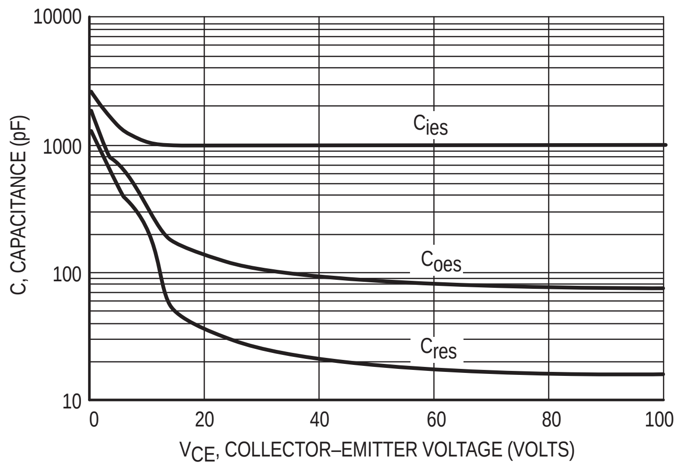


Figure 16. Capacitance Variation

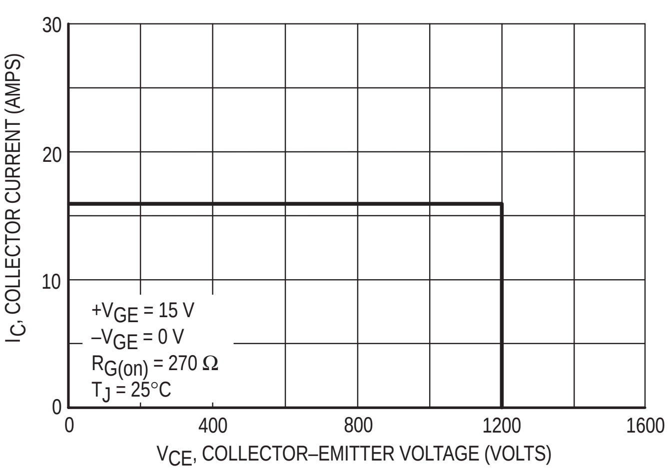


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

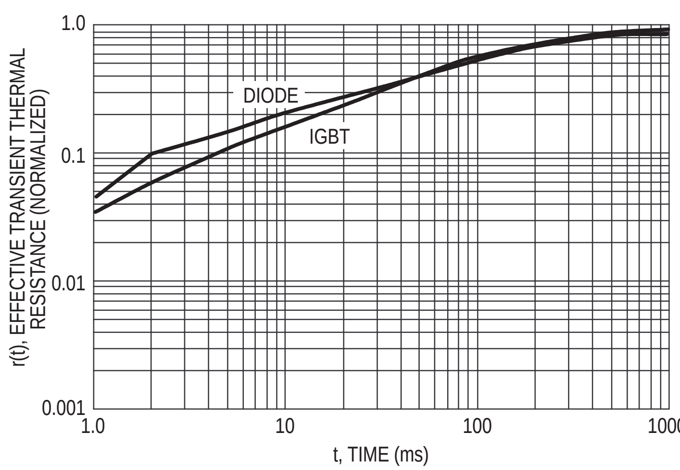


Figure 18. Thermal Response

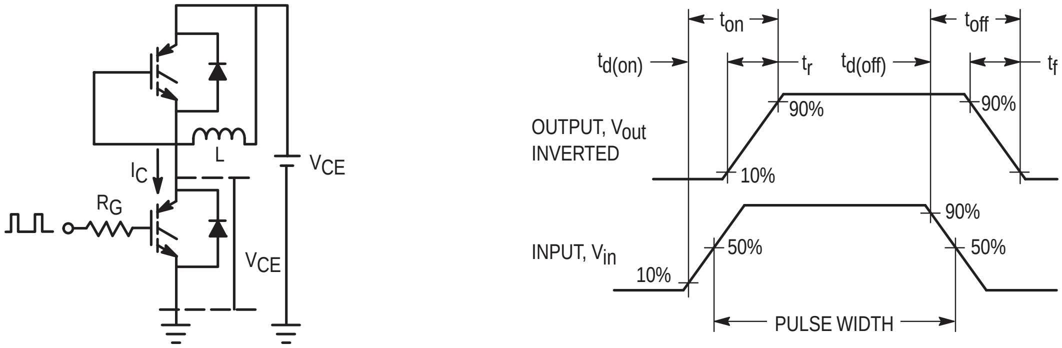


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

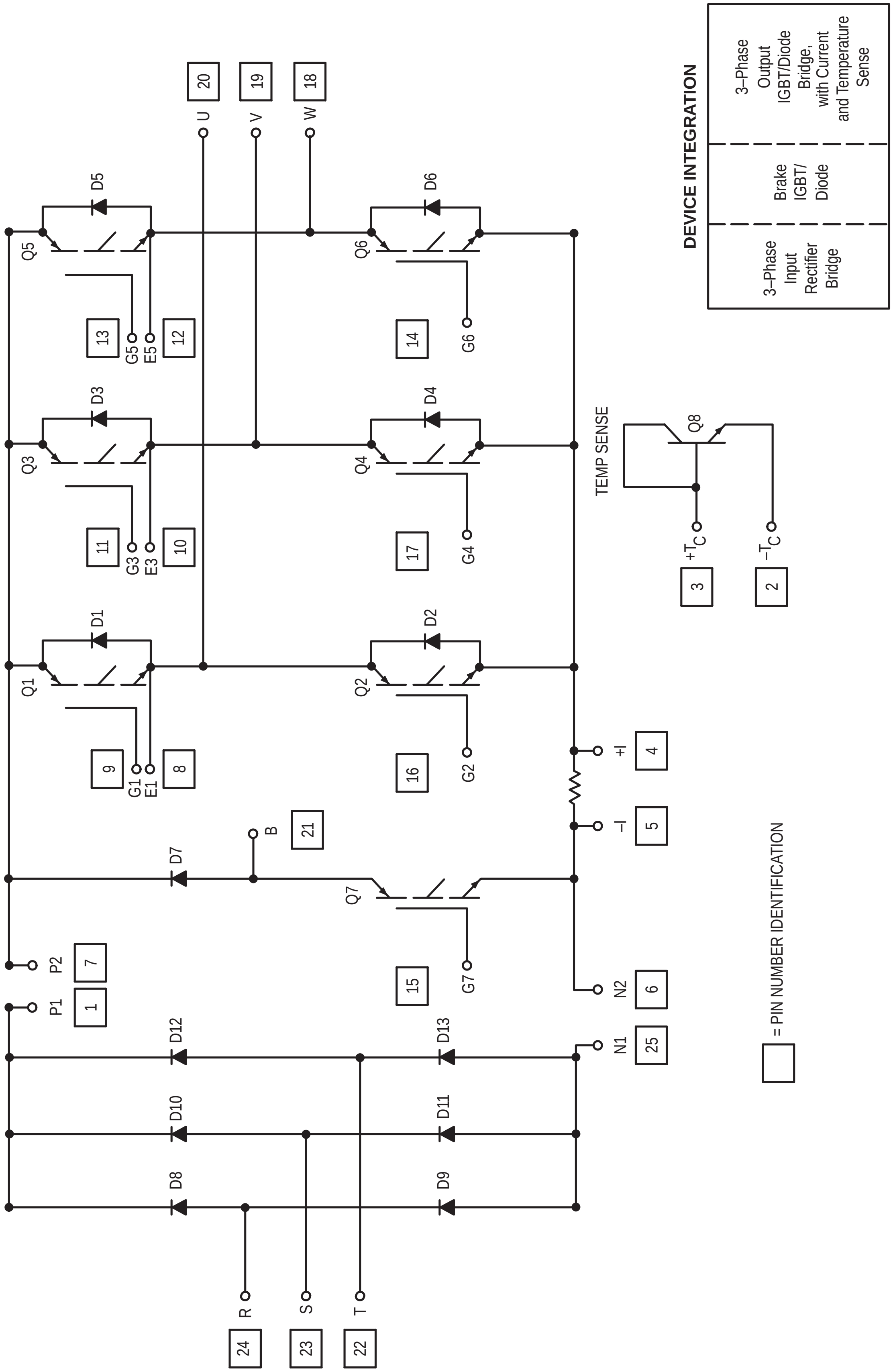


Figure 20. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 1.0 hp Motor Drives

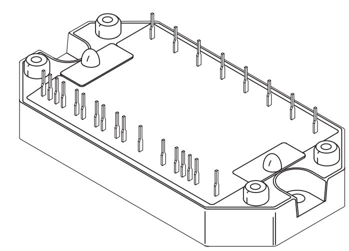
(This device is not recommended for new designs)
(This device is replaced by MHPM7A5S120DC3)

MHPM7B8A120A

8.0 AMP, 1200 VOLT
HYBRID POWER MODULE

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 600V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440-02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	8.0	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	8.0	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	16	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	8.0	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	16	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	50	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	30	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	8.0	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	16	A
IGBT Power Dissipation (T_C = 95°C)	PD	50	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	8.0	A
Peak Output Diode Current(2)	$I_{F(pk)}$	16	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	–	5.0	50	μA
Forward Voltage (I_F = 8.0 A)	V_F	–	1.9	2.65	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	μA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 500	 100	μA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 8.0 A)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 25 V, f = 1.0 MHz)	C_{ies}	–	930	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V)	Q_T	–	35	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	250	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(on)}$ = 270 Ω)	E_{on}	–	–	1.5	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	1.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 8.0 A, V_{GE} = 0 V)	V_F	–	1.8	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 8.0 A, V = 600 V, di/dt = 100 A/μs)	t_{rr}	–	140	200	ns
Free Wheeling Diode Stored Charge (I_F = 8.0 A, V = 600 V, di/dt = 100 A/μs)	Q_{rr}	–	–	900	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	2.2	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	3.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 500	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 8.0 A)	$V_{CE(SAT)}$	–	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	930	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V)	Q_T	–	35	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_{fi}	–	250	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(on)}$ = 270 Ω)	$E_{(on)}$	–	–	1.5	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 8.0 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	$E_{(off)}$	–	–	1.0	mJ
Output Diode Forward Voltage (I_F = 8.0 A)	V_F	–	1.8	2.2	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	2.2	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	3.7	°C/W

Typical Characteristics

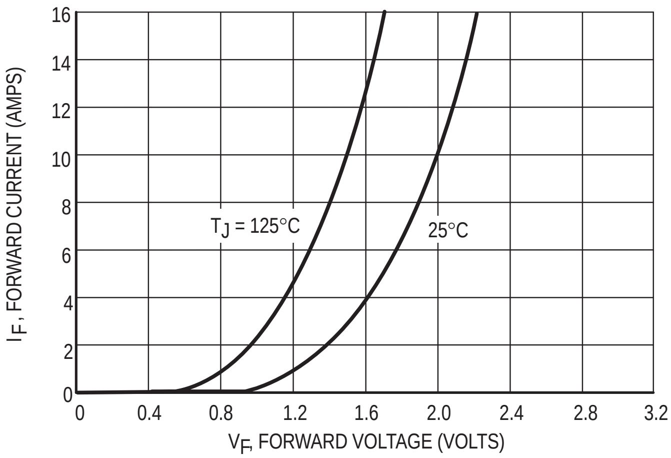


Figure 1. Forward Characteristics – Input Rectifier

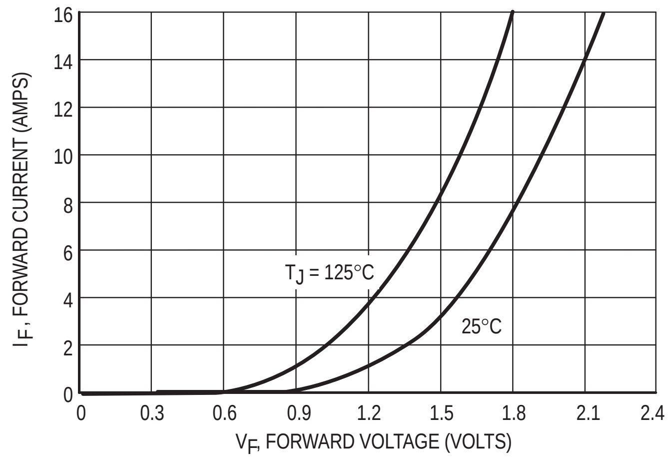


Figure 2. Forward Characteristics – Free–Wheeling Diode

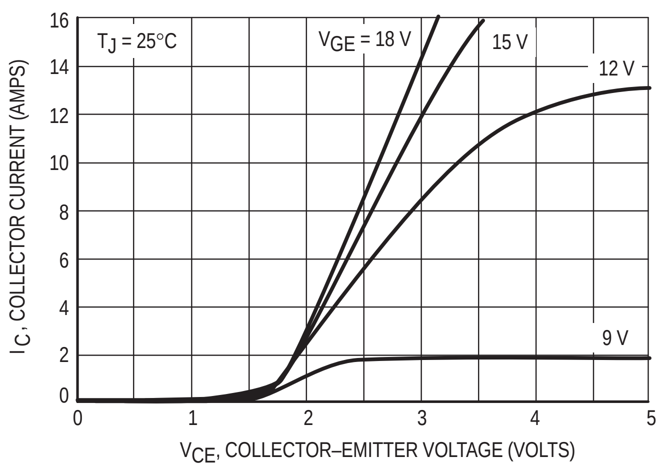


Figure 3. Forward Characteristcs, T_J = 25°C

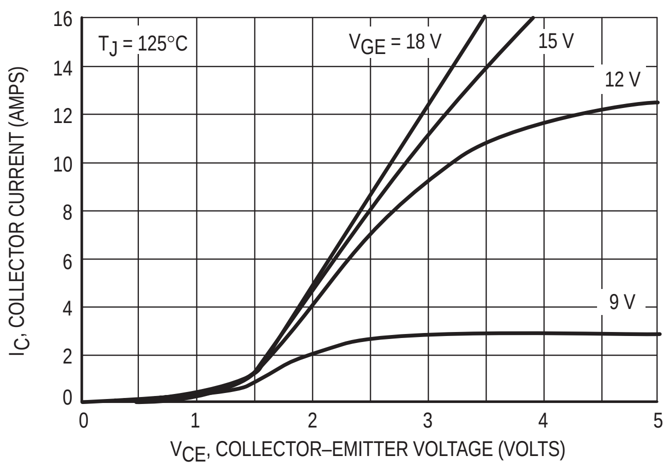


Figure 4. Forward Characteristcs, T_J = 125°C

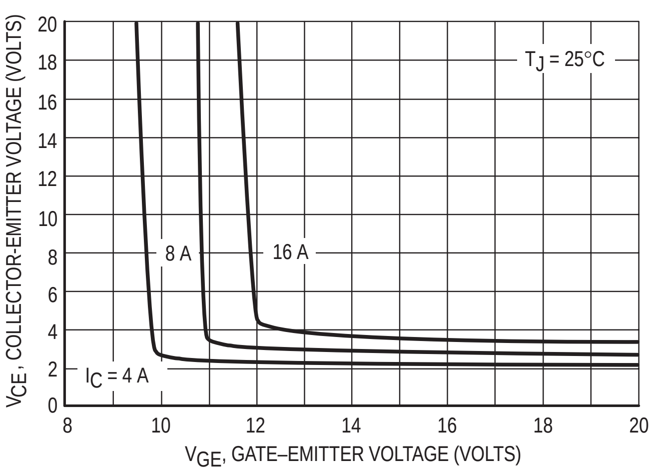


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

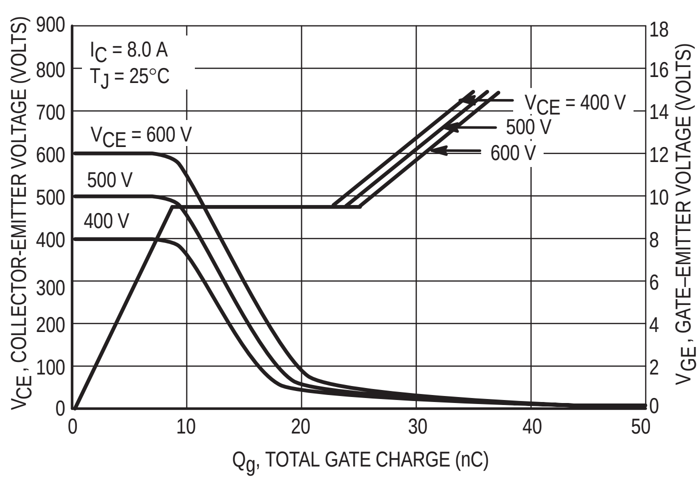


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

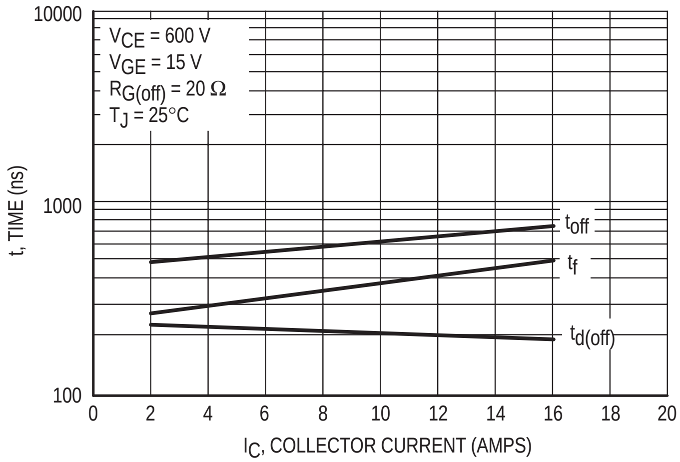


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

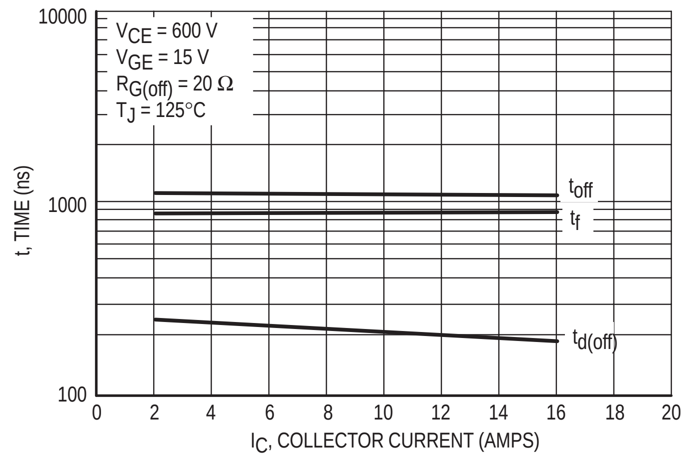


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

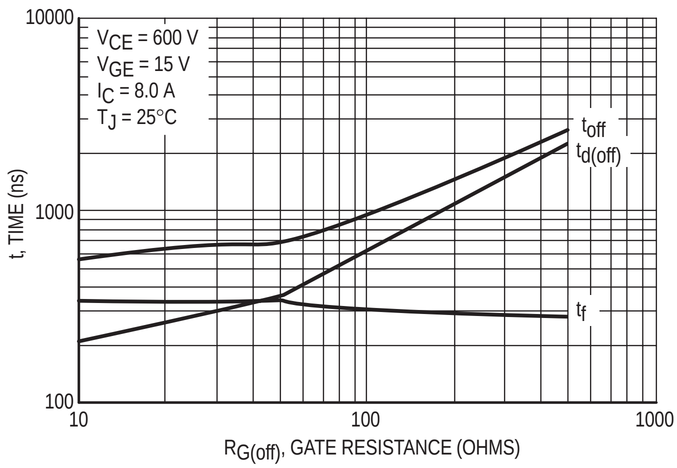


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

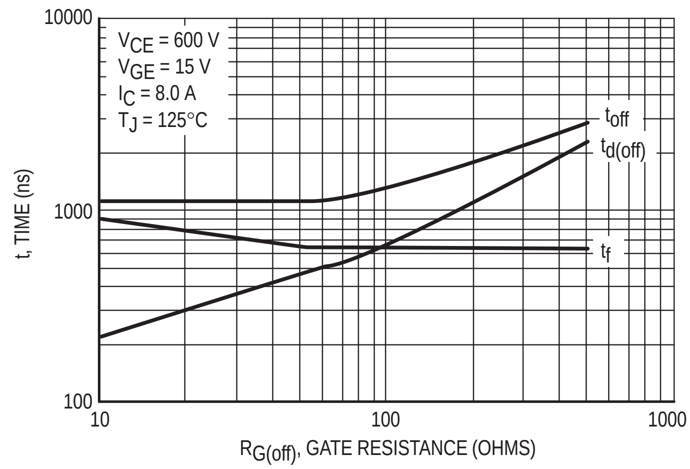


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

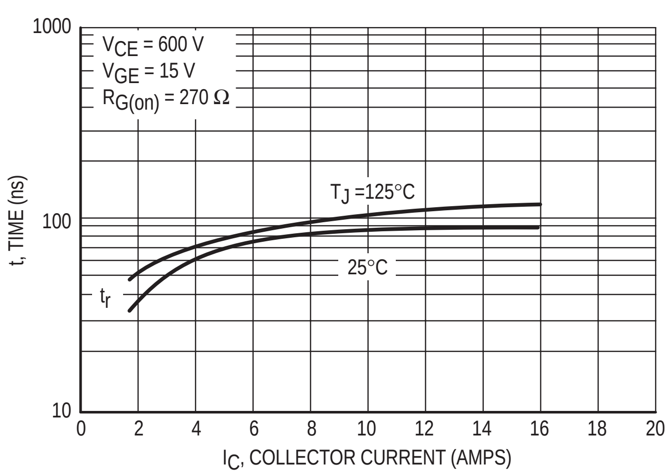


Figure 11. Inductive Switching Times versus Collector Current

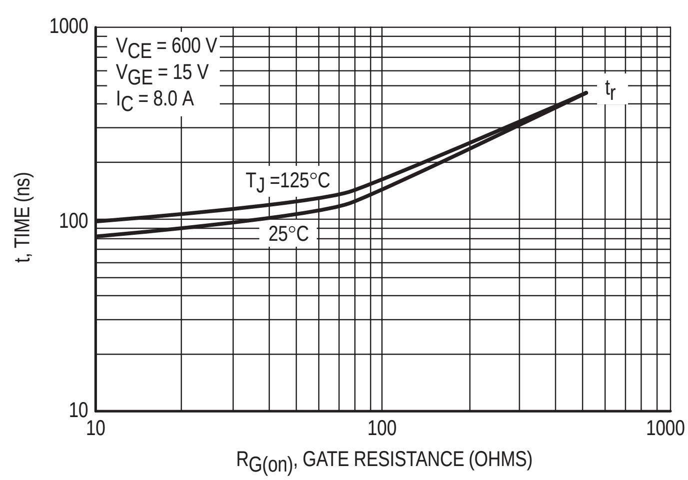


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

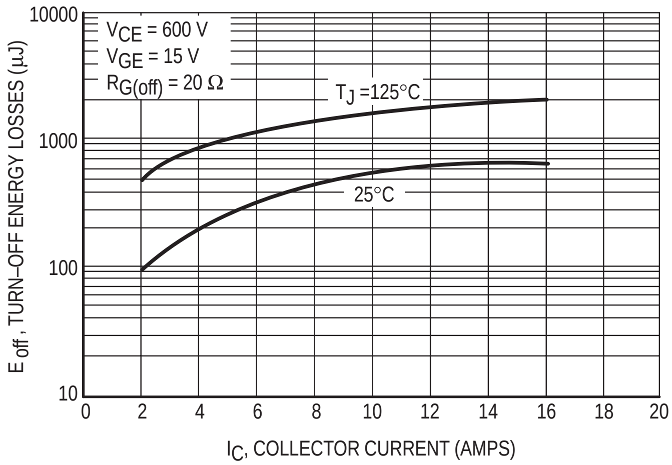


Figure 13. Turn–Off Energy Losses versus Collector Current

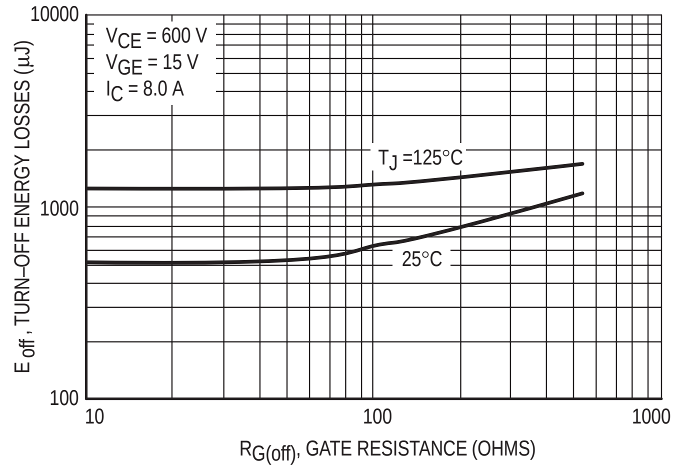


Figure 14. Turn–Off Energy Losses versus Gate Resistance

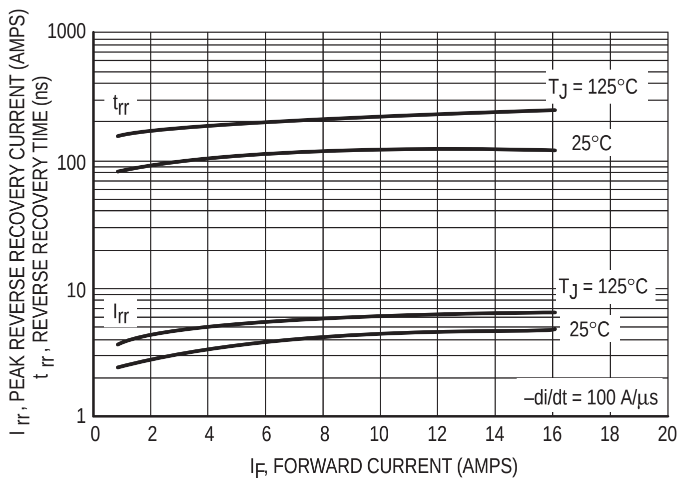


Figure 15. Reverse Recovery Characteristics – Free–Wheeling Diode

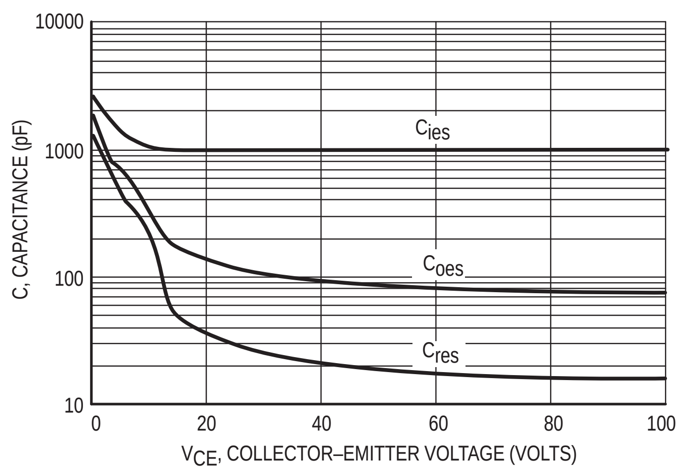


Figure 16. Capacitance Variation

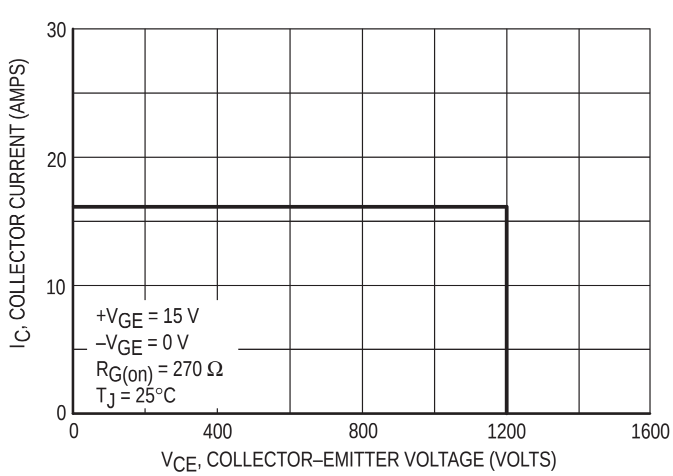


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

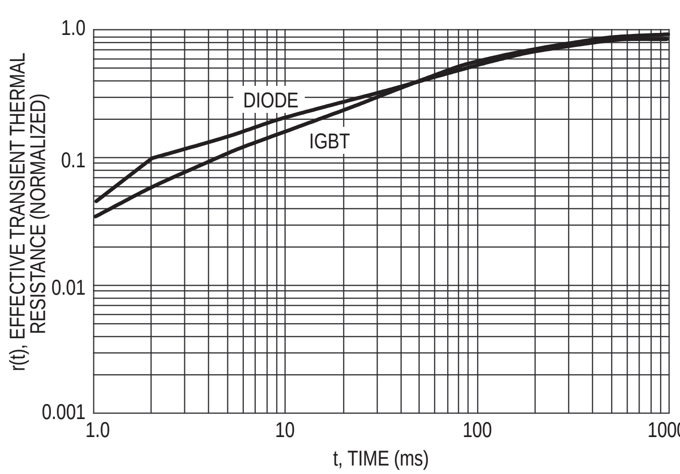


Figure 18. Thermal Response

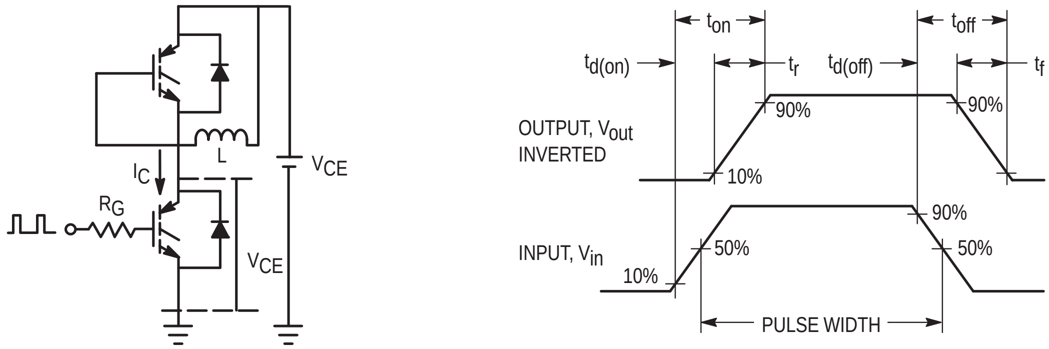


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

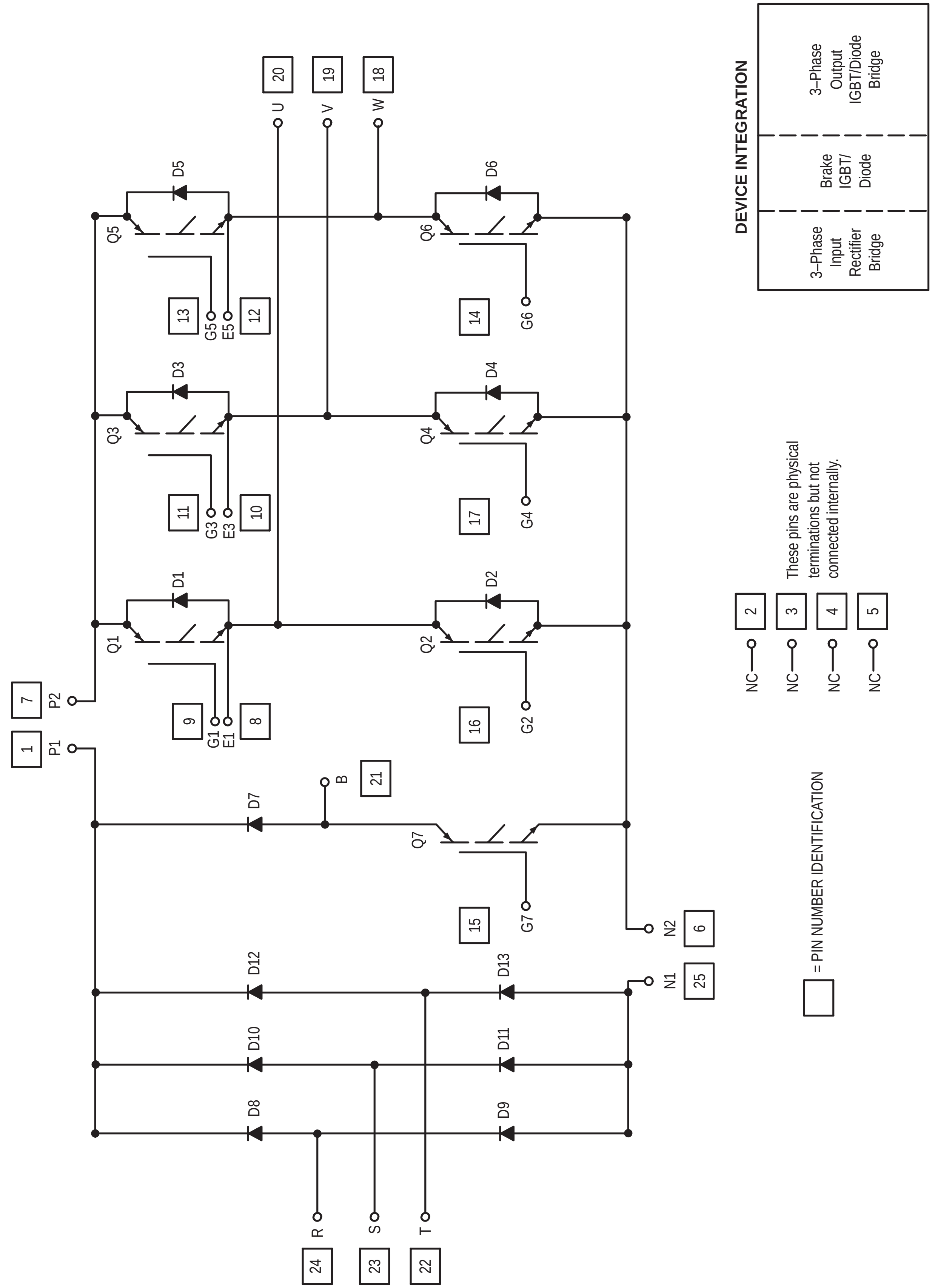


Figure 20. Integrated Power Stage Schematic

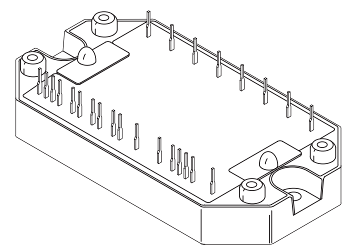
Hybrid Power Module

Integrated Power Stage for 2.0 hp Motor Drives

(This device is not recommended for new designs)
(This device is replaced by MHPM7A10S120DC3)

MHPM7A12A120A

12 AMP, 1200 VOLT
HYBRID POWER MODULE



PLASTIC PACKAGE
CASE 440-02, Style 1

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 600V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	12	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	12	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	24	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	12	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	24	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	60	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	12	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	24	A
IGBT Power Dissipation (T_C = 95°C	PD	60	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	12	A
Peak Output Diode Current	$I_{F(pk)}$	24	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	–	5.0	50	µA
Forward Voltage (I_F = 12 A)	V_F	–	0.97	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (I_C = 12 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	1840	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V)	Q_T	–	66	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	2.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 12 A, V_{GE} = 0 V)	V_F	–	1.6	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 12 A, V = 600 V, di/dt = 100 A/µs)	t_{rr}	–	170	200	ns
Free Wheeling Diode Stored Charge (I_F = 12 A, V = 600 V, di/dt = 100 A/µs)	Q_{rr}	–	575	900	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.7	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 12 A)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	1840	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V)	Q_T	–	66	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	2.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.0	mJ
Output Diode Forward Voltage (I_F = 12 A)	V_F	–	1.6	2.2	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.7	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.7	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	–	10	–	mΩ
Resistance Tolerance	R_{tol}	–1.0	–	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	–	0.660	–	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	–	–1.95	–	mV/°C

Typical Characteristics

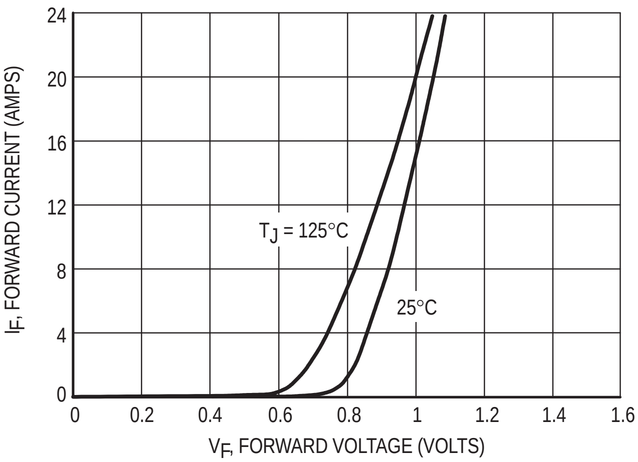


Figure 1. Forward Characteristics – Input Rectifier

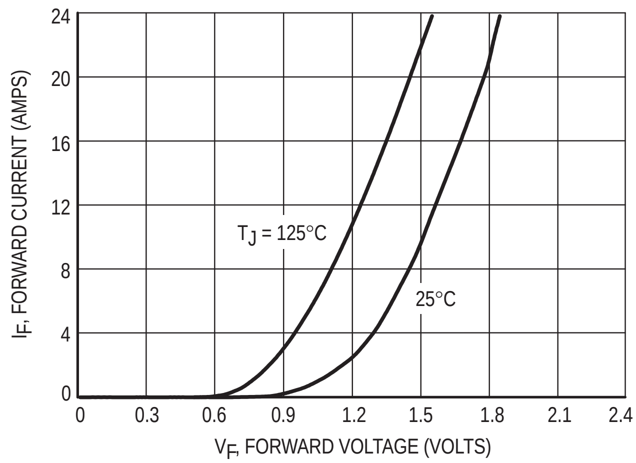


Figure 2. Forward Characteristics – Free–Wheeling Diode

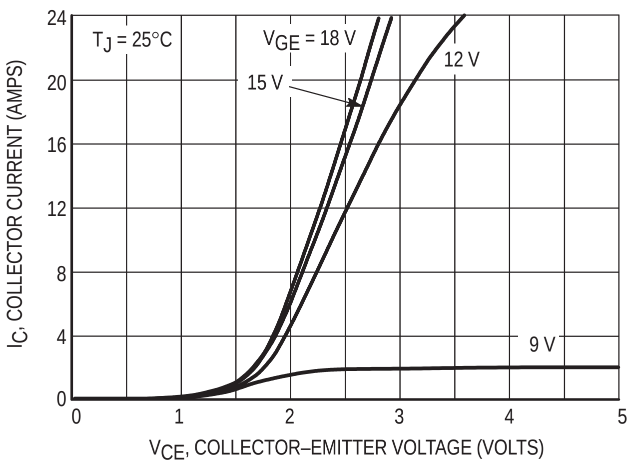


Figure 3. Forward Characteristics, T_J = 25°C

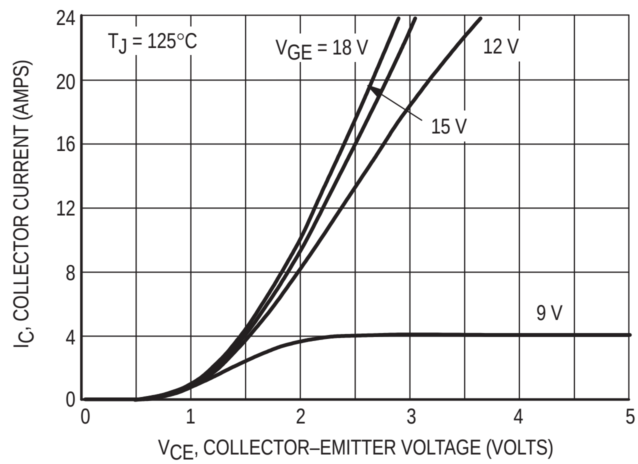


Figure 4. Forward Characteristics, T_J = 125°C

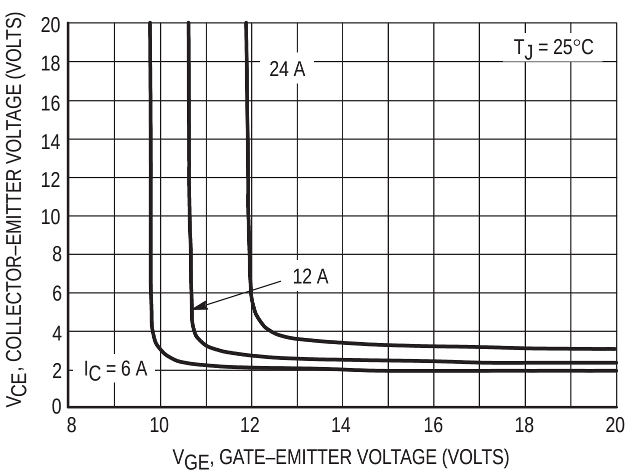


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

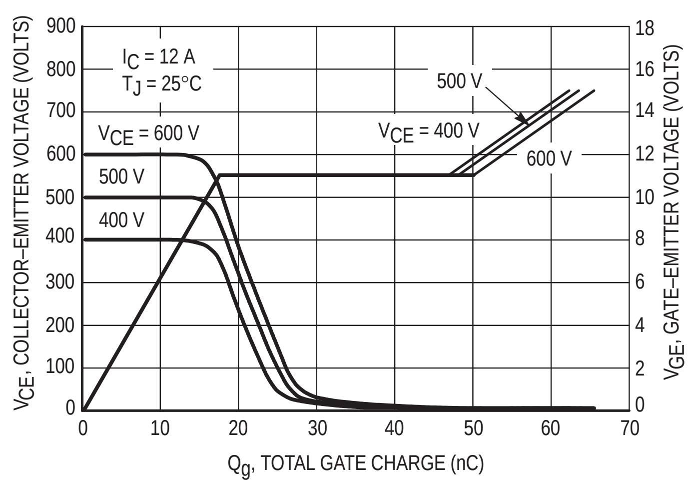


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

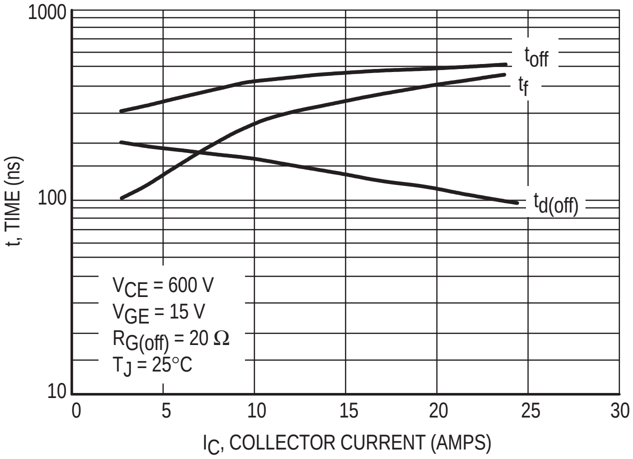


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

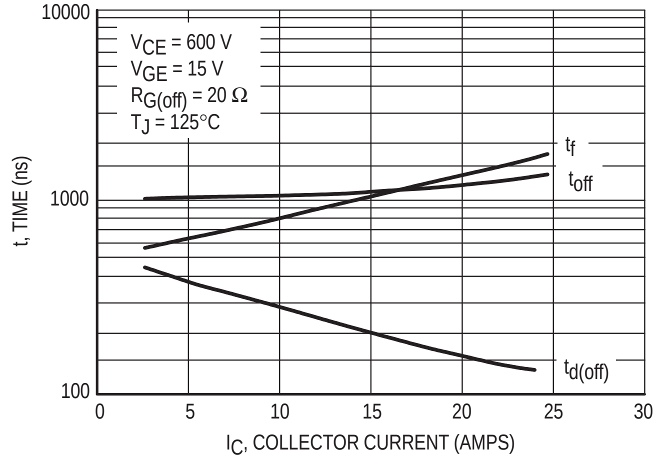


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

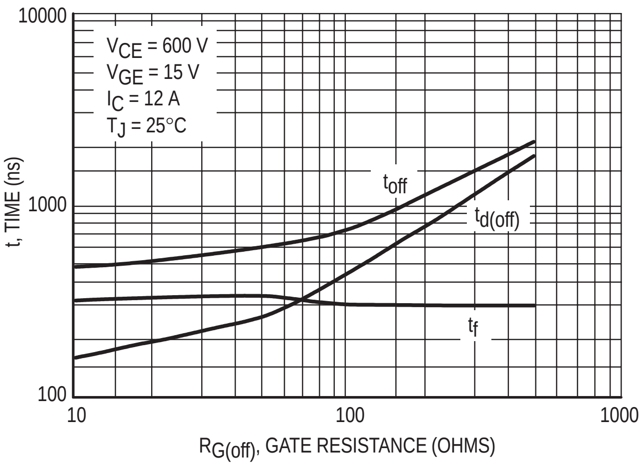


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

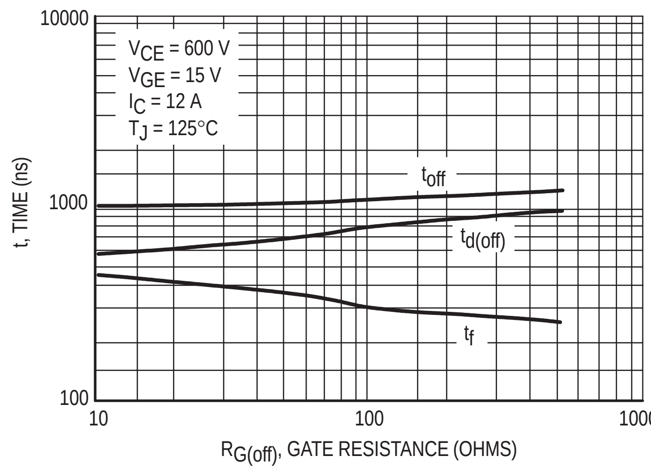


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

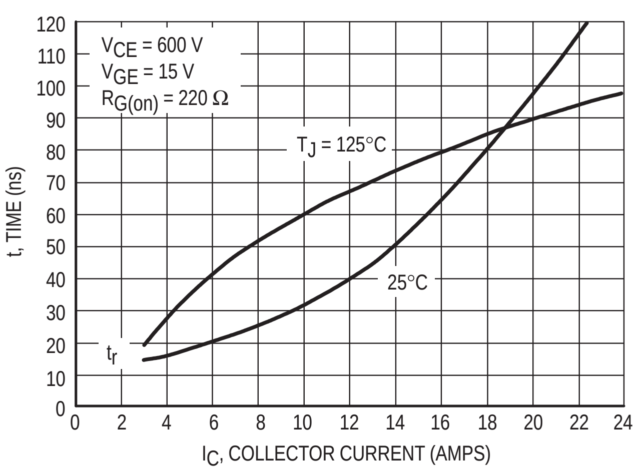


Figure 11. Inductive Switching Times versus Collector Current

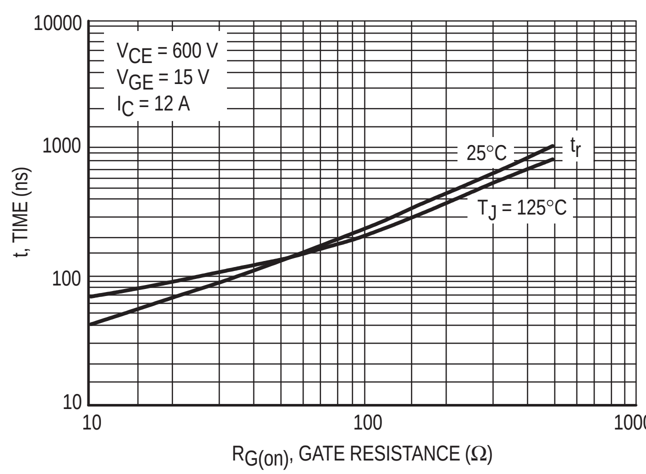


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

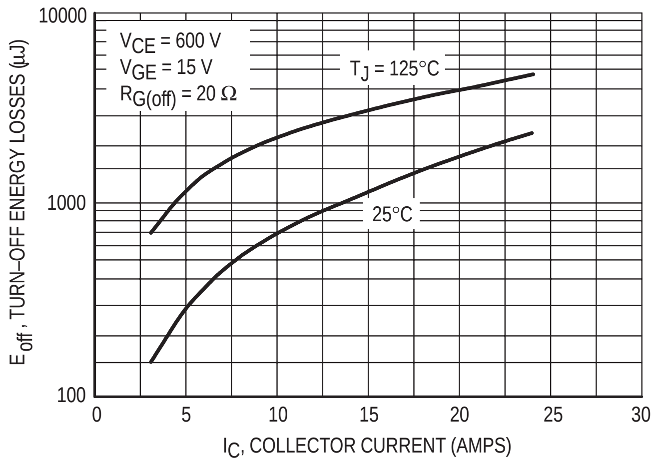


Figure 13. Turn–Off Energy Losses versus Collector Current

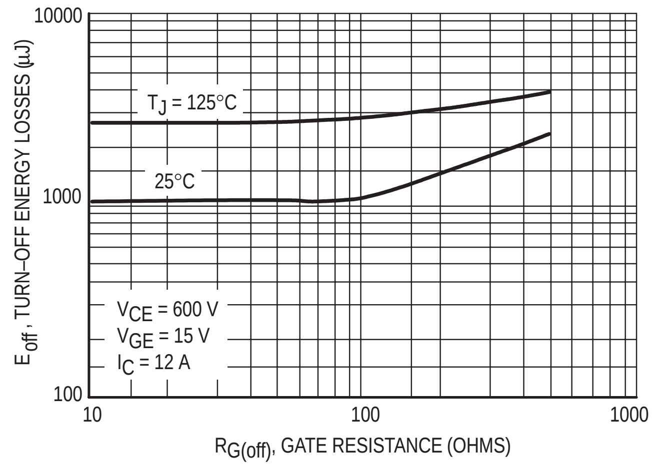


Figure 14. Turn–Off Energy Losses versus Gate Resistance

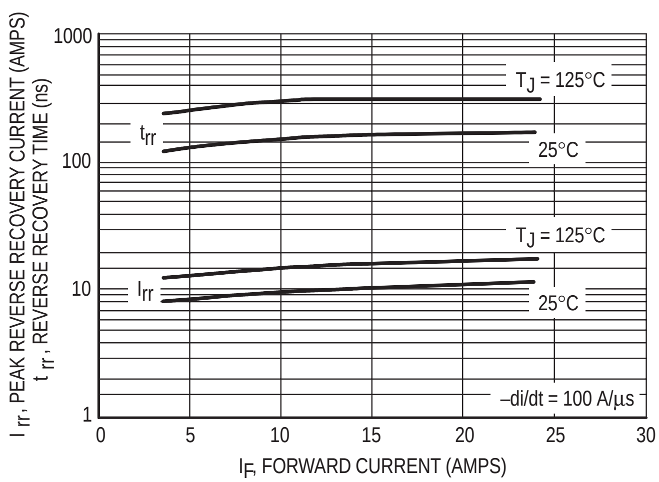


Figure 15. Reverse Recovery Characteristics – Free–Wheeling Diode

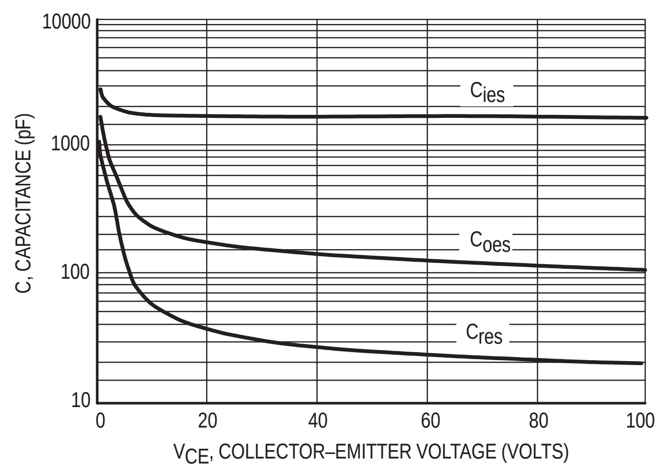


Figure 16. Capacitance Variation

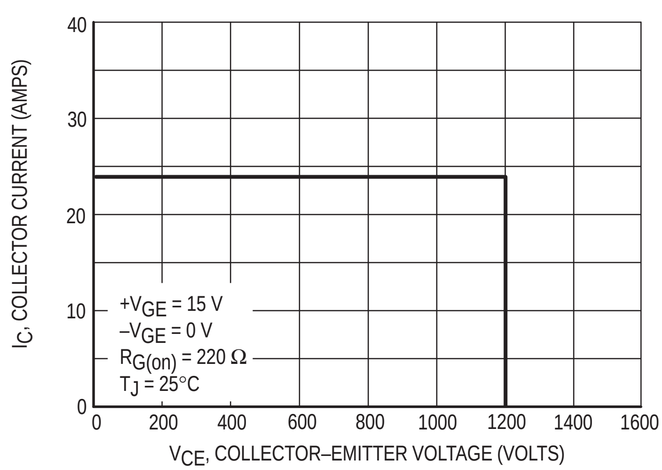


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

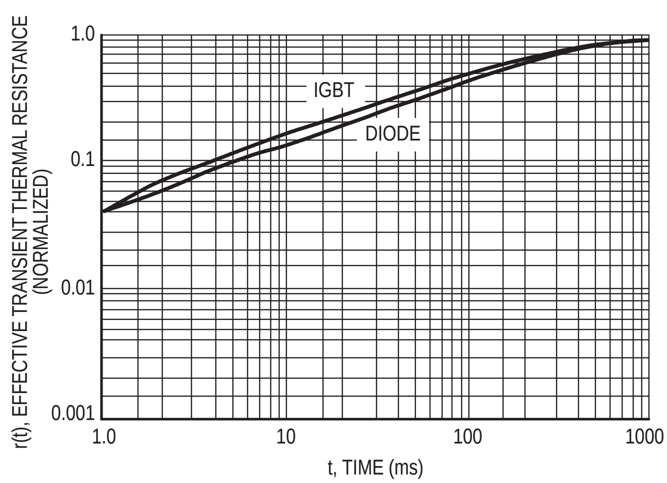


Figure 18. Thermal Response

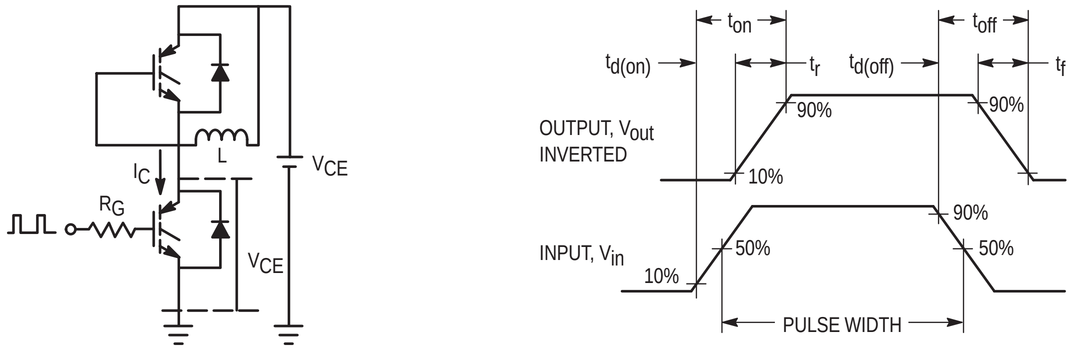


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

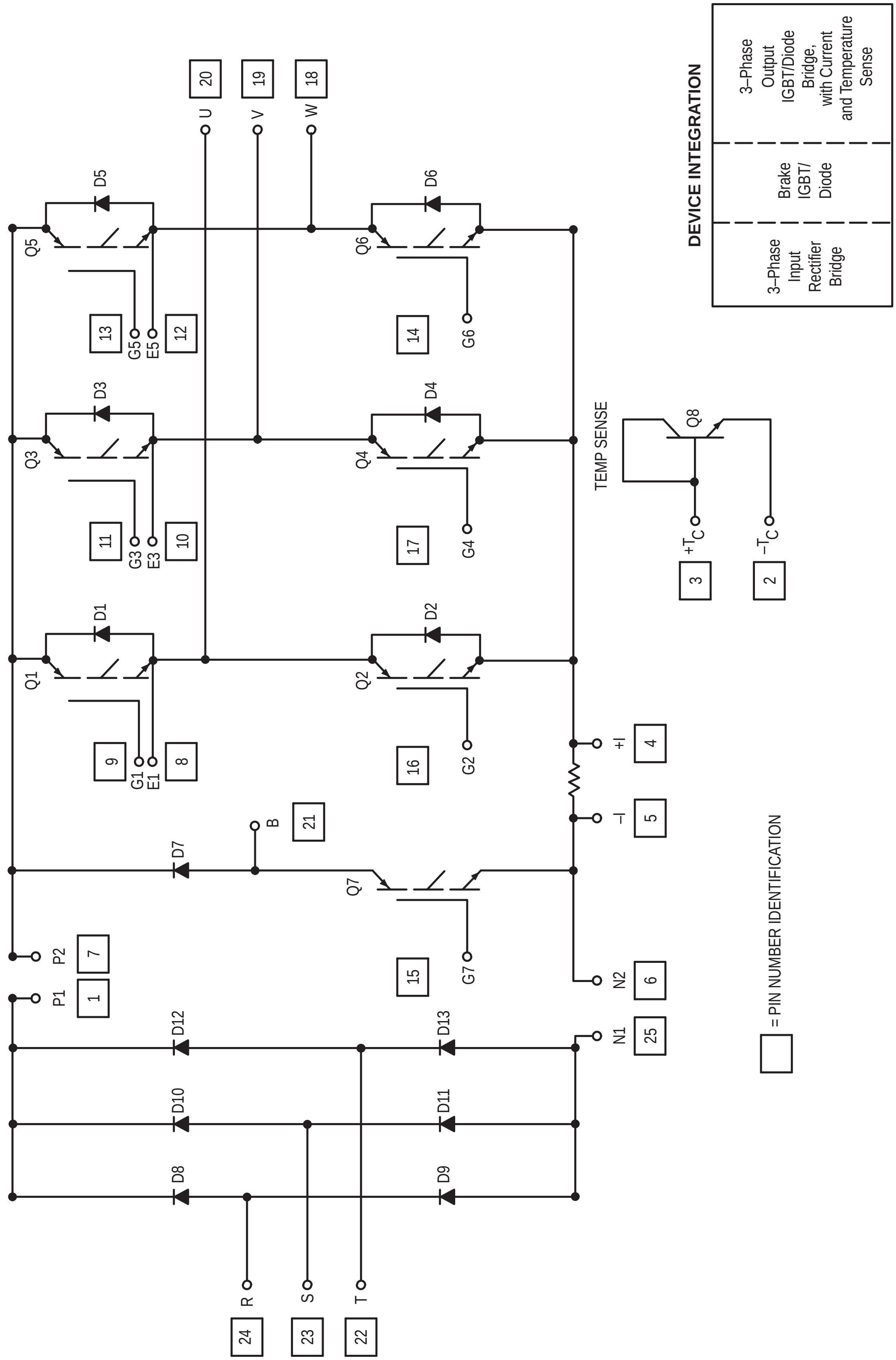


Figure 20. Integrated Power Stage Schematic

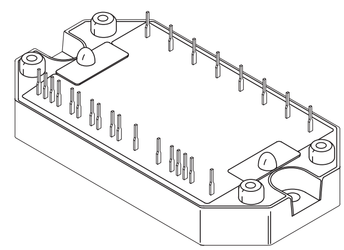
Hybrid Power Module

Integrated Power Stage for 2.0 hp Motor Drives

(This device is not recommended for new designs)
(This device is replaced by MHPM7A10S120DC3)

MHPM7B12A120A

12 AMP, 1200 VOLT
HYBRID POWER MODULE



PLASTIC PACKAGE
CASE 440-02, Style 1

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 600V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	12	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	12	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	24	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	12	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	24	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	60	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	12	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	24	A
IGBT Power Dissipation (T_C = 95°C)	PD	60	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	12	A
Peak Output Diode Current	$I_{F(pk)}$	24	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	–	5.0	50	μA
Forward Voltage (I_F = 12 A)	V_F	–	2.1	2.65	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.9	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	μA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	μA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (I_C = 12 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	1840	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V)	Q_T	–	66	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	2.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 12 A, V_{GE} = 0 V)	V_F	–	1.6	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 12 A, V = 600 V, di/dt = 100 A/μs)	t_{rr}	–	170	200	ns
Free Wheeling Diode Stored Charge (I_F = 12 A, V = 600 V, di/dt = 100 A/μs)	Q_{rr}	–	575	900	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.7	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	– –	6.0 2000	100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 12 A)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	1840	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V)	Q_T	–	66	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	300	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	2.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 12 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	2.0	mJ
Output Diode Forward Voltage (I_F = 12 A)	V_F	–	1.6	2.2	V
Output Diode Reverse Leakage Current	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.7	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.7	°C/W

Typical Characteristics

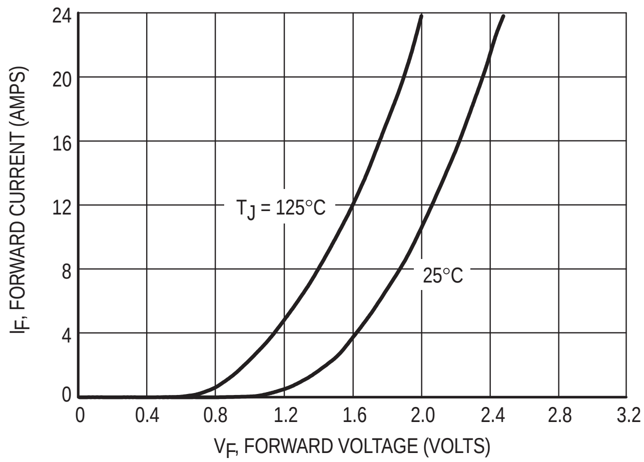


Figure 1. Forward Characteristics – Input Rectifier

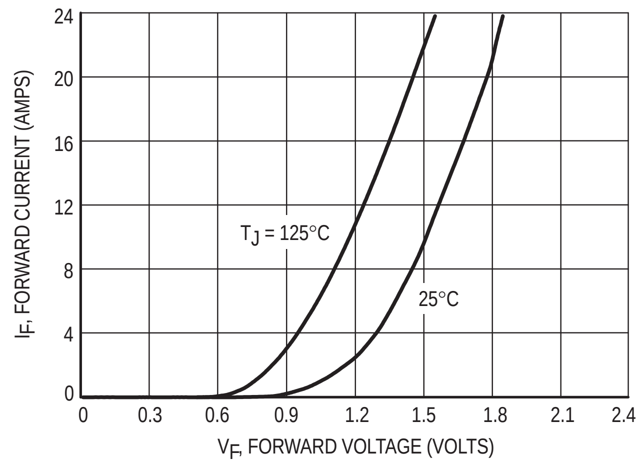


Figure 2. Forward Characteristics – Free–Wheeling Diode

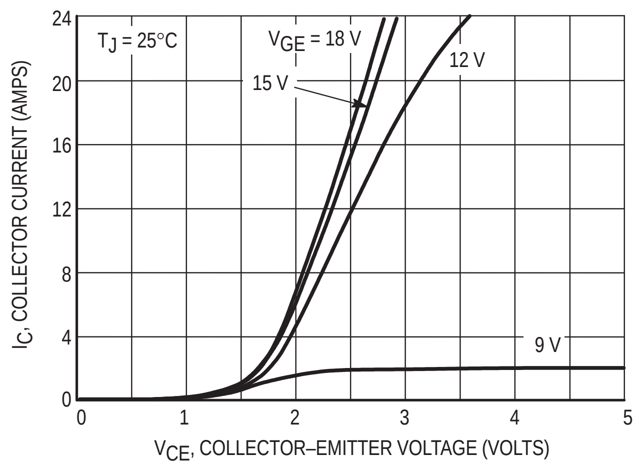


Figure 3. Forward Characteristics, T_J = 25°C

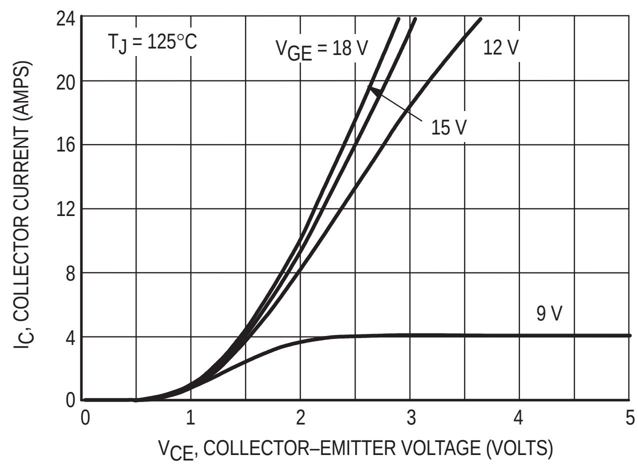


Figure 4. Forward Characteristics, T_J = 125°C

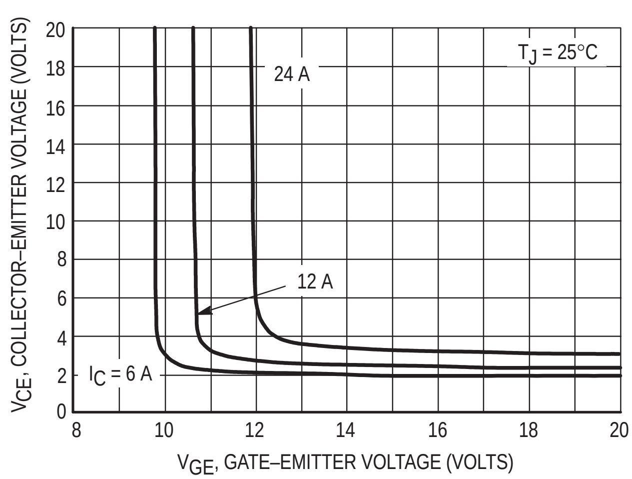


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

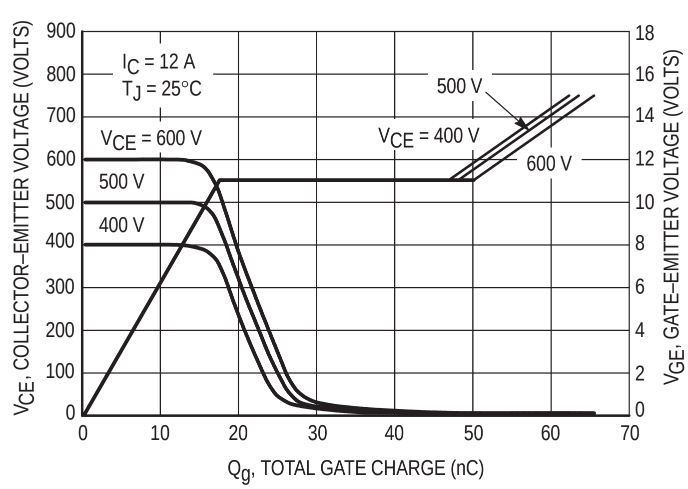


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

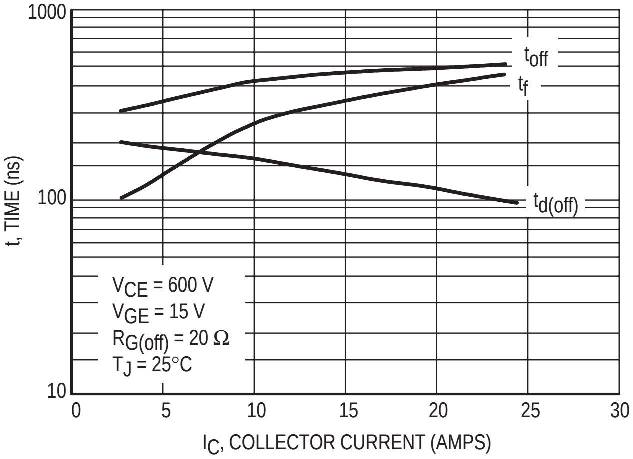


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

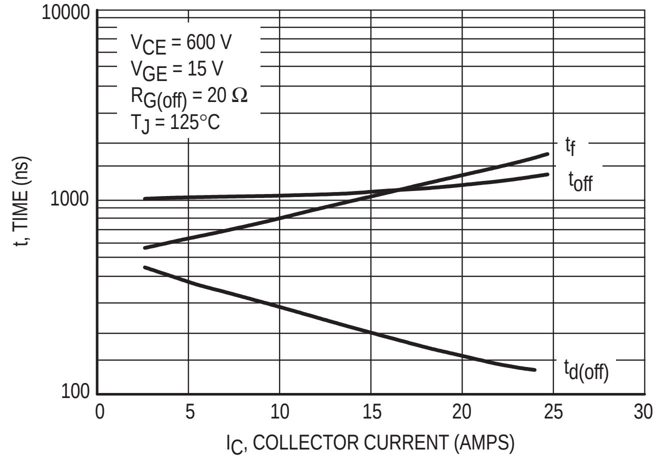


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

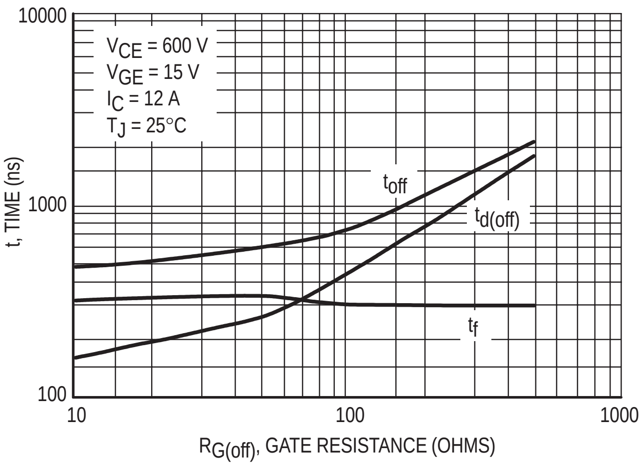


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

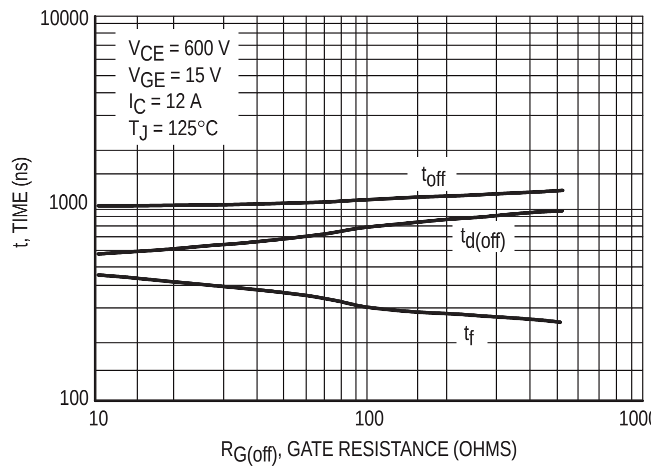


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

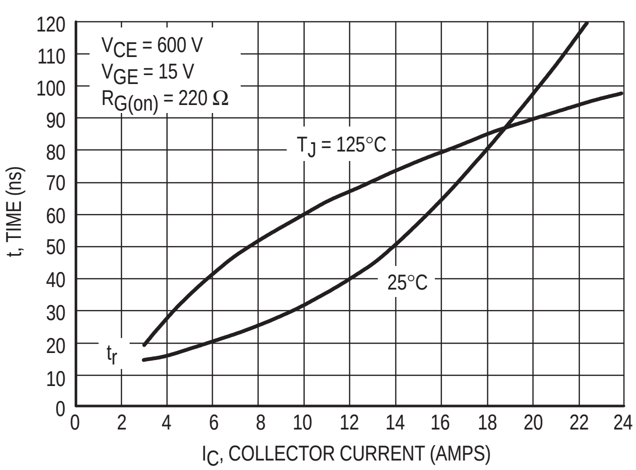


Figure 11. Inductive Switching Times versus Collector Current

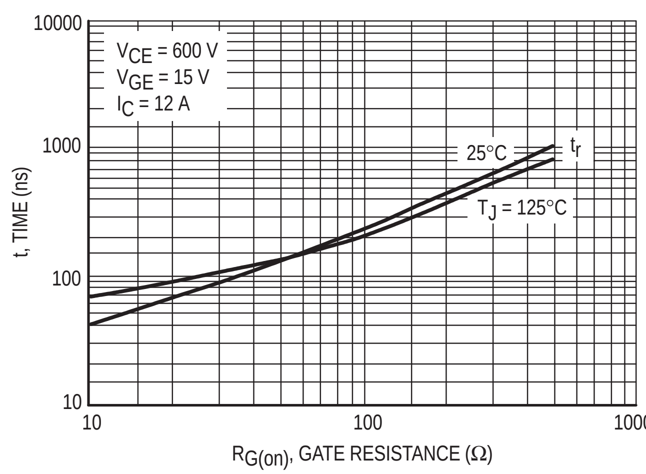


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

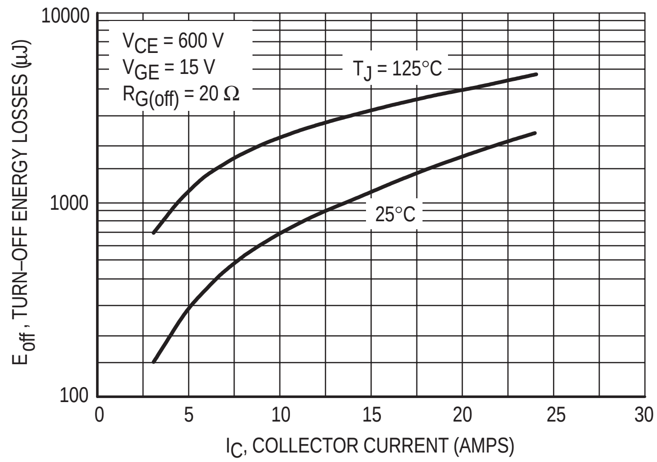


Figure 13. Turn–Off Energy Losses versus Collector Current

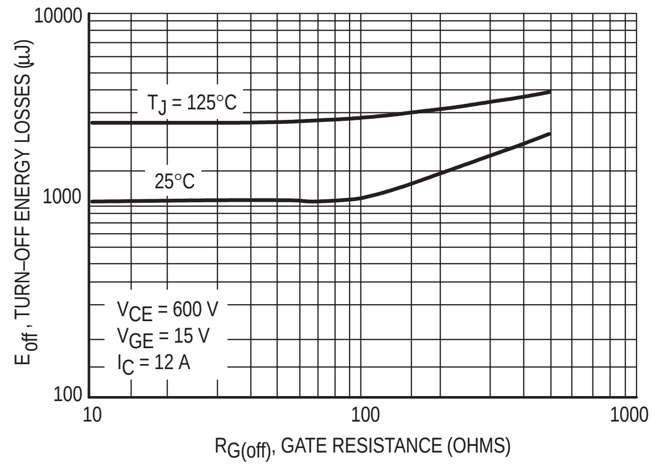


Figure 14. Turn–Off Energy Losses versus Gate Resistance

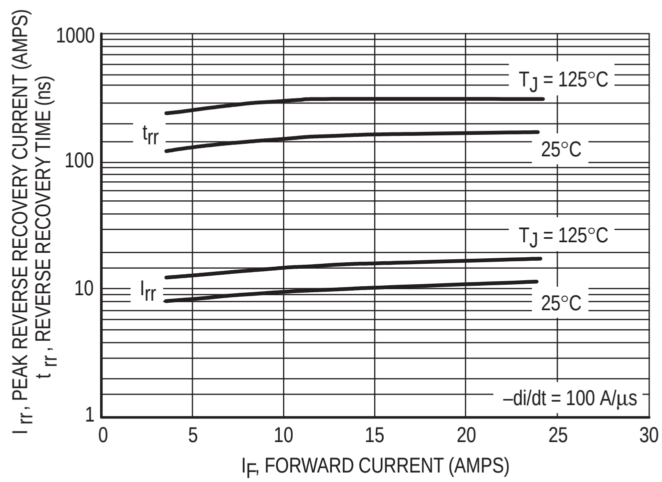


Figure 15. Reverse Recovery Characteristics – Free–Wheeling Diode

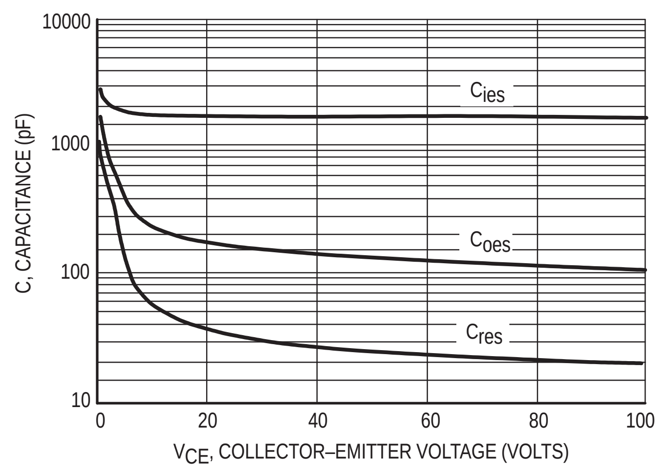


Figure 16. Capacitance Variation

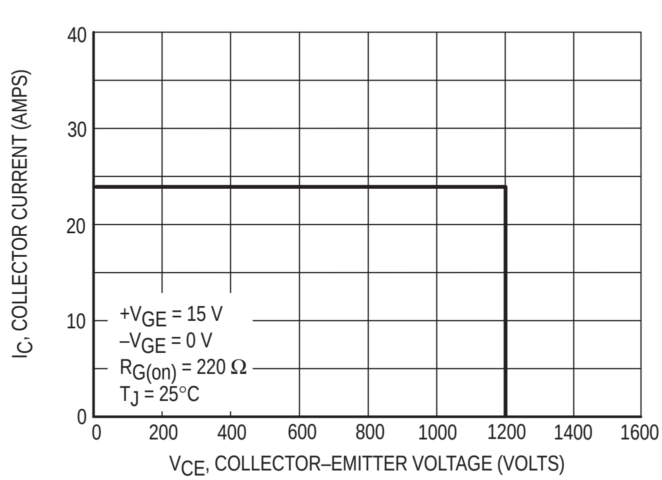


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

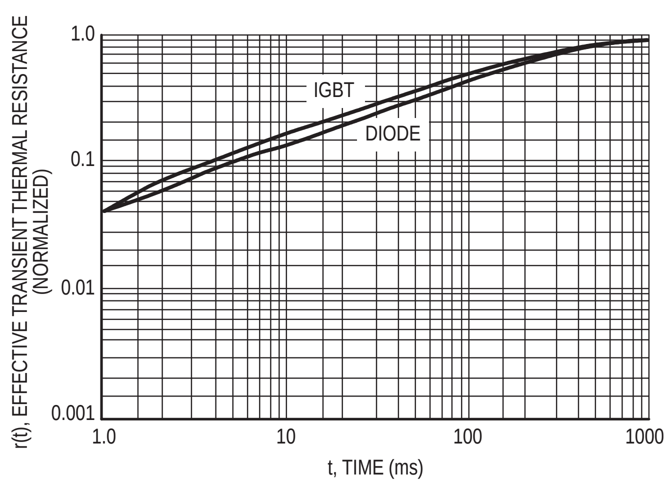


Figure 18. Thermal Response

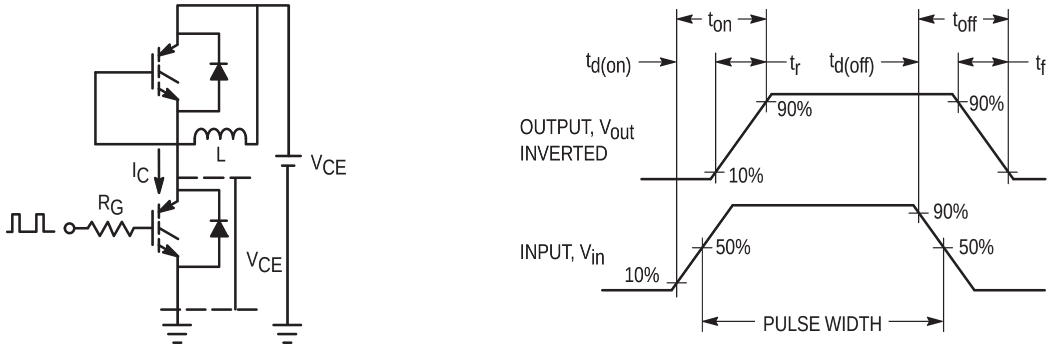


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

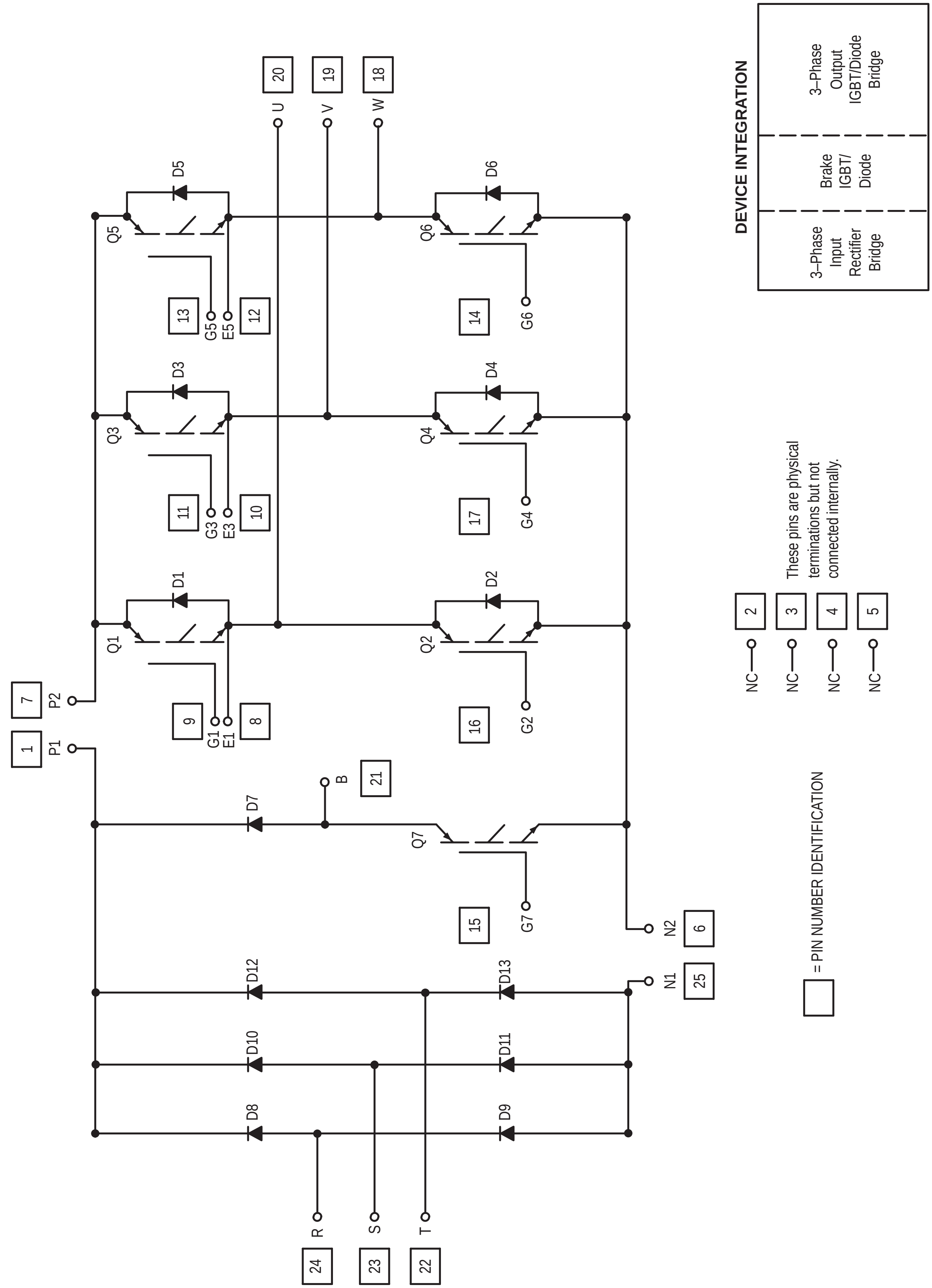


Figure 20. Integrated Power Stage Schematic

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

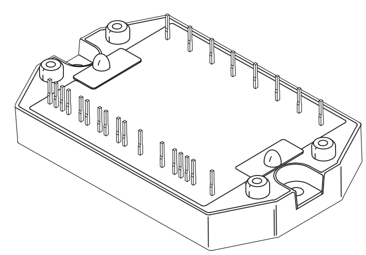
Hybrid Power Module

Integrated Power Stage for 3.0 hp Motor Drives

(This device is not recommended for new designs)
(This device is replaced by MHPM7A15S120DC3)

MHPM7A16A120B

16 AMP, 1200 VOLT
HYBRID POWER MODULE



PLASTIC PACKAGE
CASE 440A–02, Style 1

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 600V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	16	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	330	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	16	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	32	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	16	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	32	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	75	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	16	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	32	A
IGBT Power Dissipation (T_C = 95°C)	PD	75	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	16	A
Peak Output Diode Current	$I_{F(pk)}$	32	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	–	5.0	50	µA
Forward Voltage (I_F = 16 A)	V_F	–	1.02	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (I_C = 16 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	2800	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V)	Q_T	–	102	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	350	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 16 A, V_{GE} = 0 V)	V_F	–	1.7	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 16 A, V = 400 V, di/dt = 100 A/µs)	t_{rr}	–	165	200	ns
Free Wheeling Diode Stored Charge (I_F = 16 A, V = 400 V, di/dt = 100 A/µs)	Q_{rr}	–	860	900	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.4	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C	I_{CES}	–	6.0	100	µA
T_J = 125°C		–	2000		
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 16 A)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	2800	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V)	Q_T	–	102	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	350	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Output Diode Forward Voltage (I_F = 16 A)	V_F	–	1.7	2.2	V
Output Diode Reverse Leakage Current (V_R = 1200 V)	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.4	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.7	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	–	5.0	–	mΩ
Resistance Tolerance	R_{tol}	–1.0	–	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	–	0.660	–	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	–	–1.95	–	mV/°C

Typical Characteristics

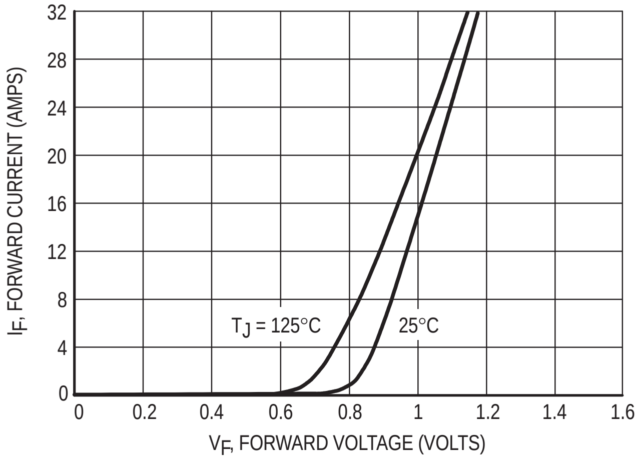


Figure 1. Forward Characteristics – Input Rectifier

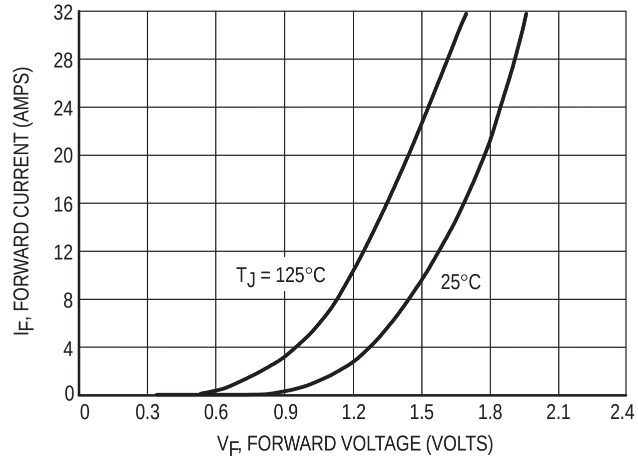


Figure 2. Forward Characteristics – Free–Wheeling Diode

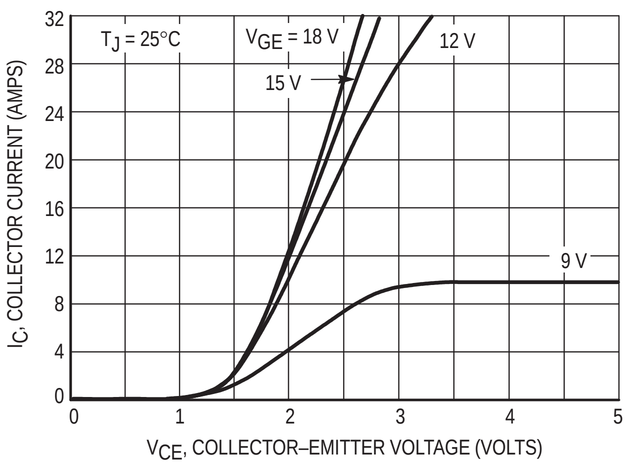


Figure 3. Forward Characteristics, T_J = 25°C

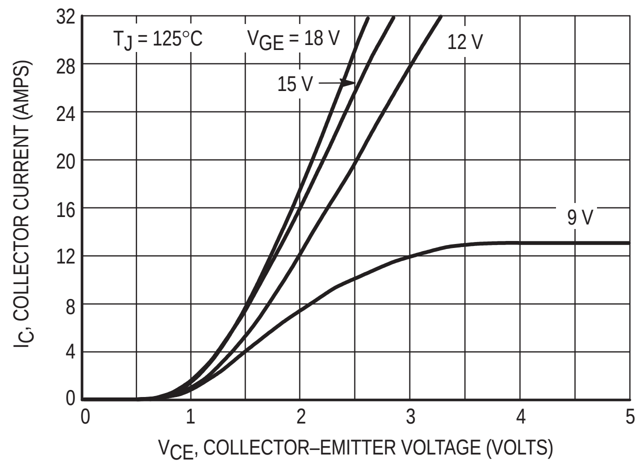


Figure 4. Forward Characteristics, T_J = 125°C

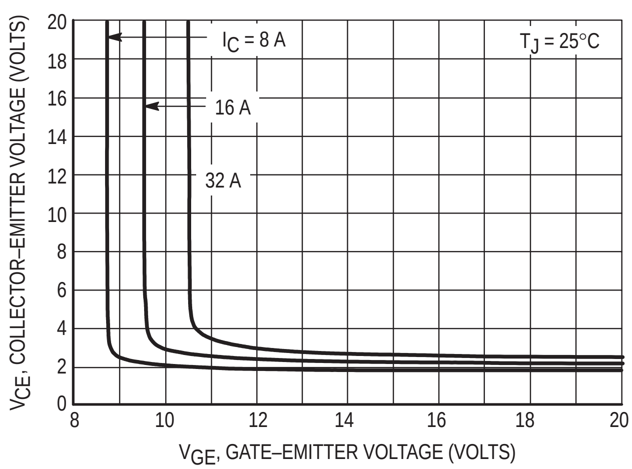


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

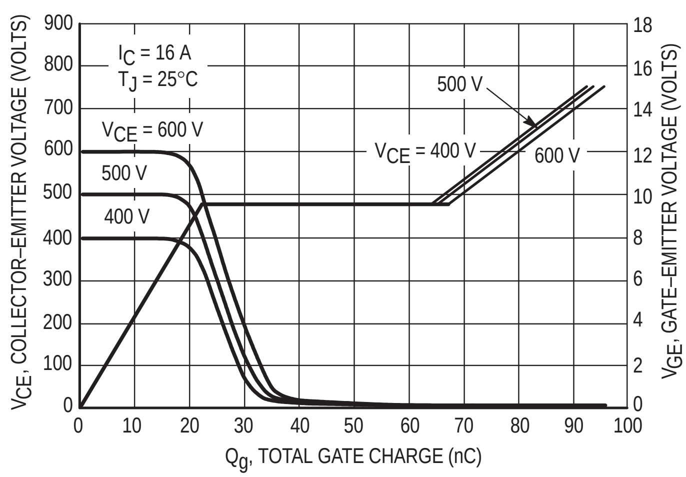


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

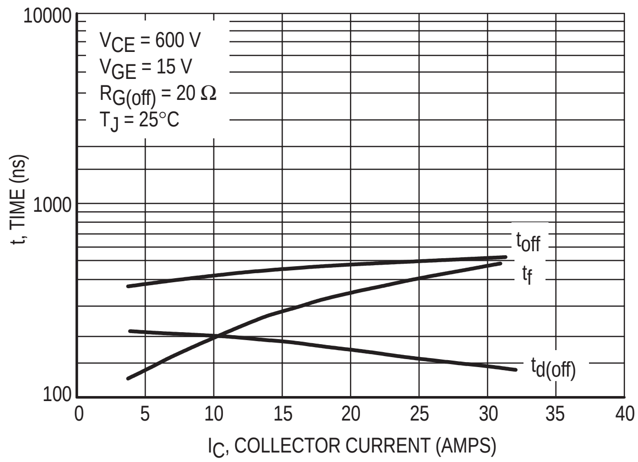


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

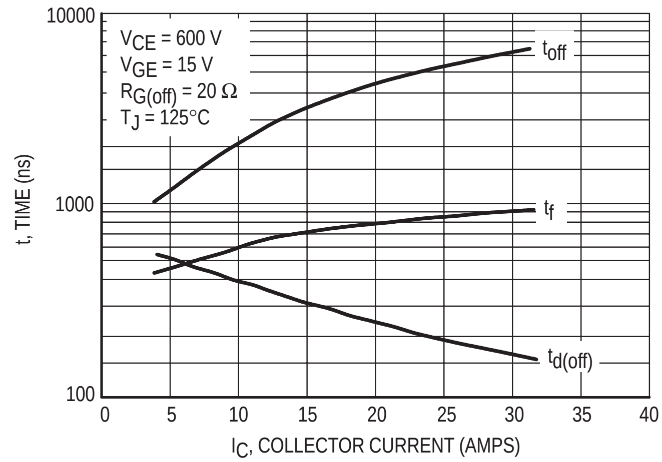


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

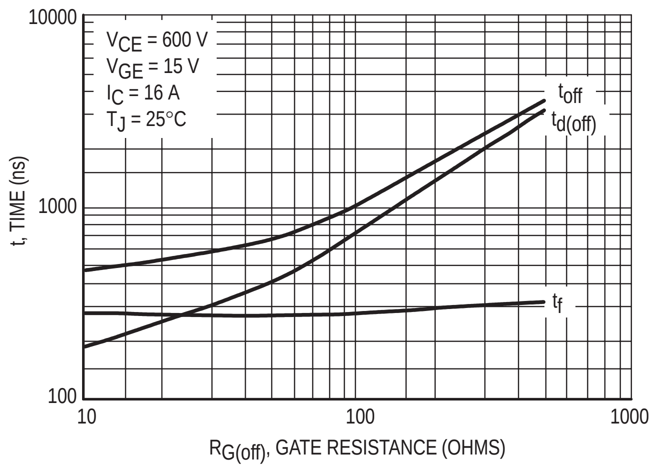


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

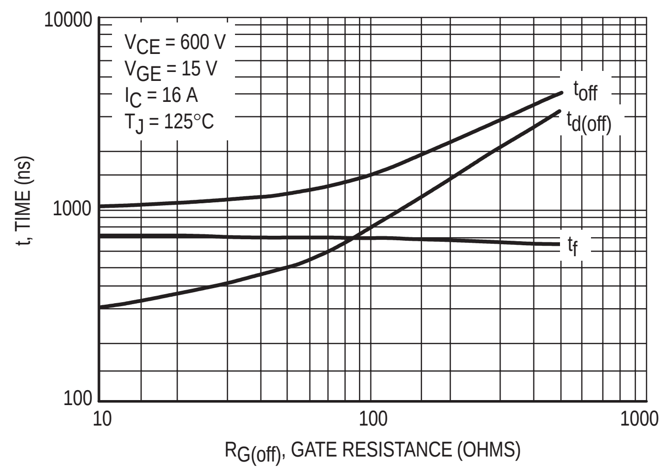


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

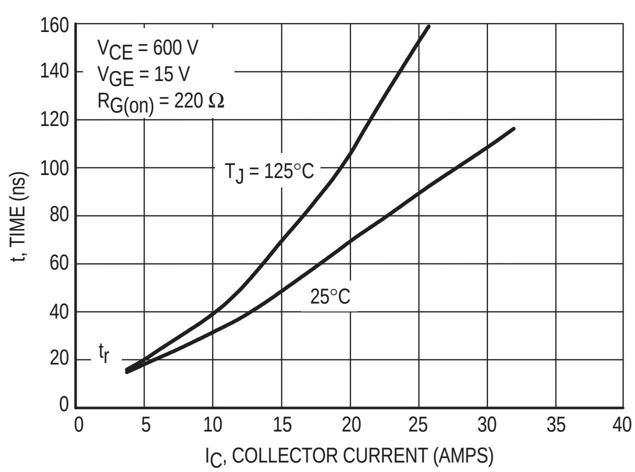


Figure 11. Inductive Switching Times versus Collector Current

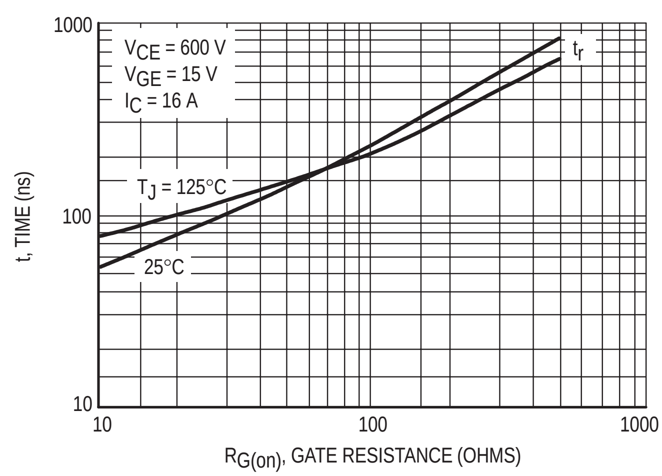


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

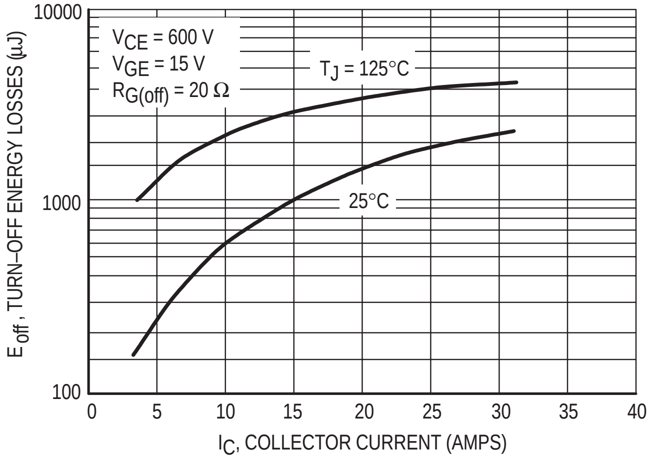


Figure 13. Turn–Off Energy Losses versus Collector Current

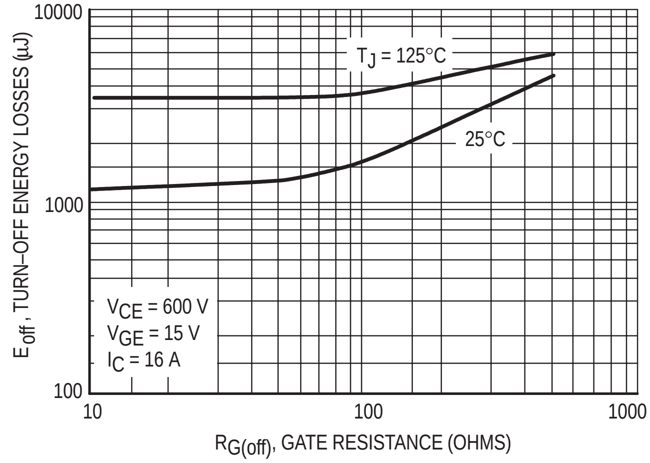


Figure 14. Turn–Off Energy Losses versus Gate Resistance

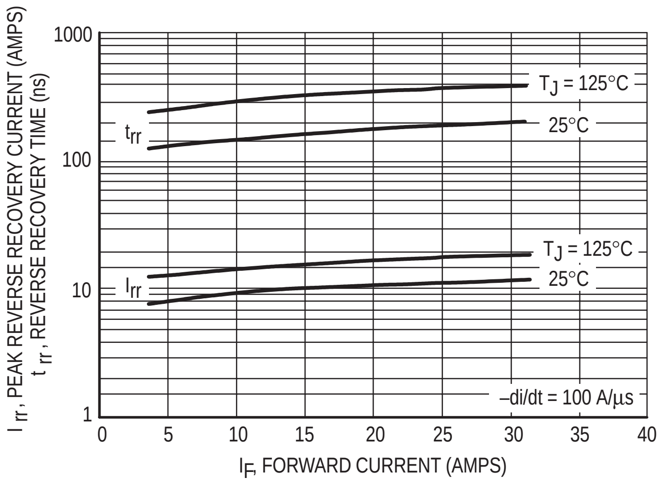


Figure 15. Reverse Recovery Characteristics – Free–Wheeling Diode

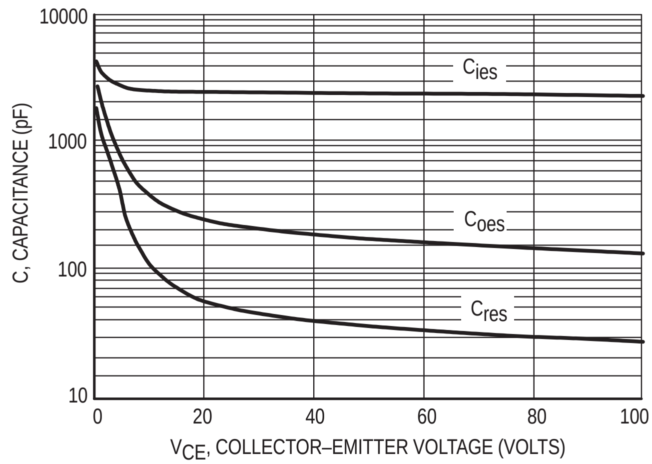


Figure 16. Capacitance Variation

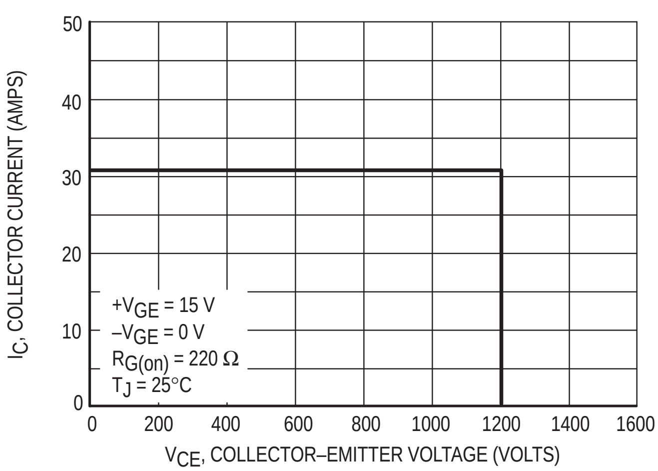


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

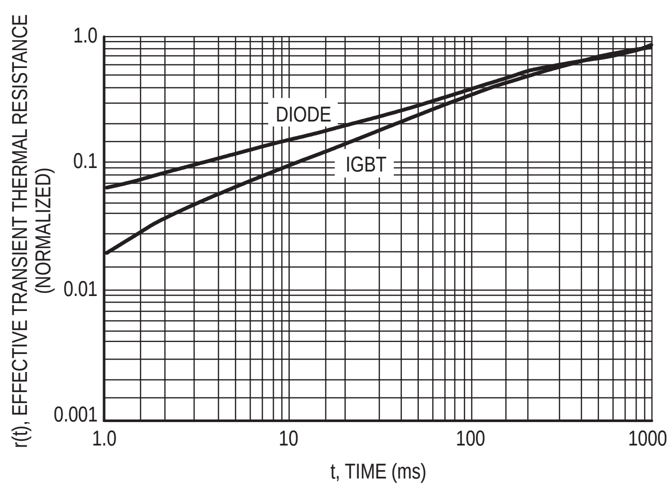


Figure 18. Thermal Response

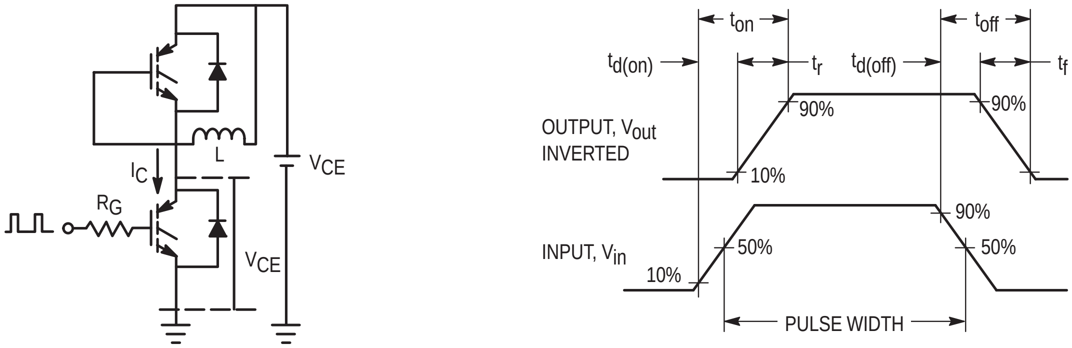


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

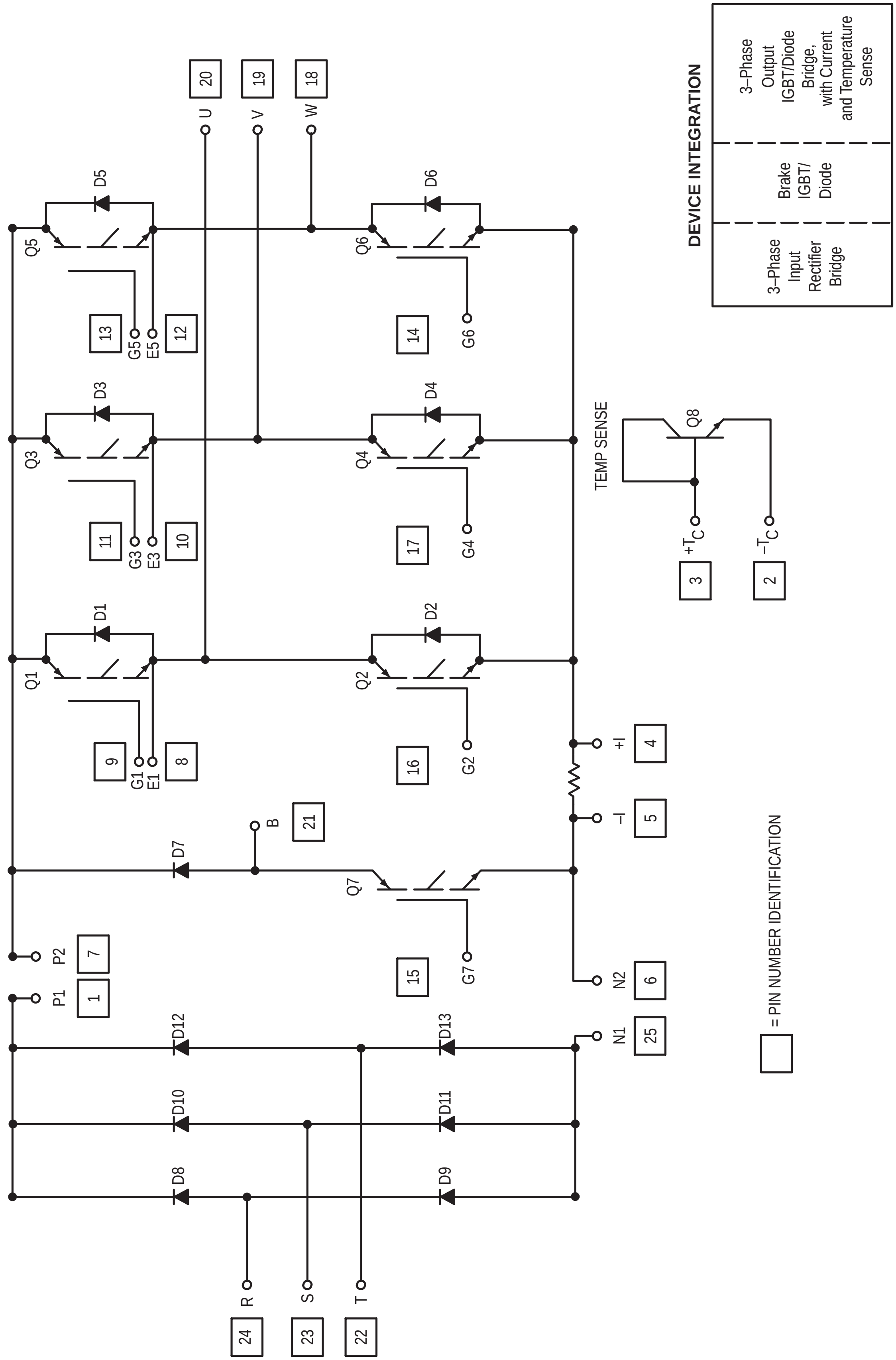


Figure 20. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 3.0 hp Motor Drives

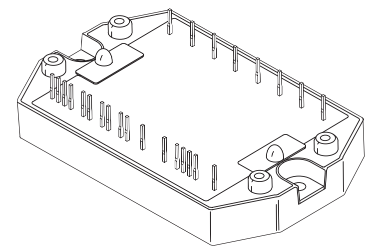
(This device is not recommended for new designs)
(This device is replaced by MHPM7A15S120DC3)

MHPM7B16A120B

16 AMP, 1200 VOLT
HYBRID POWER MODULE

This module integrates a 3–phase input rectifier bridge, 3–phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free–wheeling diodes to give optimal dynamic performance. It has been configured for use as a three–phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 600V
- Pin-to-Baseplate Isolation Exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440A–02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	16	A
Peak Non-repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	330	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	16	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	32	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	16	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	32	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	75	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
IGBT Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1 ms = 1.0% duty cycle

REV 2

MAXIMUM DEVICE RATINGS (continued) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	16	A
Peak Repetitive IGBT Collector Current[(2)]	$I_{C(pk)}$	32	A
IGBT Power Dissipation (T_C = 95°C	PD	75	W
Peak Repetitive Output Diode Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	16	A
Peak Output Diode Current	$I_{F(pk)}$	32	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1.0 Minute Duration)	V_{ISO}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to + 90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	–	6.0	lb–in

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	–	5.0	100	µA
Forward Voltage (I_F = 16 A)	V_F	–	2.24	2.65	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (I_C = 16 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	2800	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V)	Q_T	–	102	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	350	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Free Wheeling Diode Forward Voltage (I_F = 16 A, V_{GE} = 0 V)	V_F	–	1.7	2.2	V
Free Wheeling Diode Reverse Recovery Time (I_F = 16 A, V = 600 V, di/dt = 100 A/µs)	t_{rr}	–	165	200	ns
Free Wheeling Diode Stored Charge (I_F = 16 A, V = 600 V, di/dt = 100 A/µs)	Q_{rr}	–	860	900	nC
Thermal Resistance – IGBT (Each Die)	$R_{\theta JC}$	–	–	1.4	°C/W
Thermal Resistance – Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	–	–	2.7	°C/W

(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	–	–	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 – –	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	–	–	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 16 A)	$V_{CE(SAT)}$	–	2.4	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	–	2800	–	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V)	Q_T	–	102	–	nC
Fall Time – Inductive Load (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	t_f	–	350	500	ns
Turn-On Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(on)}$ = 220 Ω)	E_{on}	–	–	3.0	mJ
Turn-Off Energy (V_{CE} = 600 V, I_C = 16 A, V_{GE} = 15 V, $R_{G(off)}$ = 20 Ω)	E_{off}	–	–	3.0	mJ
Output Diode Forward Voltage (I_F = 16 A)	V_F	–	1.7	2.2	V
Output Diode Reverse Leakage Current (V_R = 1200 V)	I_R	–	–	50	µA
Thermal Resistance – IGBT	$R_{\theta JC}$	–	–	1.4	°C/W
Thermal Resistance – Output Diode	$R_{\theta JC}$	–	–	2.7	°C/W

Typical Characteristics

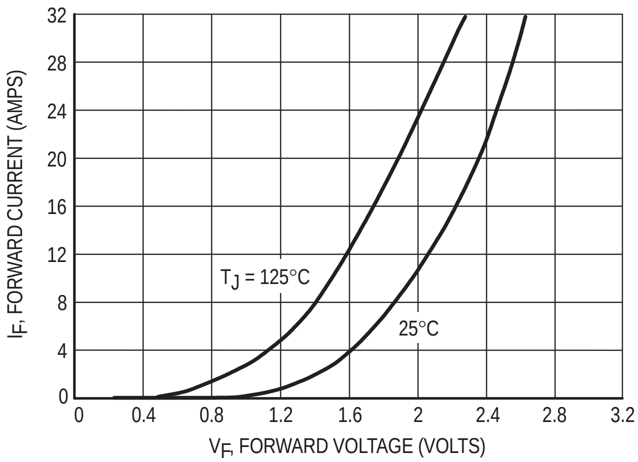


Figure 1. Forward Characteristics – Input Rectifier

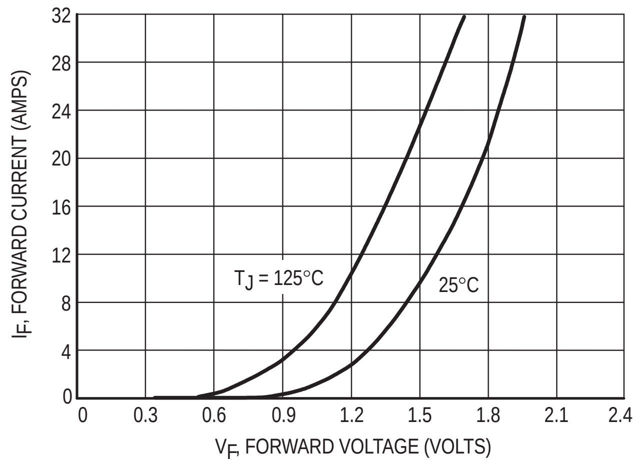


Figure 2. Forward Characteristics – Free–Wheeling Diode

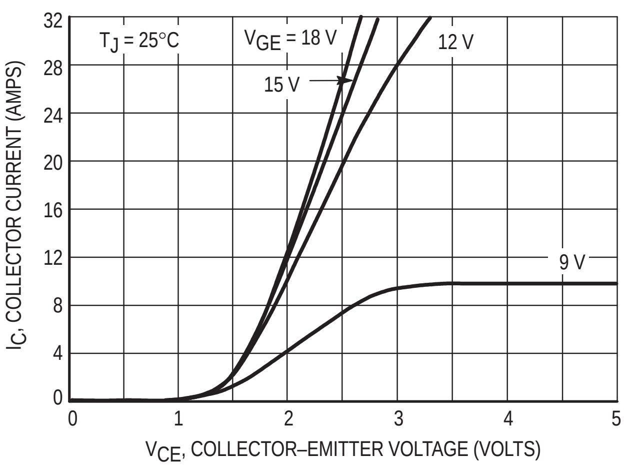


Figure 3. Forward Characteristics, T_J = 25°C

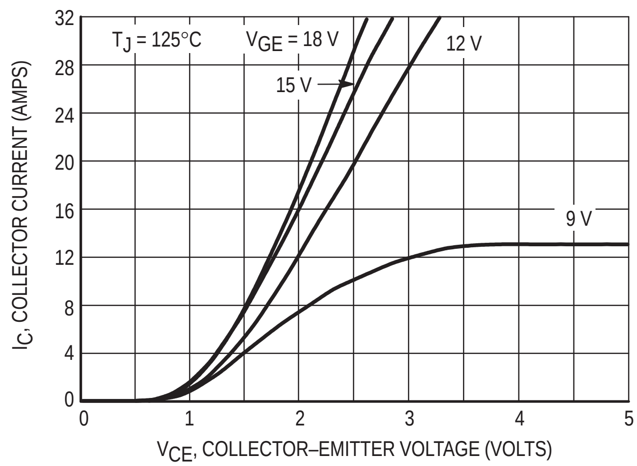


Figure 4. Forward Characteristics, T_J = 125°C

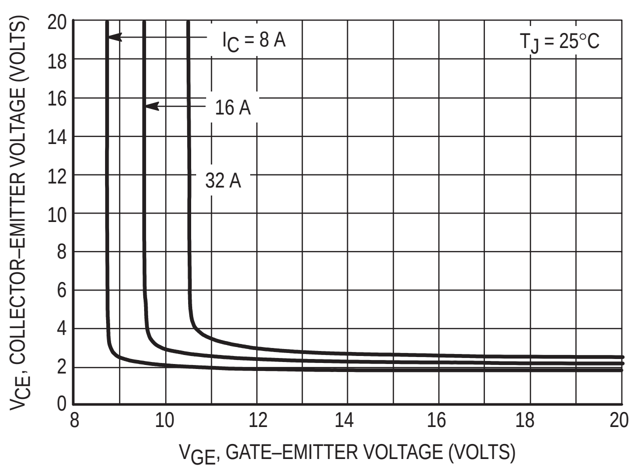


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

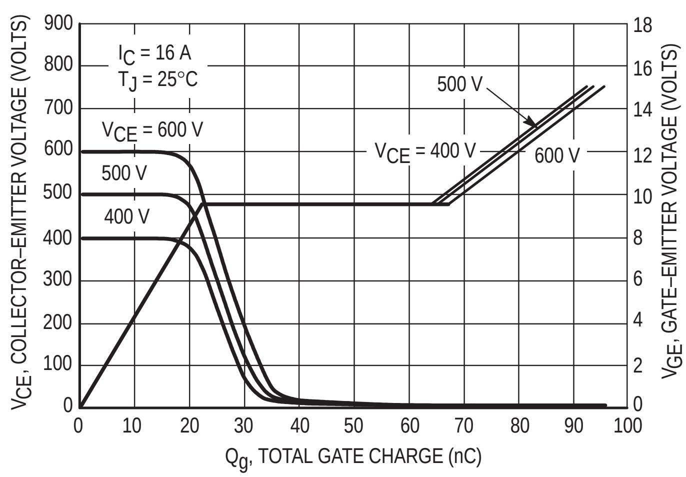


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

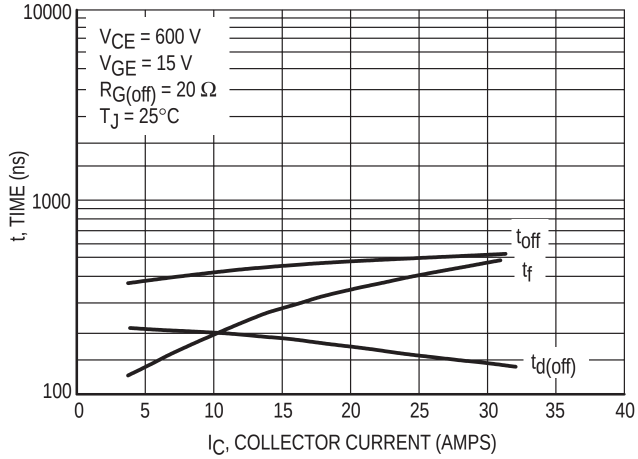


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

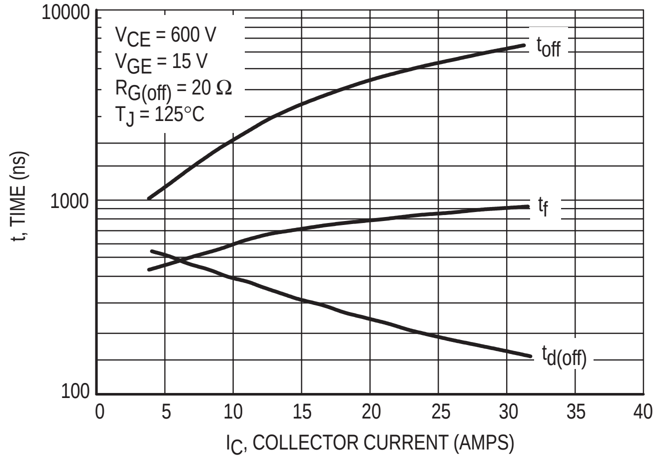


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

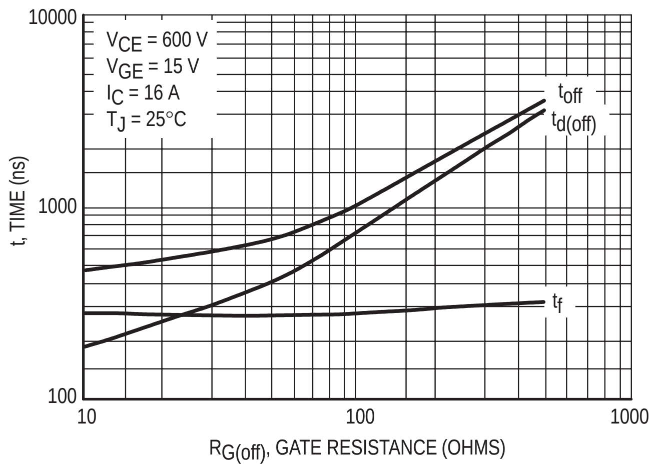


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

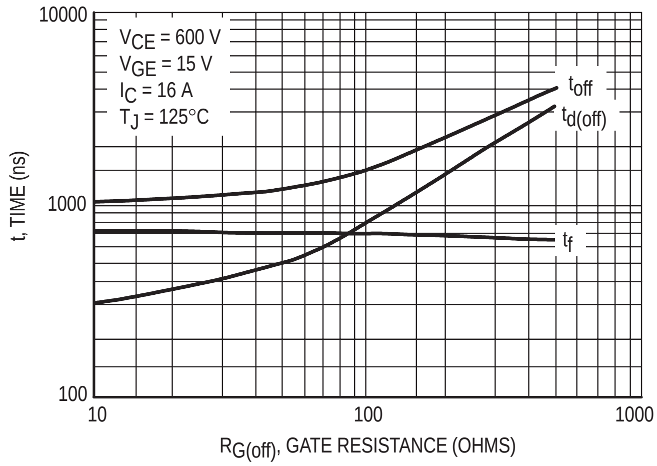


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

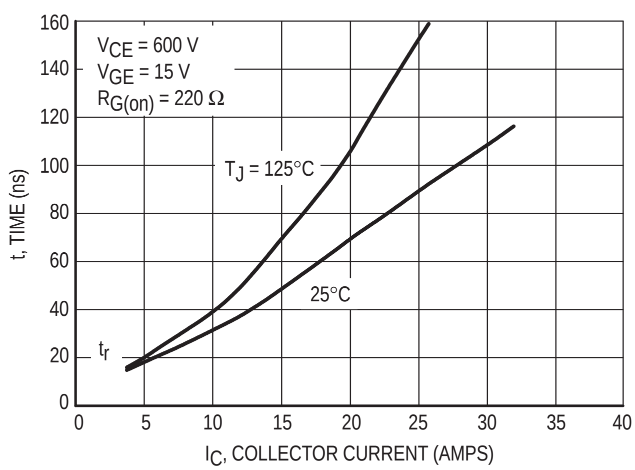


Figure 11. Inductive Switching Times versus Collector Current

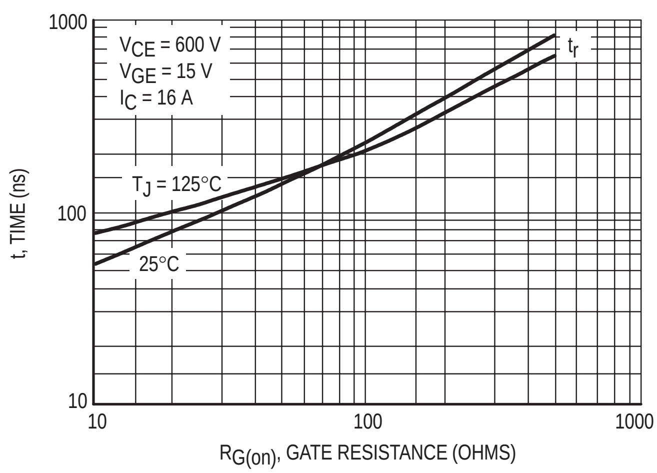


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

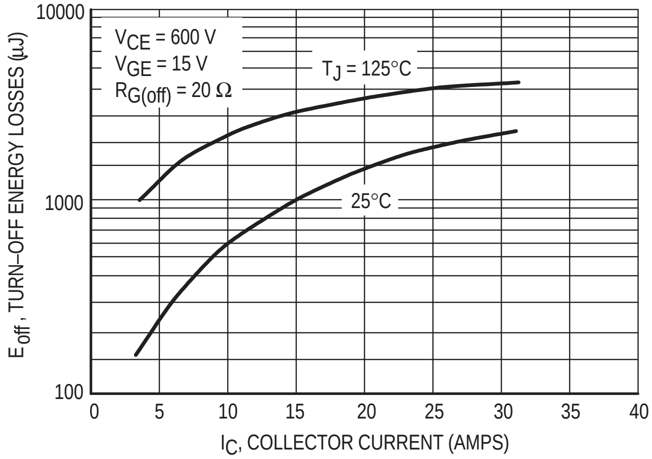


Figure 13. Turn–Off Energy Losses versus Collector Current

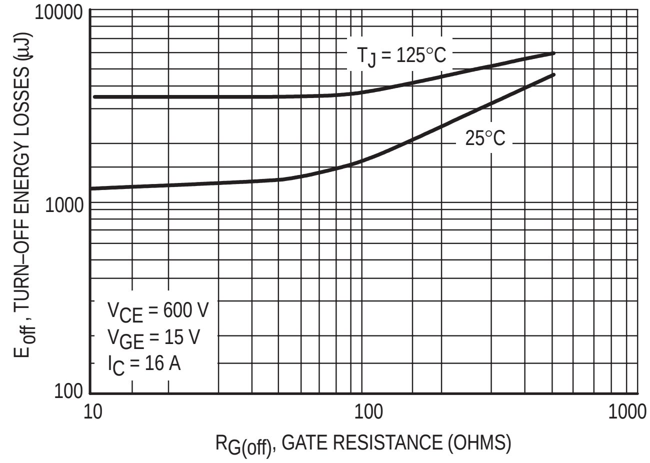


Figure 14. Turn–Off Energy Losses versus Gate Resistance

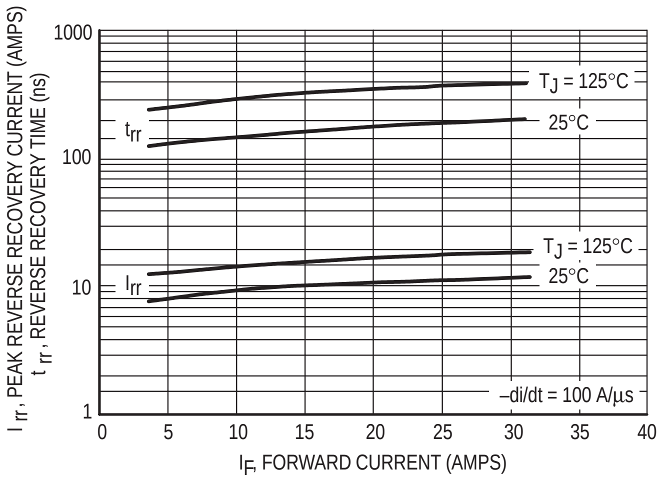


Figure 15. Reverse Recovery Characteristics – Free–Wheeling Diode

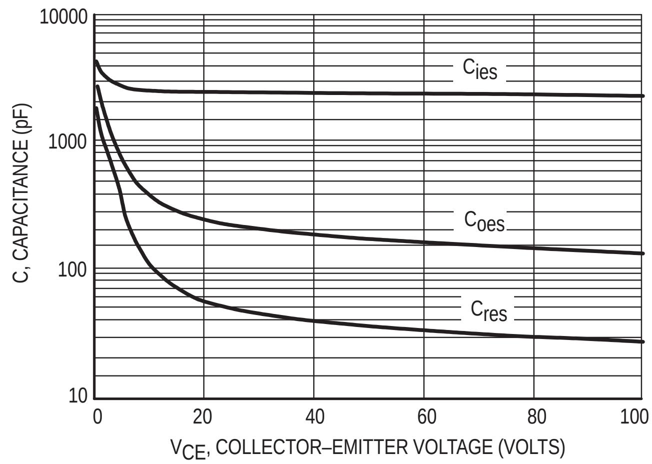


Figure 16. Capacitance Variation

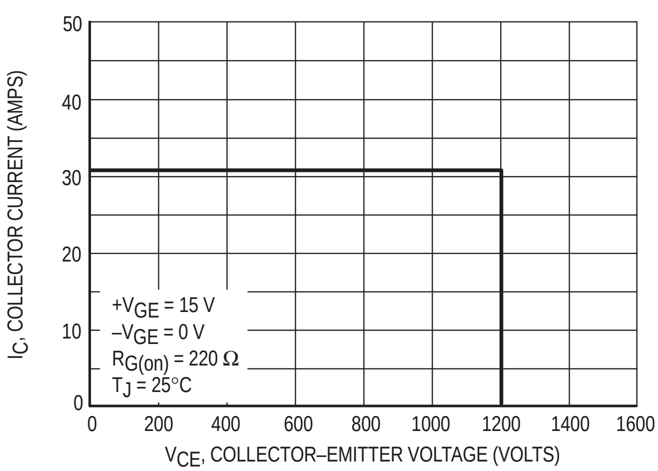


Figure 17. Reversed Biased Safe Operating Area (RBSOA)

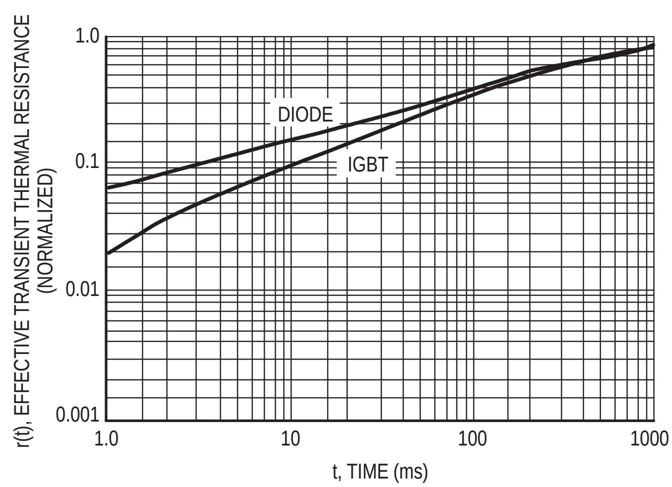
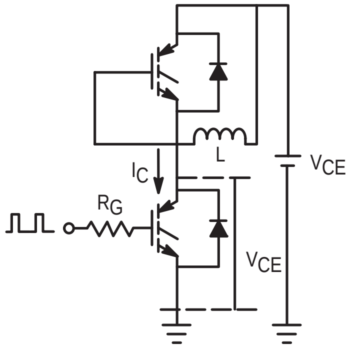


Figure 18. Thermal Response



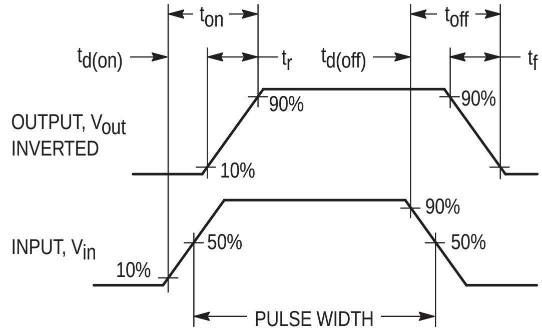


Figure 19. Inductive Switching Time Test Circuit and Timing Chart

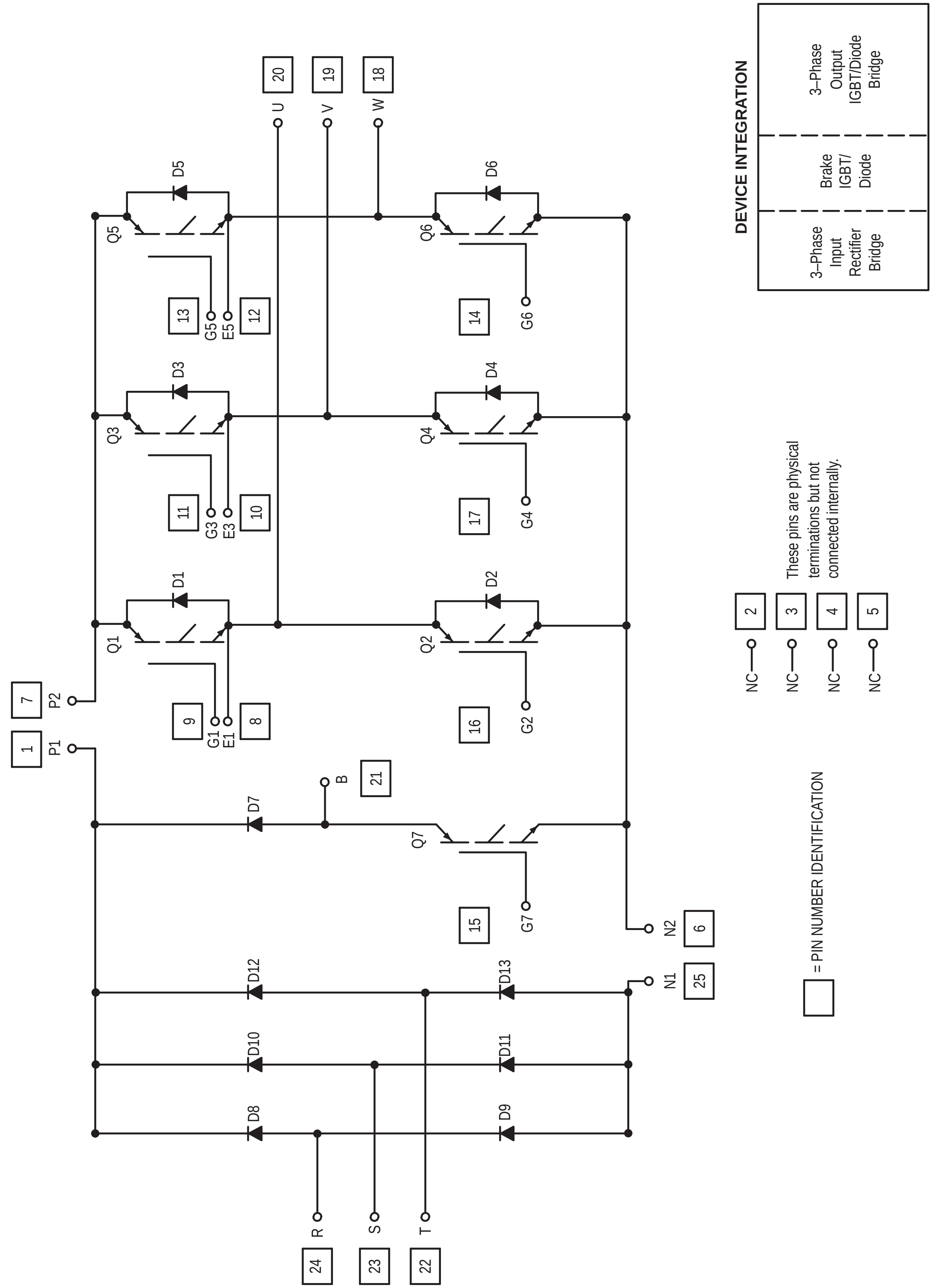


Figure 20. Integrated Power Stage Schematic

Hybrid Power Module

Integrated Power Stage for 5 hp Motor Drives

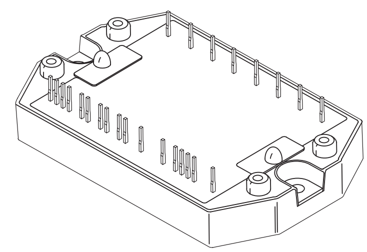
(This device is not recommended for new designs)
(This device is replaced by MHPM7A25S120DC3)

MHPM7A25A120B

25 AMP, 1200 VOLT
HYBRID POWER MODULE

This module integrates a 3-phase input rectifier bridge, 3-phase output inverter, brake transistor/diode, current sense resistor and temperature sensor in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free-wheeling diodes to give optimal dynamic performance. It has been configured for use as a three-phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- DC Bus Current Sense Resistor Included
- Short Circuit Rated 10 µs @ 25°C, 600 V
- Temperature Sensor Included
- Pin-to-Baseplate Isolation exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440A–02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	25	A
Peak Non-Repetitive Surge Current (1/2 cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	25	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	50	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	25	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	50	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	75	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600 V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1.0 ms = 1.0% duty cycle

REV 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	25	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	50	A
IGBT Power Dissipation	P_D	75	W
Diode Reverse Voltage	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	25	A
Peak Output Diode Current	$I_{F(pk)}$	50	A
TOTAL MODULE			
Isolation Voltage (47–63 Hz, 1 min. duration)	V_{iso}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to +90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	—	6.0	lb•in

(1) 1 cycle = 50 or 60 Hz
(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	—	5.0	50	µA
Forward Voltage (I_F = 25 A)	V_F	—	1.1	1.5	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	—	—	2.2	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 — —	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (I_C = 10 mA, V_{CE} = V_{GE})	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	—	—	V
Collector-Emitter Saturation Voltage (I_C = 25 A, V_{GE} = 15 V)	$V_{CE(SAT)}$	—	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	4540	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V)	Q_T	—	165	—	nC
Fall Time — Inductive Load (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	350	500	ns
Turn-On Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	9.0	mJ
Turn-Off Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	4.5	mJ
Free Wheeling Diode Forward Voltage (I_F = 25 A, V_{GE} = 0 V)	V_F	—	1.9	2.4	V
Free Wheeling Diode Reverse Recovery Time (I_F = 25 A, V = 600 V, di/dt = 200 A/µs)	t_{rr}	—	150	250	ns
Free Wheeling Diode Stored Charge (I_F = 25 A, V = 600 V, di/dt = 200 A/µs)	Q_{rr}	—	—	1050	nC
Thermal Resistance — IGBT (Each Die)	$R_{\theta JC}$	—	—	1.4	°C/W
Thermal Resistance — Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	—	—	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	— —	6.0 2000	100 —	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 25 A)	$V_{CE(SAT)}$	—	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	4540	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V)	Q_T	—	165	—	nC
Fall Time — Inductive Load (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	350	500	ns
Turn-On Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	9.0	mJ
Turn-Off Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	4.5	mJ
Output Diode Forward Voltage (I_F = 25 A)	V_F	—	1.9	2.4	V
Output Diode Reverse Leakage Current	I_R	—	—	50	µA
Thermal Resistance — IGBT	$R_{\theta JC}$	—	—	1.4	°C/W
Thermal Resistance — Output Diode	$R_{\theta JC}$	—	—	2.2	°C/W
SENSE RESISTOR					
Resistance	R_{sense}	—	5	—	mΩ
Resistance Tolerance	R_{tol}	–1.0	—	+1.0	%
TEMPERATURE SENSE DIODE					
Forward Voltage (@ I_F = 1.0 mA)	V_F	—	.66	—	V
Forward Voltage Temperature Coefficient (@ I_F = 1.0 mA)	TC_{VF}	—	–1.95	—	mV/°C

Typical Characteristics

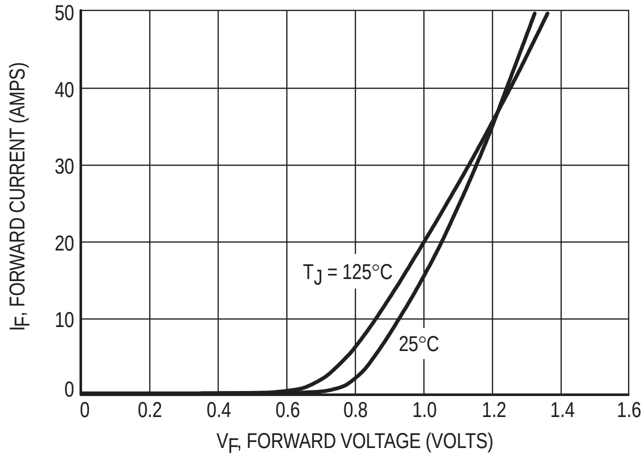


Figure 1. Forward Characteristics – Input Rectifier

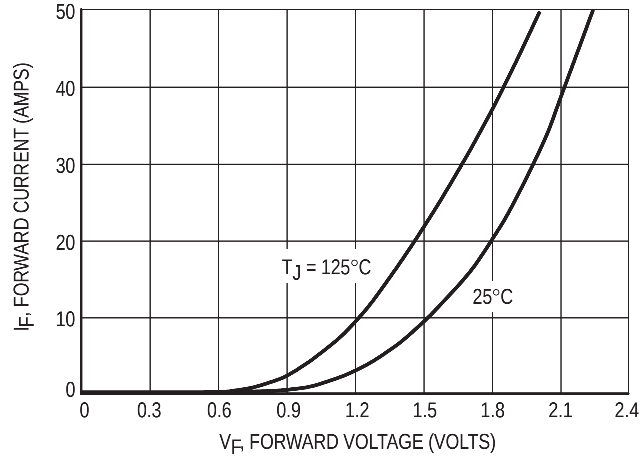


Figure 2. Forward Characteristics Free–Wheeling Diode

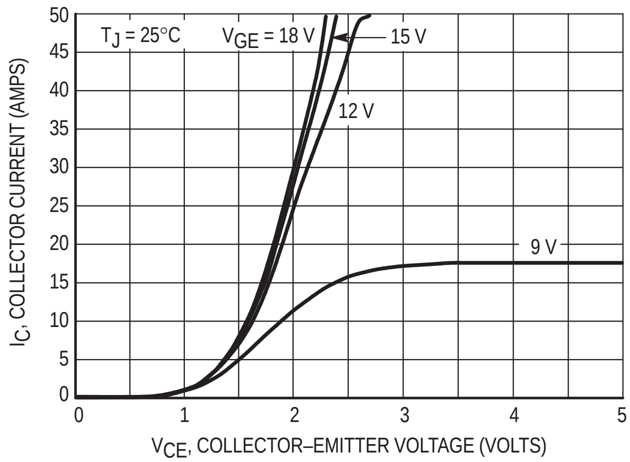


Figure 3. Forward Characteristics, T_J = 25°C

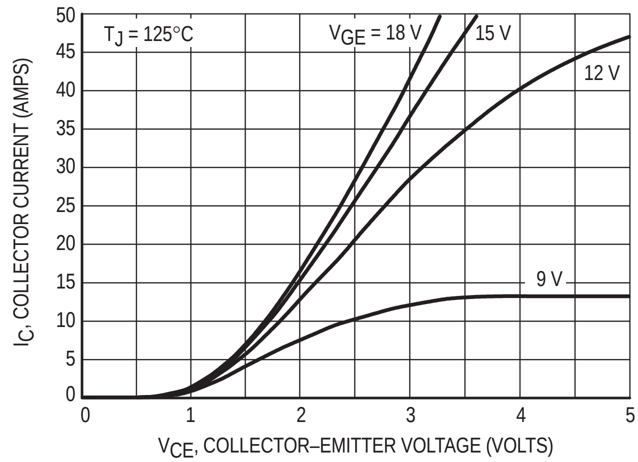


Figure 4. Forward Characteristics, T_J = 125°C

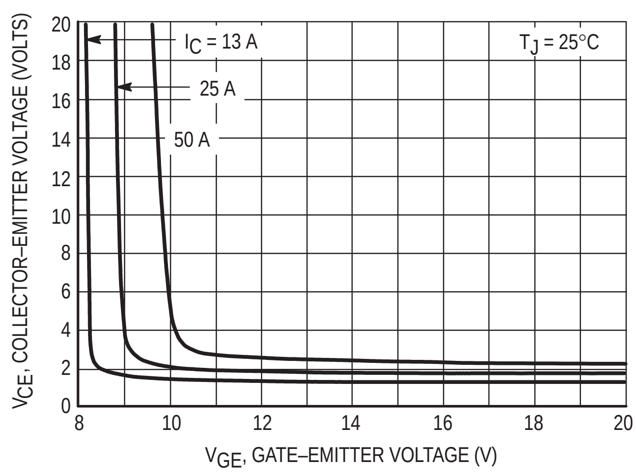


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

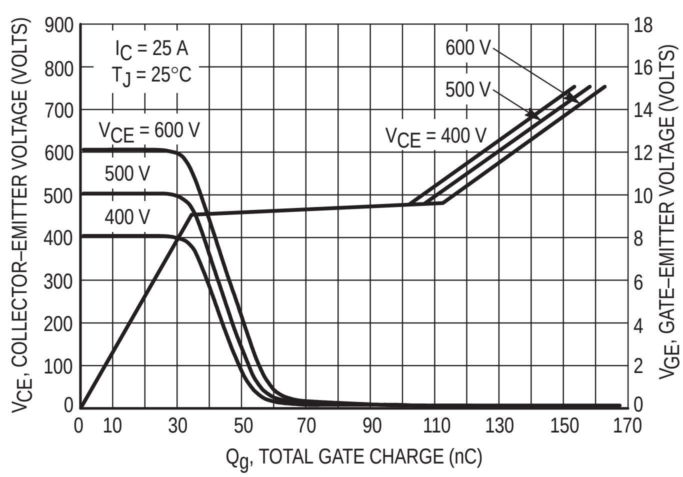


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

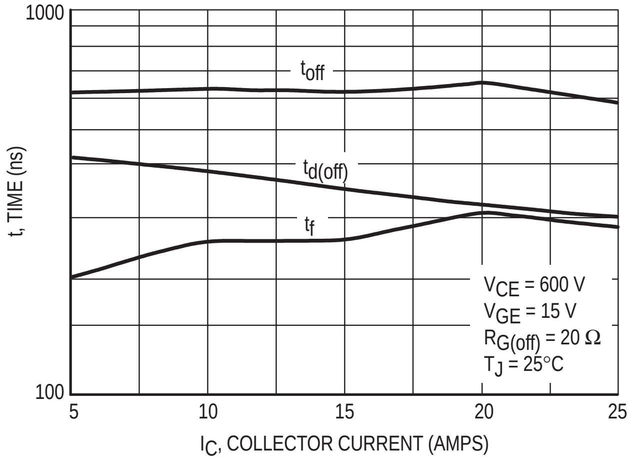


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

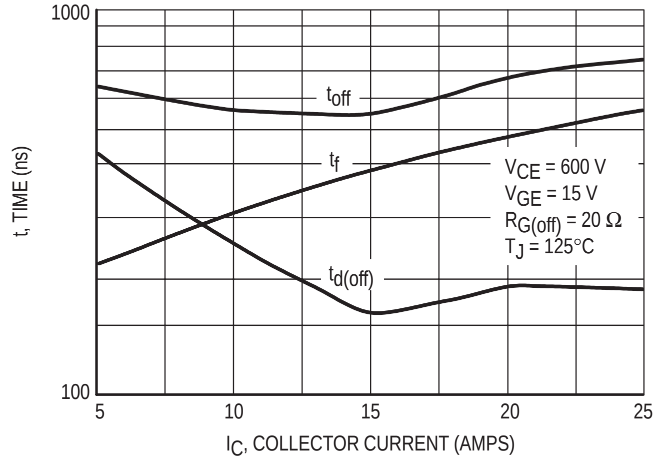


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

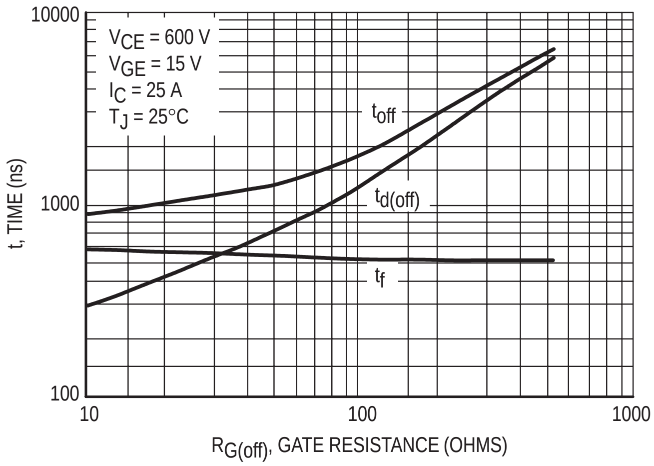


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

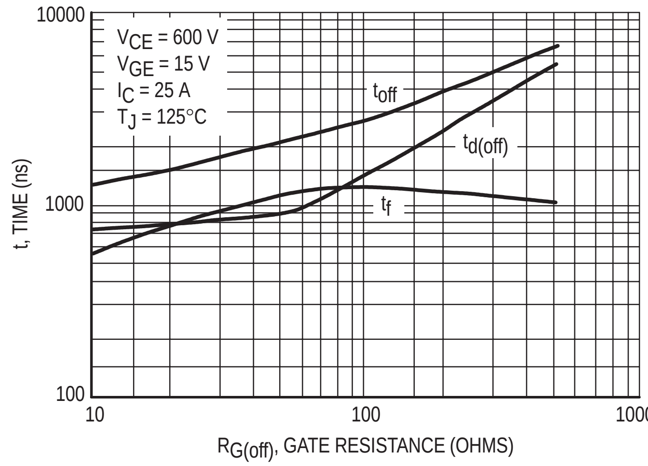


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

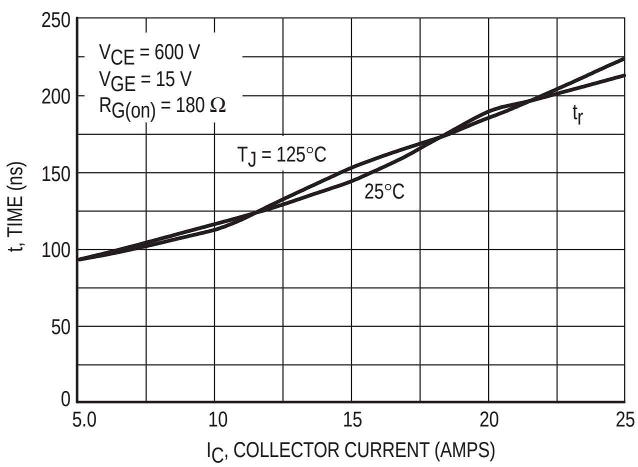


Figure 11. Inductive Switching Times versus Collector Current

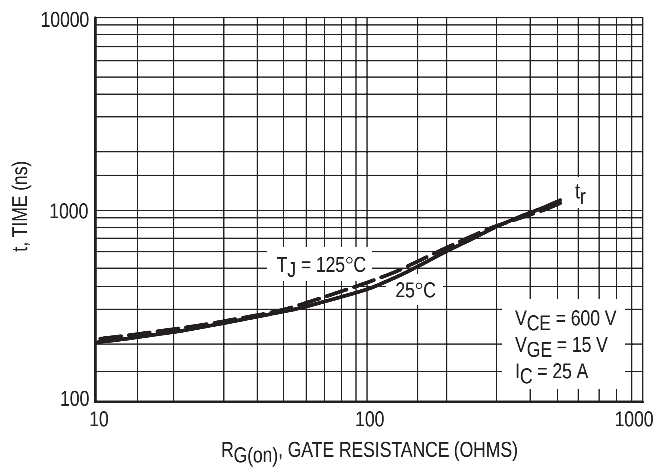


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

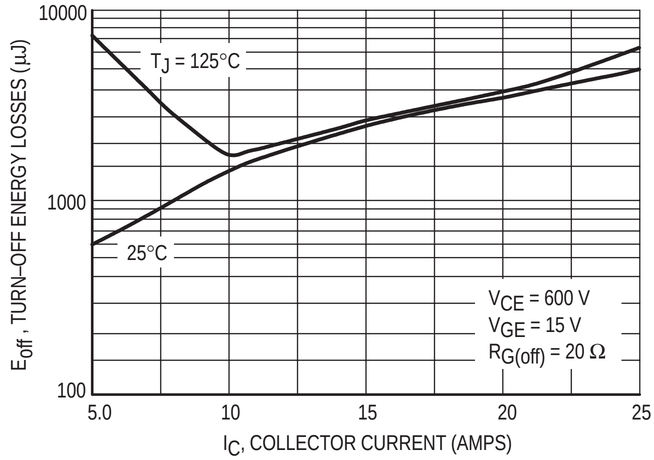


Figure 13. Turn–Off Energy Losses versus Collector Current

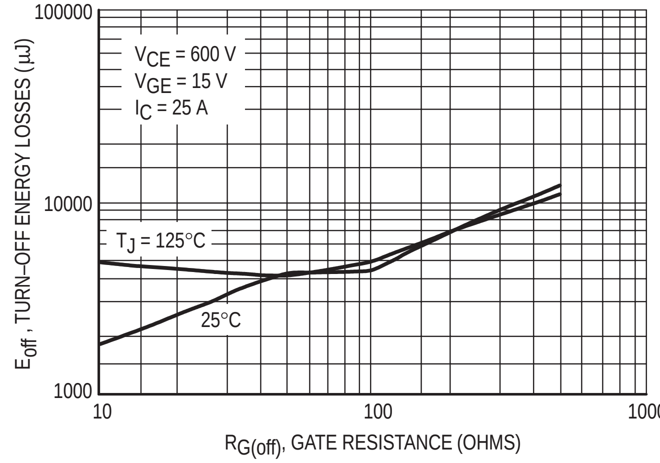


Figure 14. Turn–Off Energy Losses versus Gate Resistance

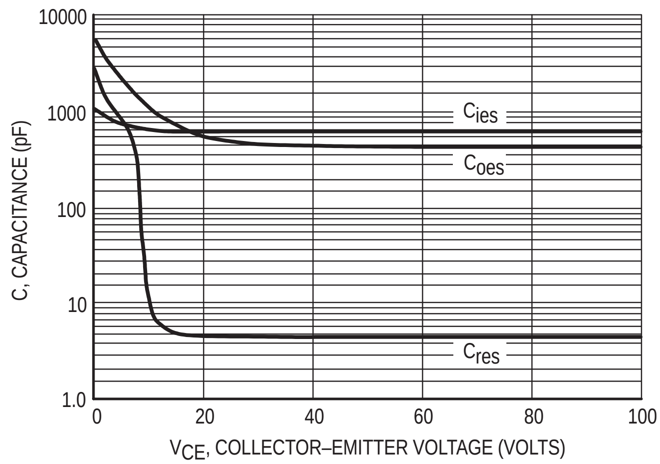


Figure 15. Capacitance Variation

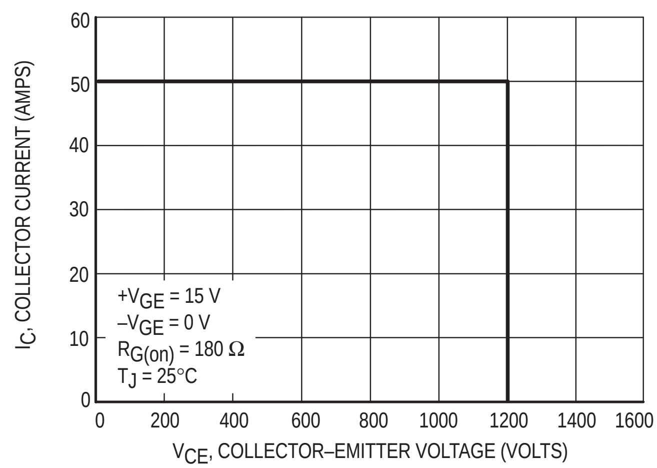


Figure 16. Reversed Biased Safe Operating Area (RBSOA)

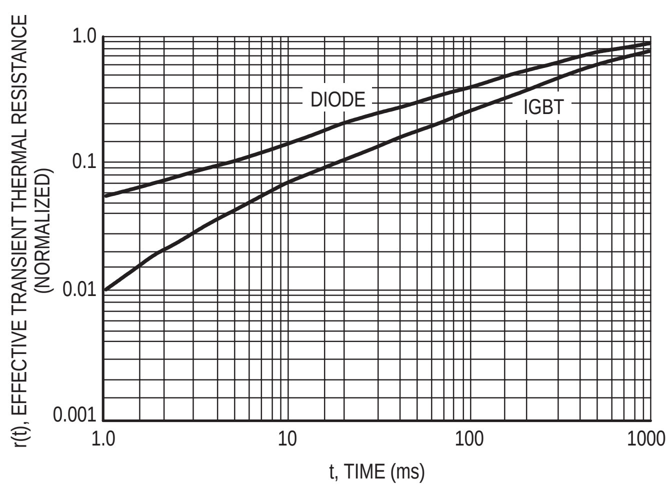


Figure 17. Thermal Response

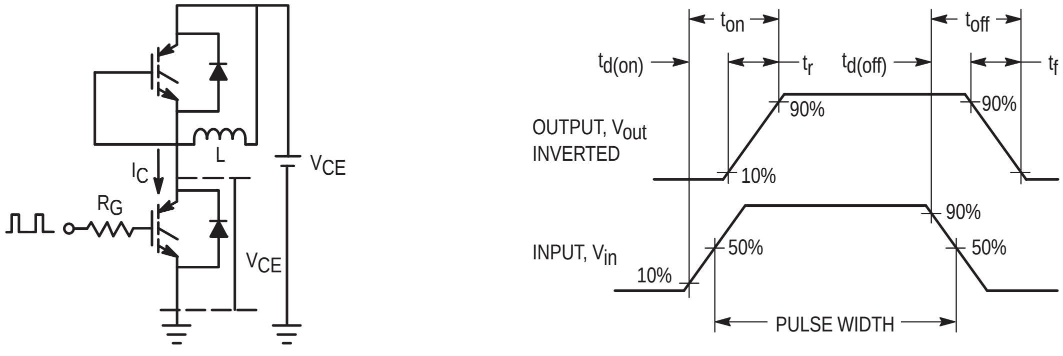


Figure 18. Inductive Switching Time Test Circuit and Timing Chart

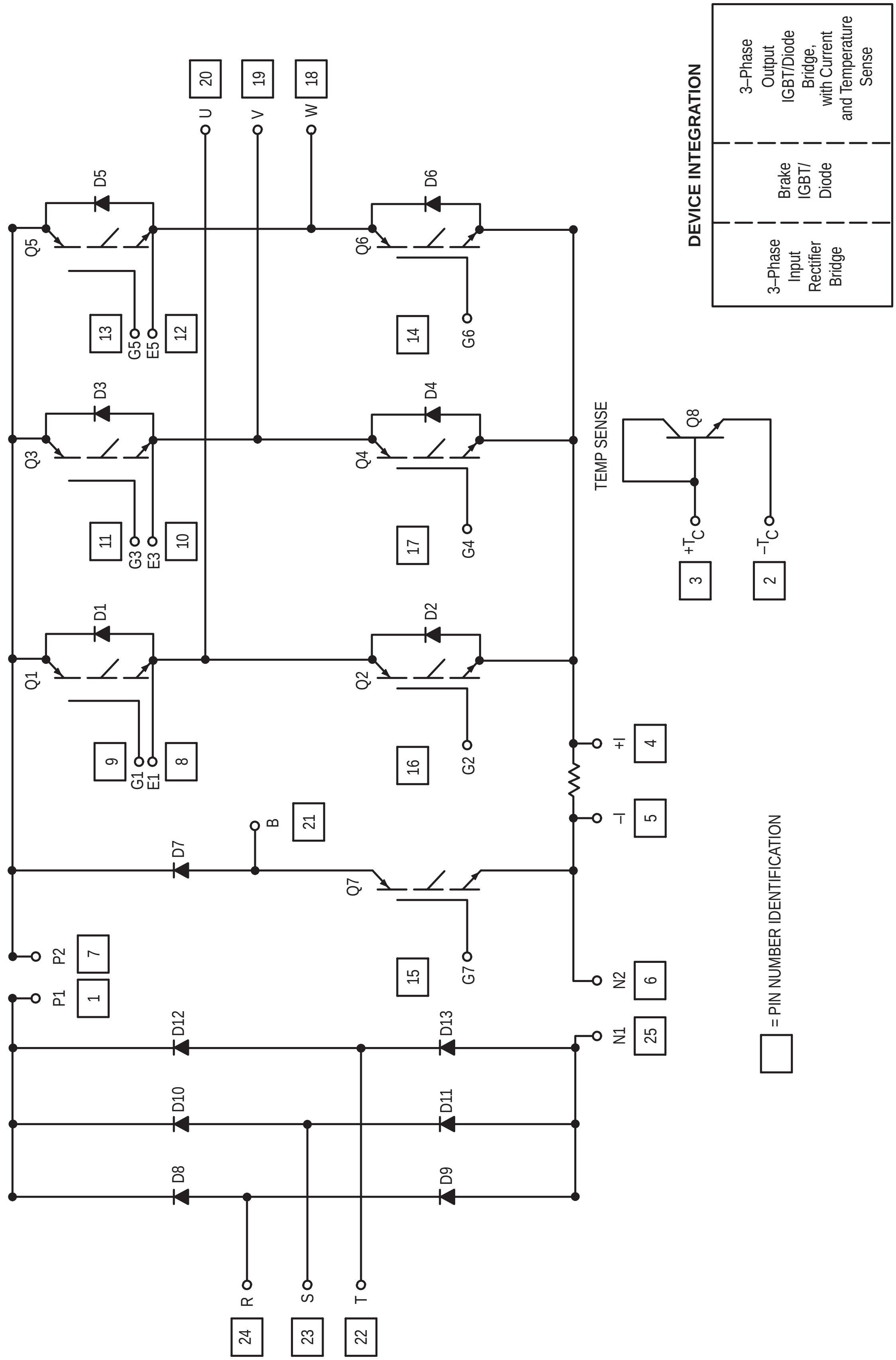


Figure 19. Integrated Power Stage Schematic

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Hybrid Power Module

Integrated Power Stage for 5 hp Motor Drives

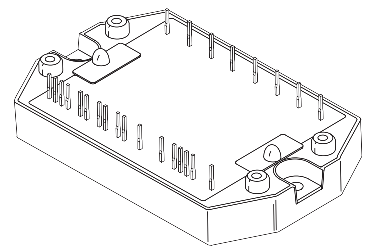
(This device is not recommended for new designs)
(This device is replaced by MHPM7A25S120DC3)

MHPM7B25A120B

25 AMP, 1200 VOLT
HYBRID POWER MODULE

This module integrates a 3-phase input rectifier bridge, 3-phase output inverter and brake transistor/diode in a single convenient package. The output inverter utilizes advanced insulated gate bipolar transistors (IGBT) matched with free-wheeling diodes to give optimal dynamic performance. It has been configured for use as a three-phase motor drive module or for many other power switching applications. The top connector pins have been designed for easy interfacing to the user's control board.

- Short Circuit Rated 10 µs @ 25°C, 600V
- Pin-to-Baseplate Isolation exceeds 2500 Vac (rms)
- Convenient Package Outline
- UL Recognized
- Access to Positive and Negative DC Bus
- Visit our website at http://www.mot–sps.com/tsg/



PLASTIC PACKAGE
CASE 440A–02, Style 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT RECTIFIER BRIDGE			
Peak Repetitive Reverse Voltage (T_J = 125°C)	V_{RRM}	1200	V
Average Output Rectified Current	I_O	25	A
Peak Non-Repetitive Surge Current(1/2 cycle)(1)	I_{FSM}	200	A
OUTPUT INVERTER			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	25	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	50	A
Continuous Free-Wheeling Diode Current	I_{Fmax}	25	A
Peak Repetitive Free-Wheeling Diode Current(2)	$I_{F(pk)}$	50	A
IGBT Power Dissipation per die (T_C = 95°C)	P_D	75	W
Free-Wheeling Diode Power Dissipation per die (T_C = 95°C)	P_D	40	W
Junction Temperature Range	T_J	– 40 to +125	°C
Short Circuit Duration (V_{CE} = 600V, T_J = 25°C)	t_{sc}	10	µs

(1) 1 cycle = 50 or 60 Hz
(2) 1.0 ms = 1.0% duty cycle

REV 1

MAXIMUM DEVICE RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
BRAKE CIRCUIT			
IGBT Reverse Voltage	V_{CES}	1200	V
Gate-Emitter Voltage	V_{GES}	± 20	V
Continuous IGBT Collector Current	I_{Cmax}	25	A
Peak Repetitive IGBT Collector Current(2)	$I_{C(pk)}$	50	A
IGBT Power Dissipation	P_D	75	W
Diode Reverse Voltage	V_{RRM}	1200	V
Continuous Output Diode Current	I_{Fmax}	25	A
Peak Output Diode Current	$I_{F(pk)}$	50	A
TOTAL MODULE			
Isolation Voltage (47– 63 Hz, 1 min. duration)	V_{iso}	2500	Vac
Operating Case Temperature Range	T_C	– 40 to +90	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C
Mounting Torque	—	6.0	lb•in

(1) 1 cycle = 50 or 60 Hz
(2) 1.0 ms = 1.0% duty cycle

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT RECTIFIER BRIDGE					
Reverse Leakage Current (V_{RRM} = 1200 V)	I_R	—	5.0	50	µA
Forward Voltage (I_F = 25 A)	V_F	—	2.5	2.85	V
Thermal Resistance (Each Die)	$R_{\theta JC}$	—	—	2.2	°C/W
OUTPUT INVERTER					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 — —	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 25 A)	$V_{CE(SAT)}$	—	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	4540	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V)	Q_T	—	165	—	nC
Fall Time — Inductive Load (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	350	500	ns
Turn-On Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	9.0	mJ
Turn-Off Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	4.5	mJ
Free Wheeling Diode Forward Voltage (I_F = 16 A, V_{GE} = 0 V)	V_F	—	1.9	2.4	V
Free Wheeling Diode Reverse Recovery Time (I_F = 25 A, V = 600 V, di/dt = 200 A/µs)	t_{rr}	—	150	250	ns
Free Wheeling Diode Stored Charge (I_F = 25 A, V = 600 V, di/dt = 200 A/µs)	Q_{rr}	—	—	1050	nC
Thermal Resistance — IGBT (Each Die)	$R_{\theta JC}$	—	—	1.4	°C/W
Thermal Resistance — Free-Wheeling Diode (Each Die)	$R_{\theta JC}$	—	—	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BRAKE CIRCUIT					
Gate-Emitter Leakage Current (V_{CE} = 0 V, V_{GE} = ± 20 V)	I_{GES}	—	—	± 20	µA
Collector-Emitter Leakage Current (V_{CE} = 1200 V, V_{GE} = 0 V) T_J = 25°C T_J = 125°C	I_{CES}	 — —	 6.0 2000	 100	µA
Gate-Emitter Threshold Voltage (V_{CE} = V_{GE}, I_C = 10 mA)	$V_{GE(th)}$	4.0	6.0	8.0	V
Collector-Emitter Breakdown Voltage (I_C = 10 mA, V_{GE} = 0)	$V_{(BR)CES}$	1200	—	—	V
Collector-Emitter Saturation Voltage (V_{GE} = 15 V, I_C = 25 A)	$V_{CE(SAT)}$	—	2.5	3.5	V
Input Capacitance (V_{GE} = 0 V, V_{CE} = 10 V, f = 1.0 MHz)	C_{ies}	—	4500	—	pF
Input Gate Charge (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V)	Q_T	—	165	—	nC
Fall Time — Inductive Load (V_{CE} = 600 V, I_C = 25 A, V_{GE} = +15 V, $R_{G(off)}$ = 20 Ω)	t_f	—	350	500	ns
Turn-On Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(on)}$ = 180 Ω)	E_{on}	—	—	9.0	mJ
Turn-Off Energy (I_C = 25 A, V_{CE} = 600 V, $R_{G(off)}$ = 20 Ω)	E_{off}	—	—	4.5	mJ
Output Diode Forward Voltage (I_F = 25 A)	V_F	—	1.9	2.4	V
Output Diode Reverse Leakage Current	I_R	—	—	50	µA
Thermal Resistance — IGBT	$R_{\theta JC}$	—	—	1.4	°C/W
Thermal Resistance — Output Diode	$R_{\theta JC}$	—	—	2.2	°C/W

Typical Characteristics

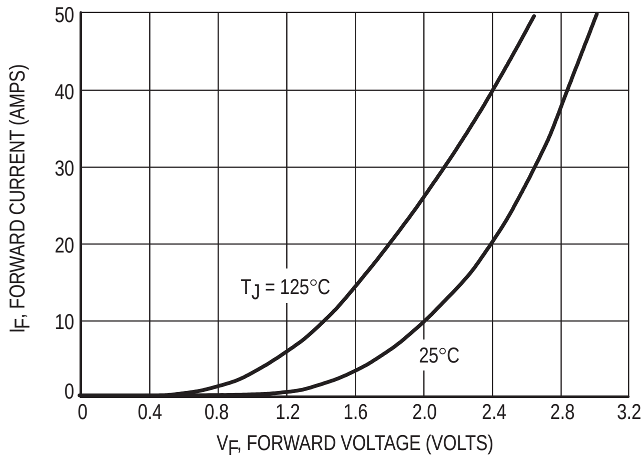


Figure 1. Forward Characteristics – Input Rectifier

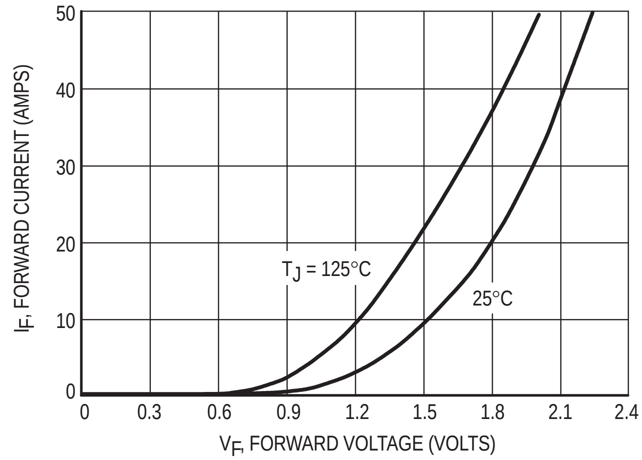


Figure 2. Forward Characteristics Free–Wheeling Diode

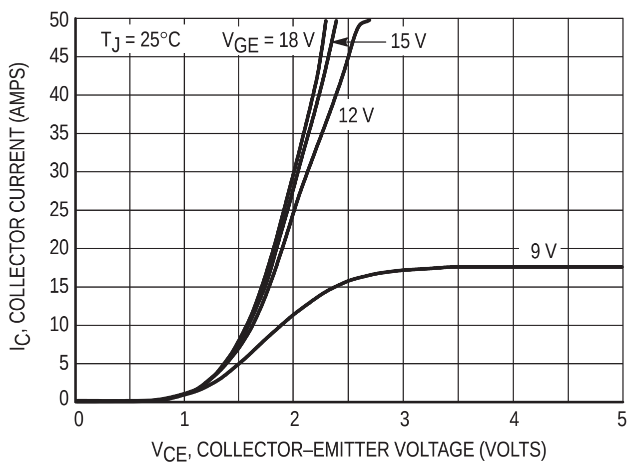


Figure 3. Forward Characteristics, T_J = 25°C

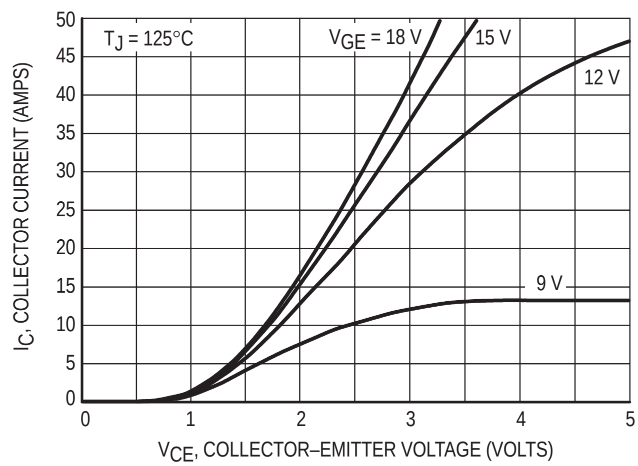


Figure 4. Forward Characteristics, T_J = 125°C

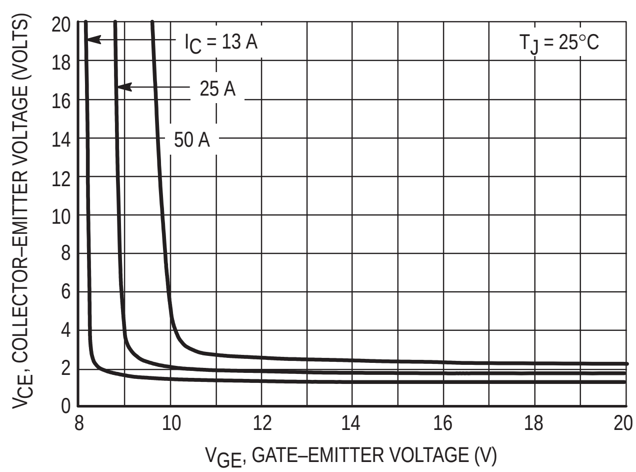


Figure 5. Collector–Emitter Voltage versus Gate–Emitter Voltage

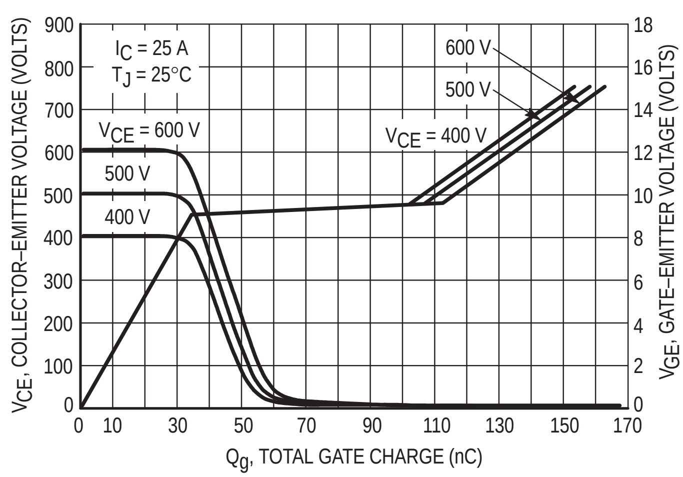


Figure 6. Collector–Emitter and Gate–Emitter Voltages versus Total Gate Charge

Typical Characteristics

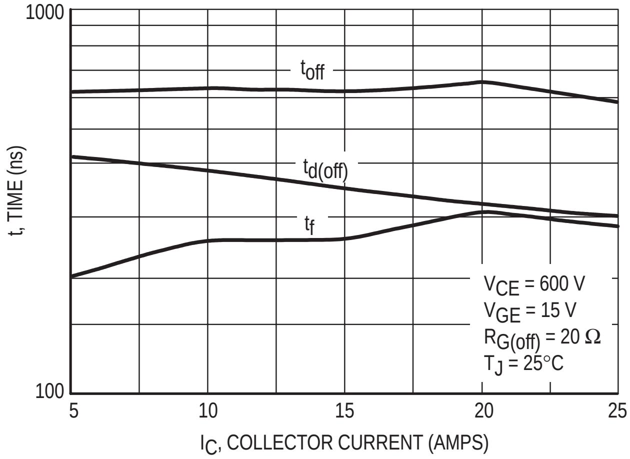


Figure 7. Inductive Switching Times versus Collector Current, T_J = 25°C

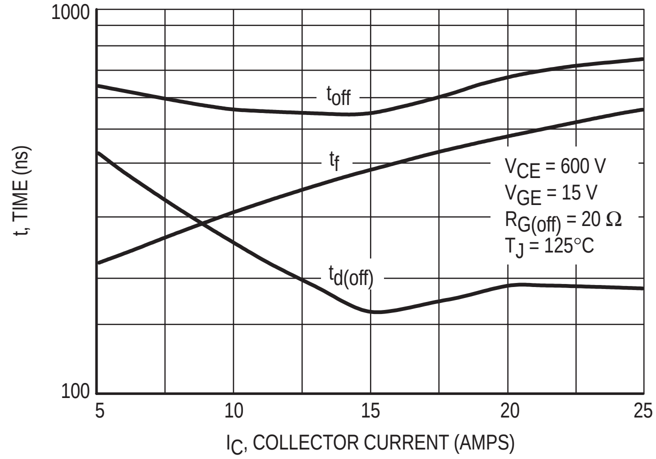


Figure 8. Inductive Switching Times versus Collector Current, T_J = 125°C

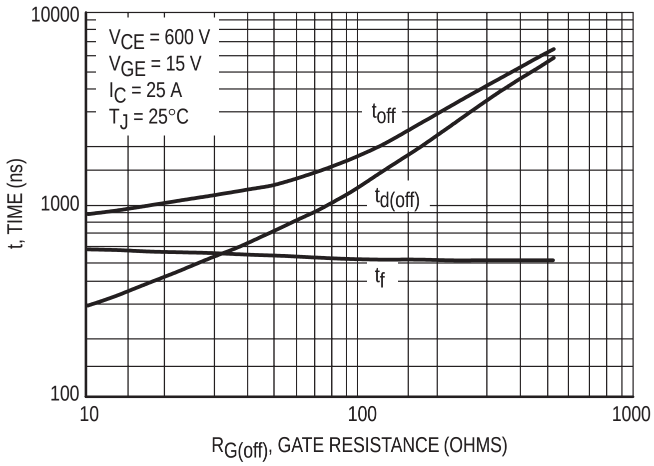


Figure 9. Inductive Switching Times versus Gate Resistance, T_J = 25°C

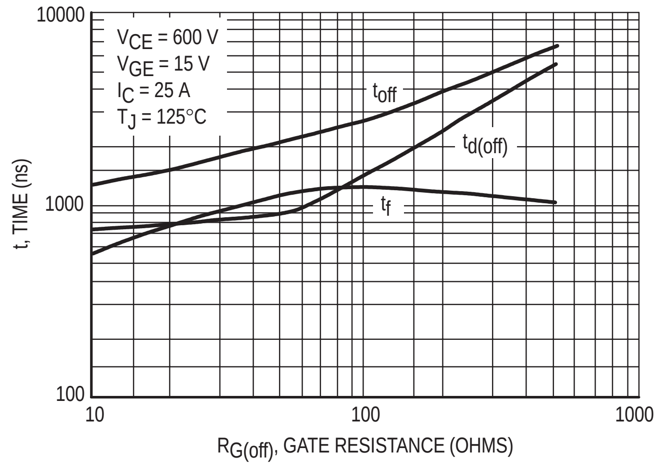


Figure 10. Inductive Switching Times versus Gate Resistance, T_J = 125°C

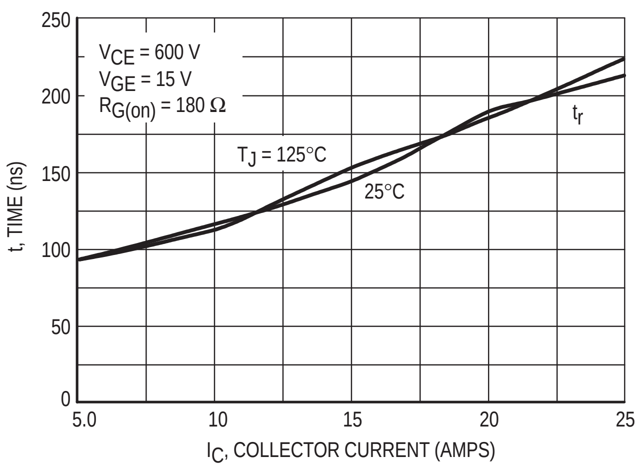


Figure 11. Inductive Switching Times versus Collector Current

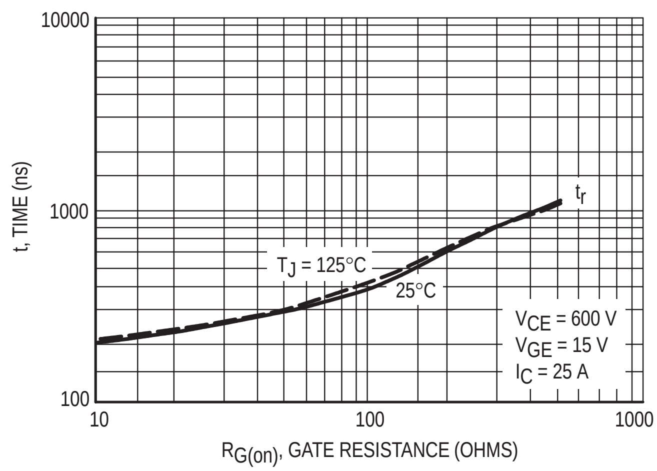


Figure 12. Inductive Switching Times versus Gate Resistance

Typical Characteristics

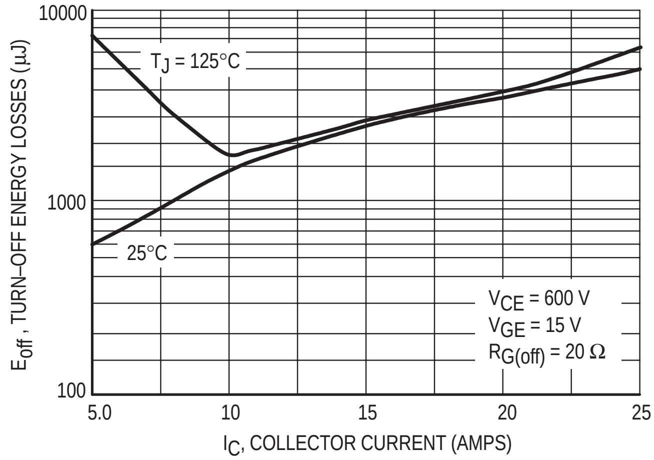


Figure 13. Turn–Off Energy Losses versus Collector Current

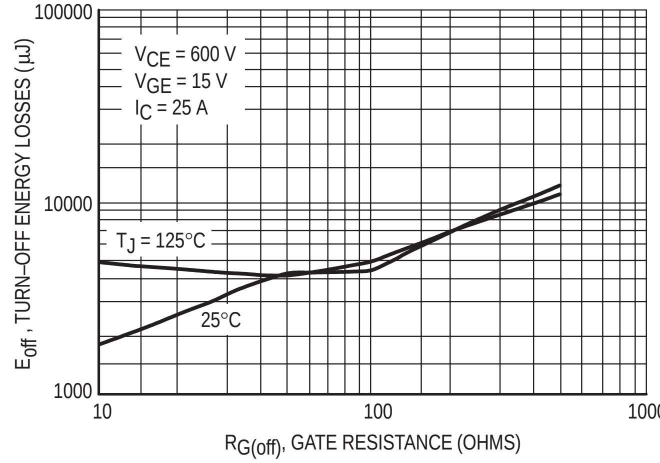


Figure 14. Turn–Off Energy Losses versus Gate Resistance

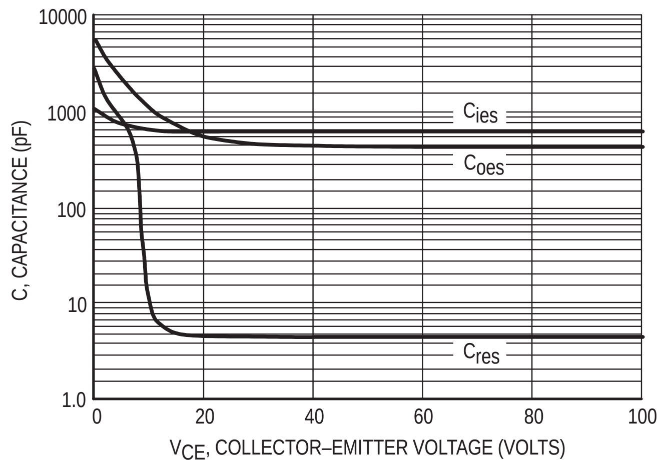


Figure 15. Capacitance Variation

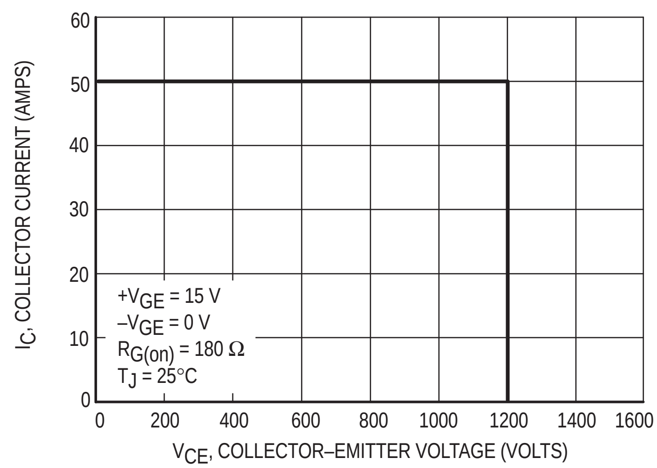


Figure 16. Reversed Biased Safe Operating Area (RBSOA)

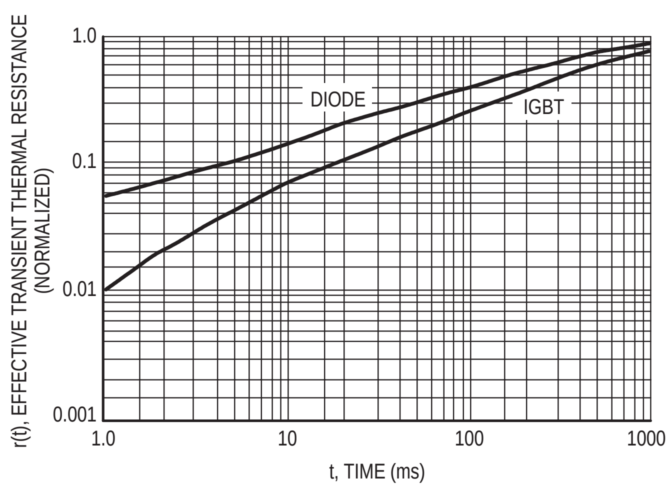


Figure 17. Thermal Response

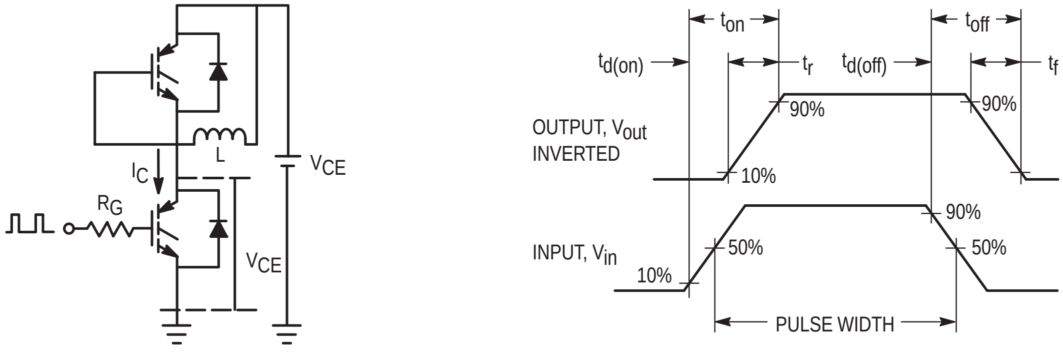


Figure 18. Inductive Switching Time Test Circuit and Timing Chart

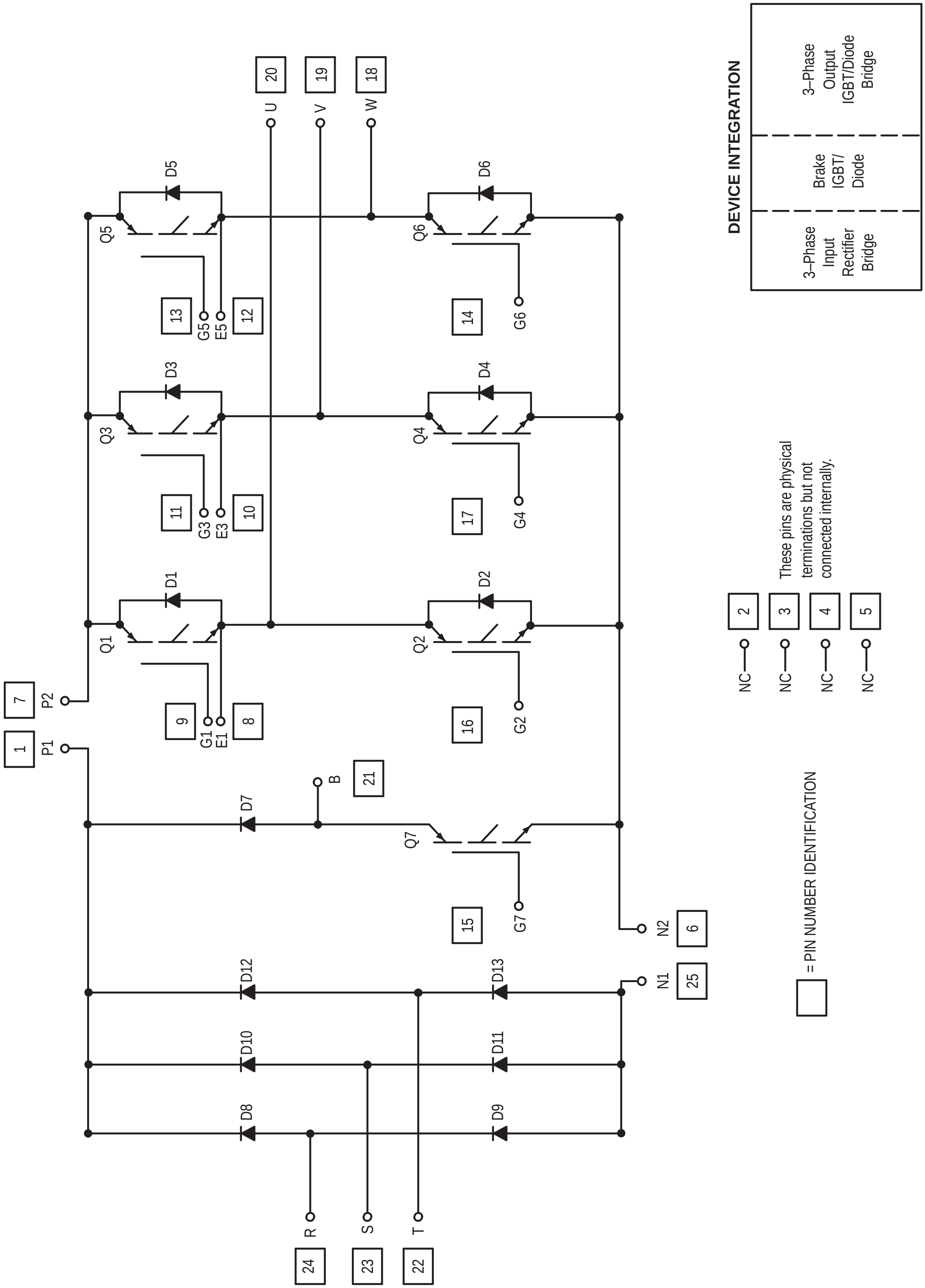


Figure 19. Integrated Power Stage Schematic

MOTOROLA

MC33153

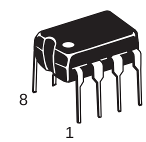
Single IGBT Gate Driver

The MC33153 is specifically designed as an IGBT driver for high power applications that include ac induction motor control, brushless dc motor control and uninterruptable power supplies. Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors. Device protection features include the choice of desaturation or overcurrent sensing and undervoltage detection. These devices are available in dual–in–line and surface mount packages and include the following features:

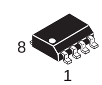
- High Current Output Stage: 1.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimized for IGBT's
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

SINGLE IGBT GATE DRIVER

SEMICONDUCTOR TECHNICAL DATA

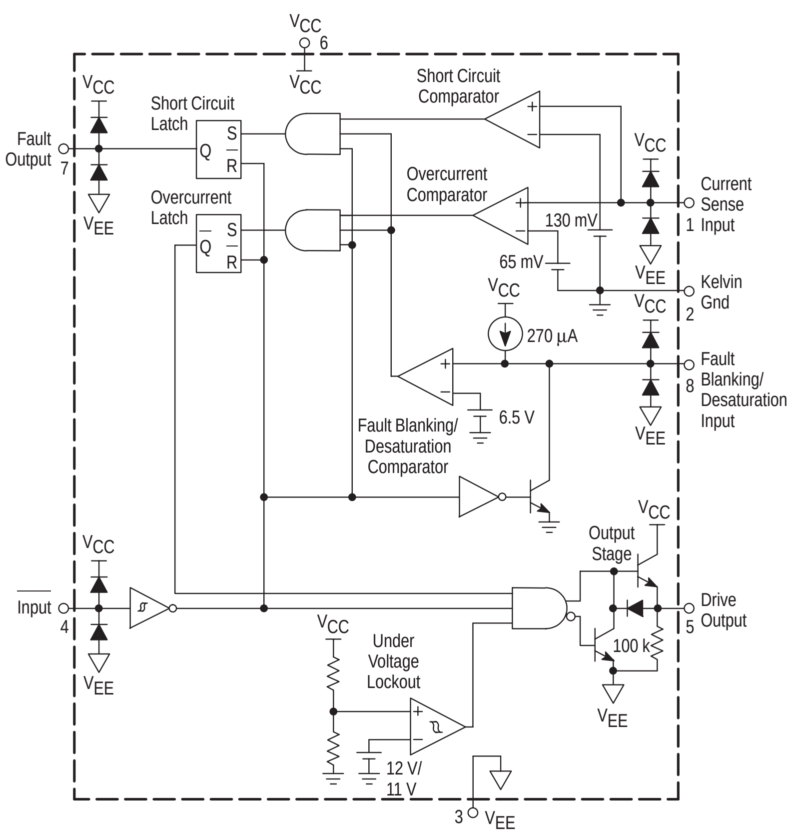


P SUFFIX
PLASTIC PACKAGE
CASE 626



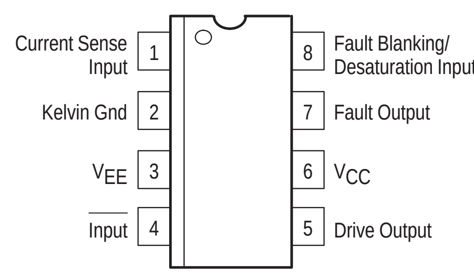
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Block Diagram



This device contains 133 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33153D	T_A = –40° to +105°C	SO–8
MC33153P		DIP–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage V_{CC} to V_{EE} Kelvin Ground to V_{EE} (Note 1)	 $V_{CC} – V_{EE}$ KGnd – V_{EE}	 20 20	V
Logic Input	V_{in}	V_{EE} –0.3 to V_{CC}	V
Current Sense Input	V_S	–0.3 to V_{CC}	V
Blanking/Desaturation Input	V_{BD}	–0.3 to V_{CC}	V
Gate Drive Output Source Current Sink Current Diode Clamp Current	I_O	 1.0 2.0 1.0	A
Fault Output Source Current Sink Curent	I_{FO}	 25 10	mA
Power Dissipation and Thermal Characteristics D Suffix SO–8 Package, Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air P Suffix DIP–8 Package, Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	–40 to +105	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT					
Input Threshold Voltage High State (Logic 1) Low State (Logic 0)	 V_{IH} V_{IL}	 – 1.2	 2.70 2.30	 3.2 –	V
Input Current High State (V_{IH} = 3.0 V) Low State (V_{IL} = 1.2 V)	 I_{IH} I_{IL}	 – –	 130 50	 500 100	μA
DRIVE OUTPUT					
Output Voltage Low State (I_{Sink} = 1.0 A) High State (I_{Source} = 500 mA)	 V_{OL} V_{OH}	 – 12	 2.0 13.9	 2.5 –	V
Output Pull–Down Resistor	R_{PD}	–	100	200	kΩ
FAULT OUTPUT					
Output voltage Low State (I_{Sink} = 5.0 mA) High State (I_{Source} = 20 mA)	 V_{FL} V_{FH}	 – 12	 0.2 13.3	 1.0 –	V
SWITCHING CHARACTERISTICS					
Propagation Delay (50% Input to 50% Output C_L = 1.0 nF) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	 $t_{PLH(in/out)}$ $t_{PHL\ (in/out)}$	 – –	 80 120	 300 300	ns
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	17	55	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	17	55	ns

NOTES: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (continued)					
Propagation Delay					µs
Current Sense Input to Drive Output	$t_{P(OC)}$	–	0.3	1.0	
Fault Blanking/Desaturation Input to Drive Output	$t_{P(FLT)}$	–	0.3	1.0	
UVLO					
Startup Voltage	$V_{CC\ start}$	11.3	12	12.6	V
Disable Voltage	$V_{CC\ dis}$	10.4	11	11.7	V
COMPARATORS					
Overcurrent Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SOC}	50	65	80	mV
Short Circuit Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SSC}	100	130	160	mV
Fault Blanking/Desaturation Threshold (V_{Pin1} > 100 mV)	$V_{th(FLT)}$	6.0	6.5	7.0	V
Current Sense Input Current (V_{SI} = 0 V)	I_{SI}	–	–1.4	–10	µA
FAULT BLANKING/DESATURATION INPUT					
Current Source (V_{Pin8} = 0 V, V_{Pin4} = 0 V)	I_{chg}	–200	–270	–300	µA
Discharge Current (V_{Pin8} = 15 V, V_{Pin4} = 5.0 V)	I_{dschg}	1.0	2.5	–	mA
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby ($V_{Pin\ 4}$ = V_{CC}, Output Open)		–	7.2	14	
Operating (C_L = 1.0 nF, f = 20 kHz)		–	7.9	20	

NOTES: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

Figure 1. Input Current versus Input Voltage

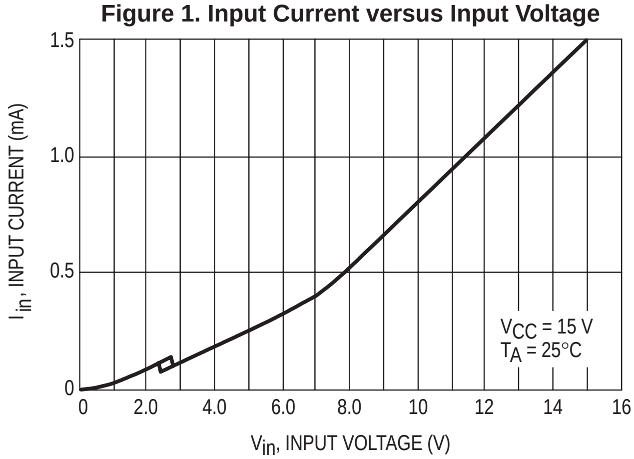


Figure 2. Output Voltage versus Input Voltage

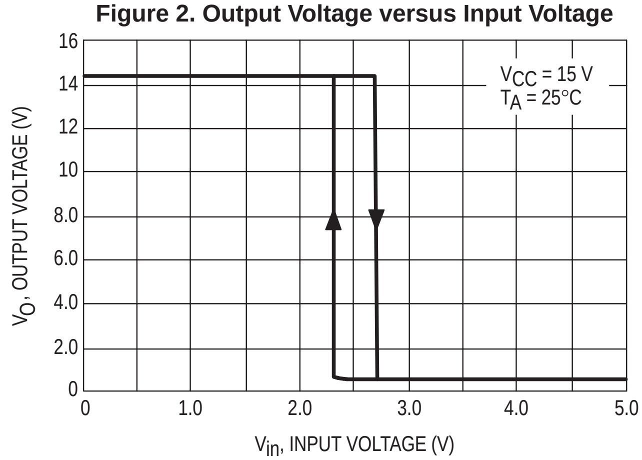


Figure 3. Input Threshold Voltage versus Temperature

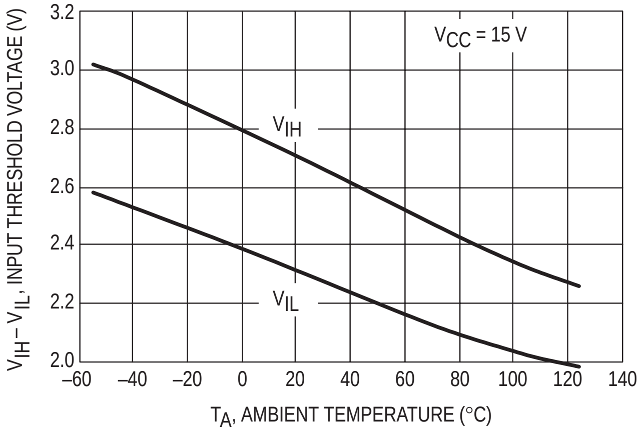


Figure 4. Input Threshold Voltage versus Supply Voltage

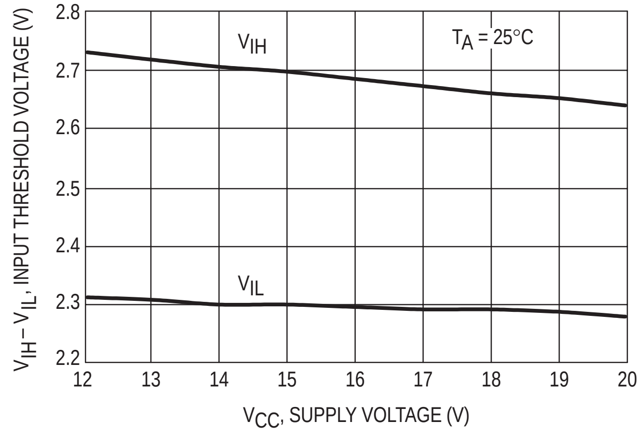


Figure 5. Drive Output Low State Voltage versus Temperature

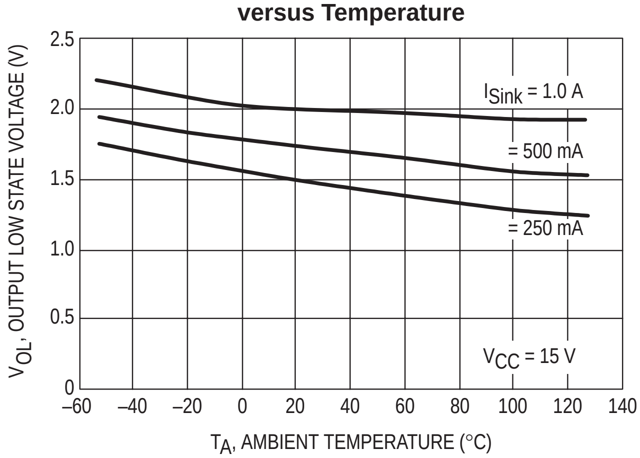


Figure 6. Drive Output Low State Voltage versus Sink Current

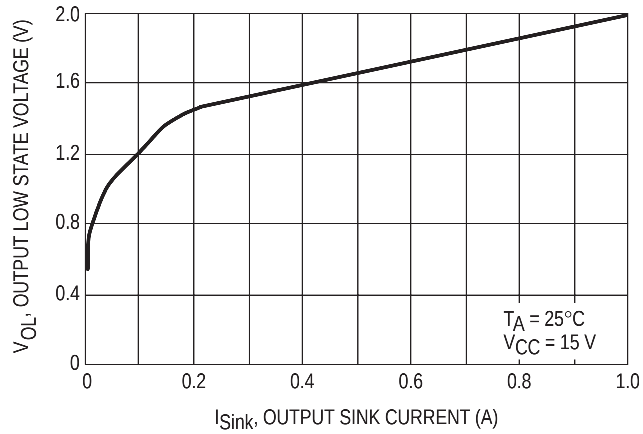


Figure 7. Drive Output High State Voltage versus Temperature

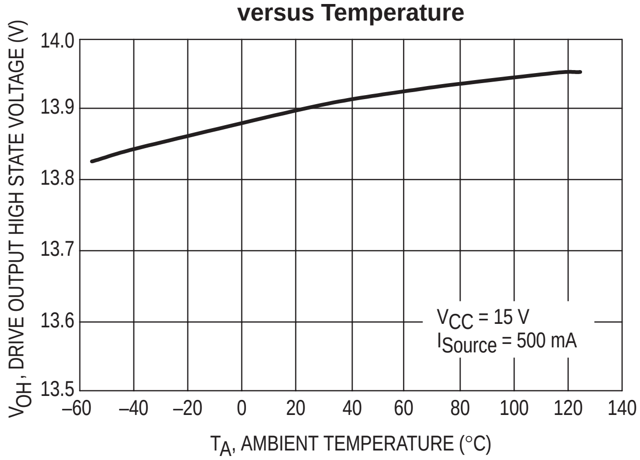


Figure 8. Drive Output High State Voltage versus Source Current

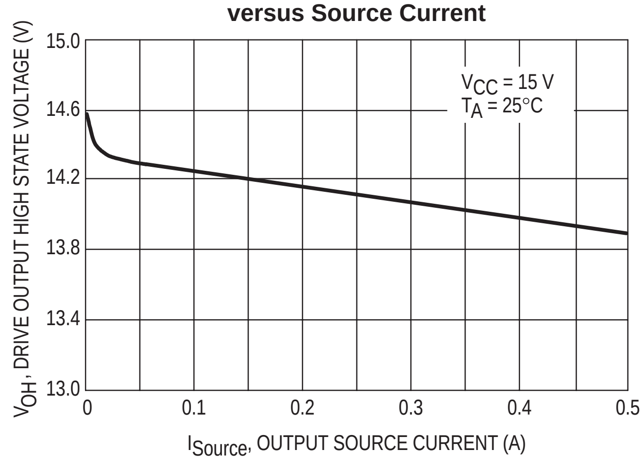


Figure 9. Drive Output Voltage versus Current Sense Input Voltage

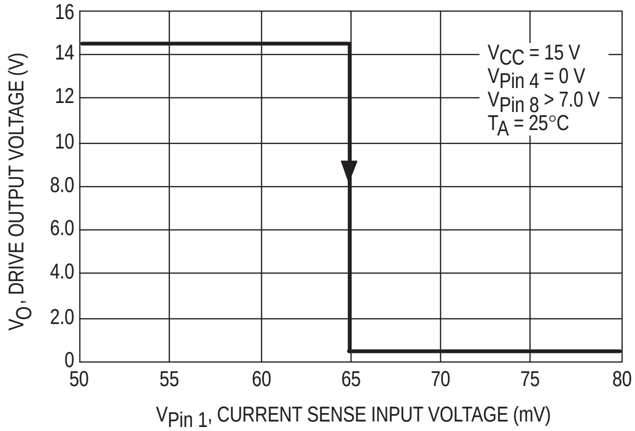


Figure 10. Fault Output Voltage versus Current Sense Input Voltage

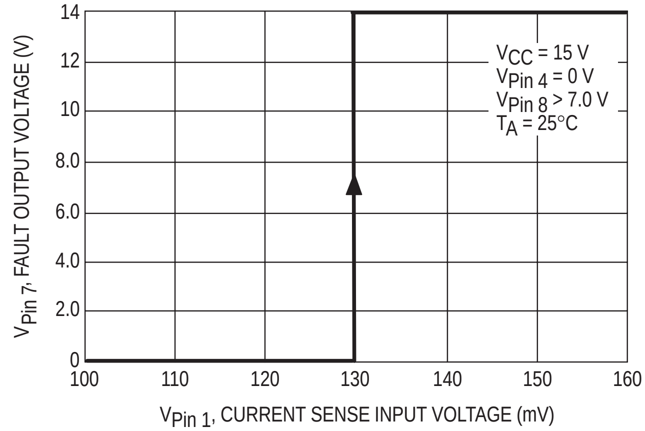


Figure 11. Overcurrent Protection Threshold Voltage versus Temperature

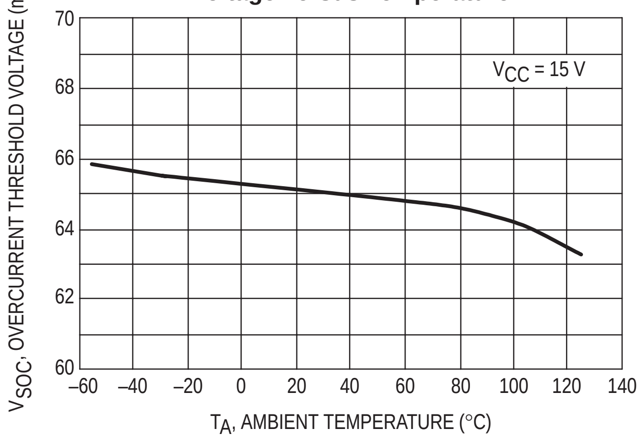


Figure 12. Overcurrent Protection Threshold Voltage versus Supply Voltage

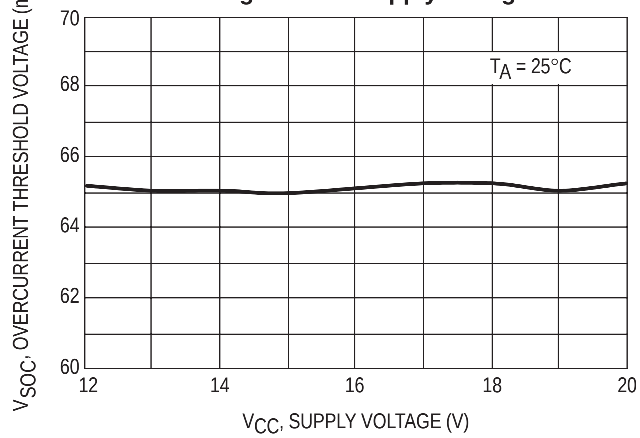


Figure 13. Short Circuit Comparator Threshold Voltage versus Temperature

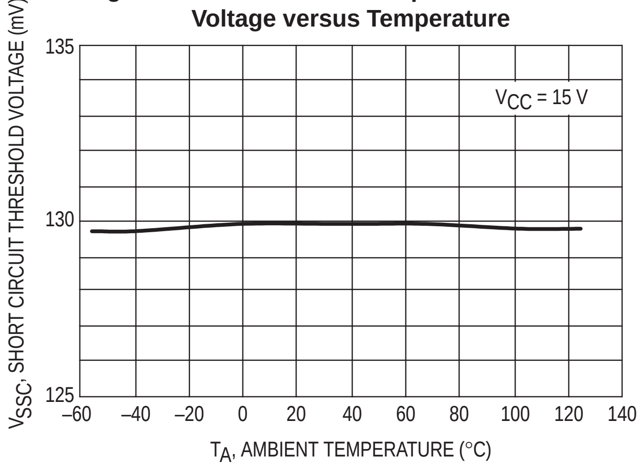


Figure 14. Short Circuit Comparator Threshold Voltage versus Supply Voltage

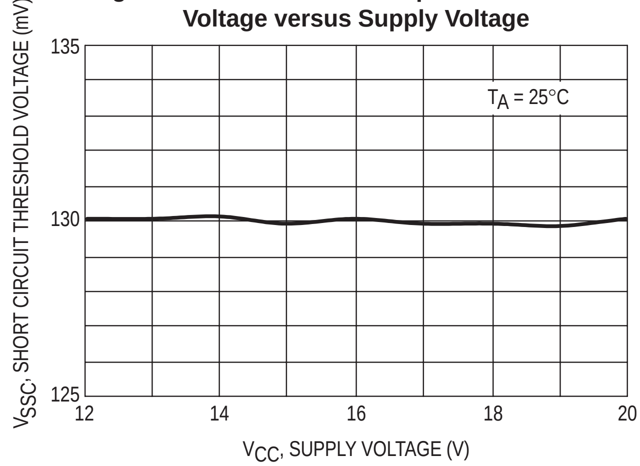


Figure 15. Current Sense Input Current versus Voltage

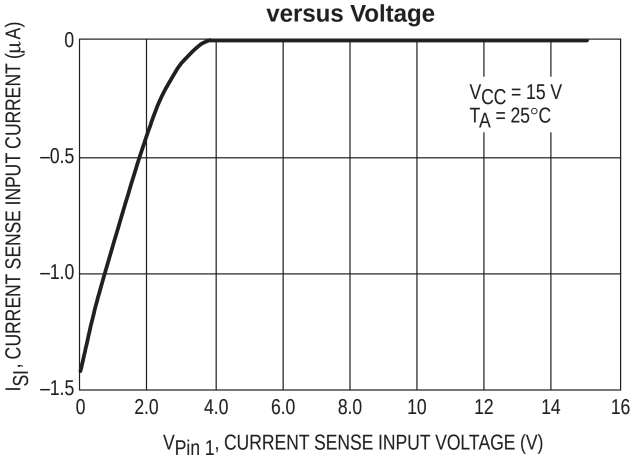


Figure 16. Drive Output Voltage versus Fault Blanking/Desaturation Input Voltage

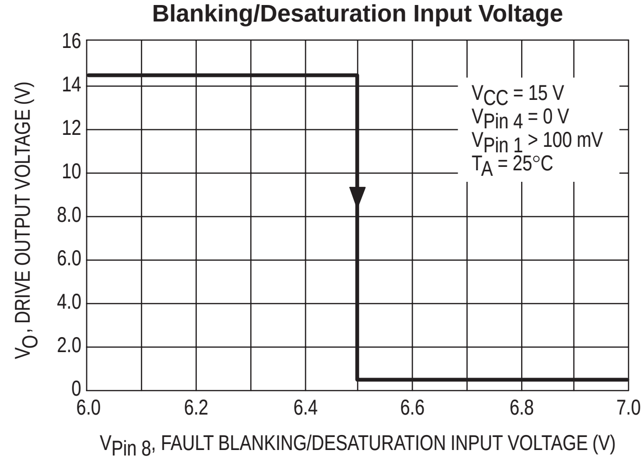


Figure 17. Fault Blanking/Desaturation Comparator Threshold Voltage versus Temperature

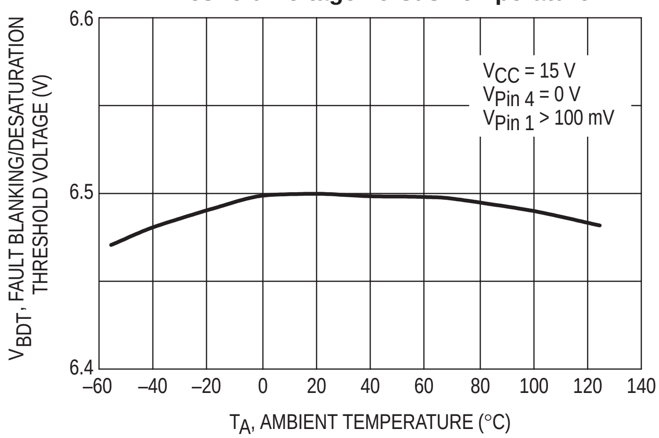


Figure 18. Fault Blanking/Desaturation Comparator Threshold Voltage versus Supply Voltage

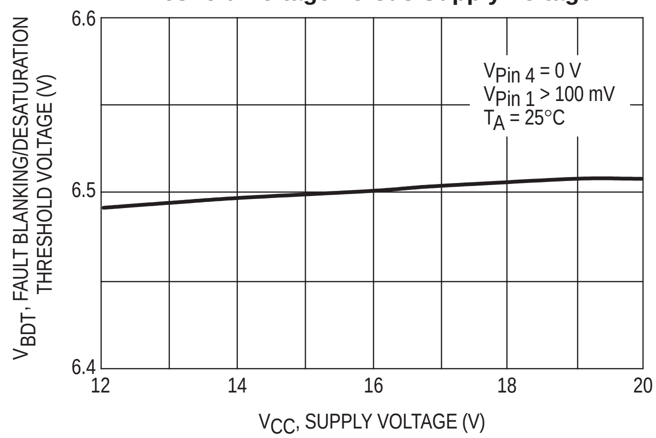


Figure 19. Fault Blanking/Desaturation Current Source versus Temperature

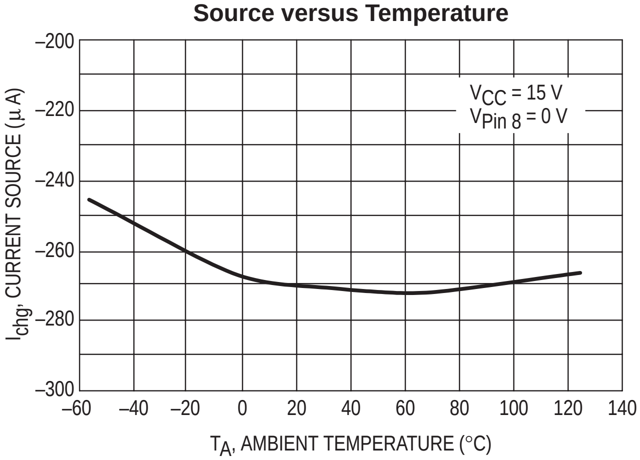


Figure 20. Fault Blanking/Desaturation Current Source versus Supply Voltage

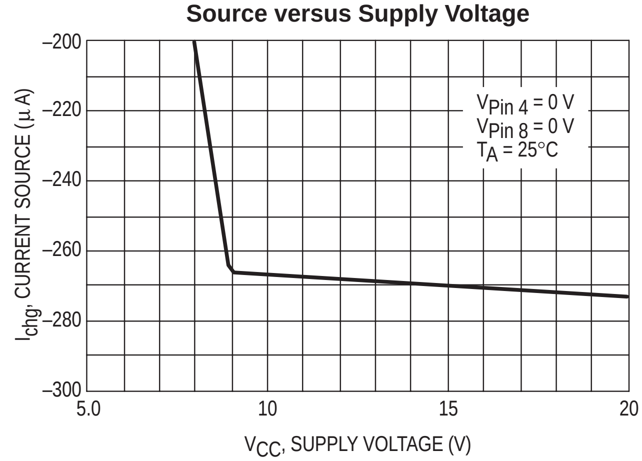


Figure 21. Fault Blanking/Desaturation Current Source versus Input Voltage

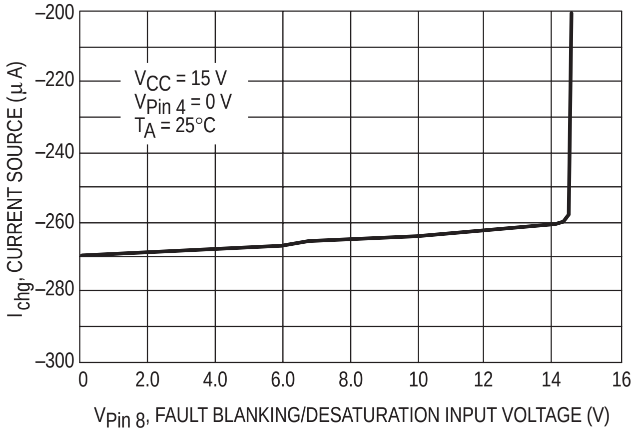


Figure 22. Fault Blanking/Desaturation Discharge Current versus Input Voltage

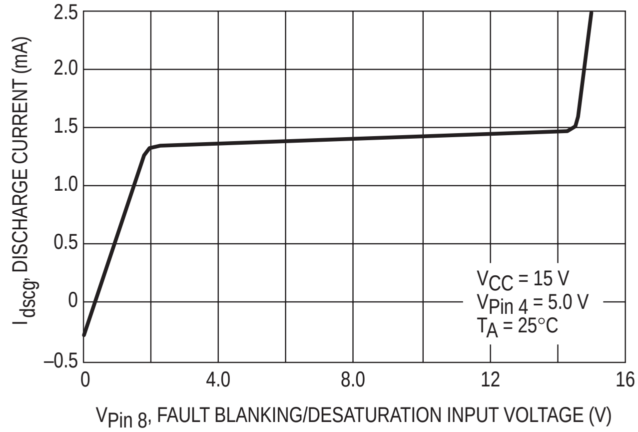


Figure 23. Fault Output Low State Voltage versus Sink Current

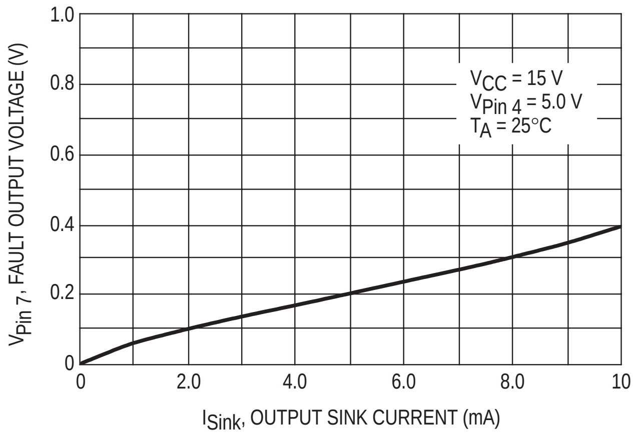


Figure 24. Fault Output High State Voltage versus Source Current

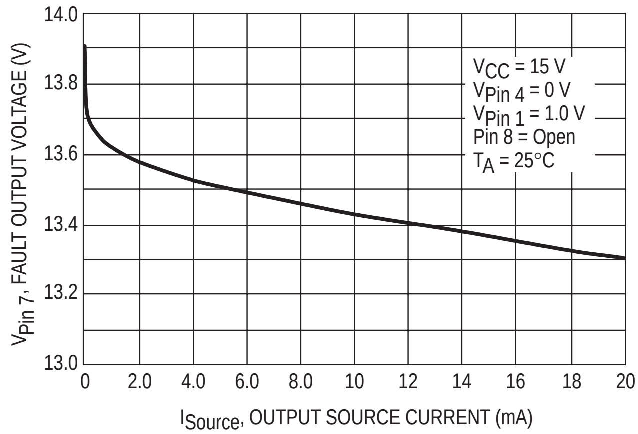


Figure 25. Drive Output Voltage versus Supply Voltage

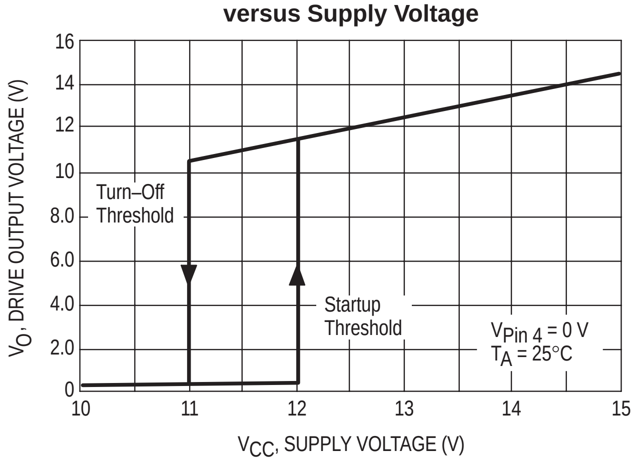


Figure 26. UVLO Thresholds versus Temperature

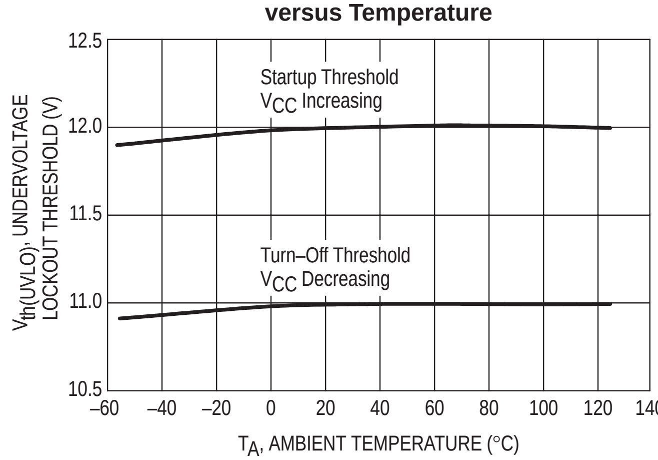


Figure 27. Supply Current versus Supply Voltage

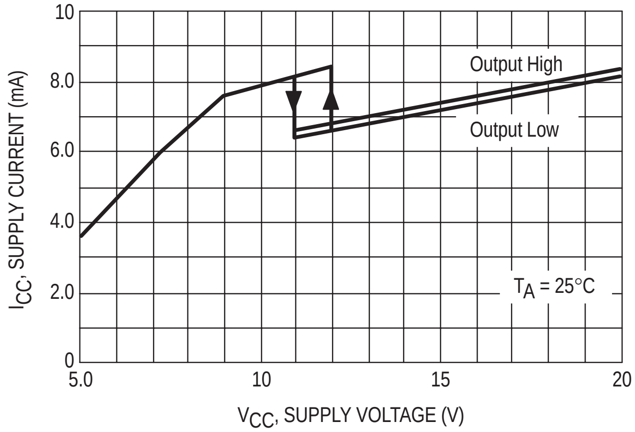


Figure 28. Supply Current versus Temperature

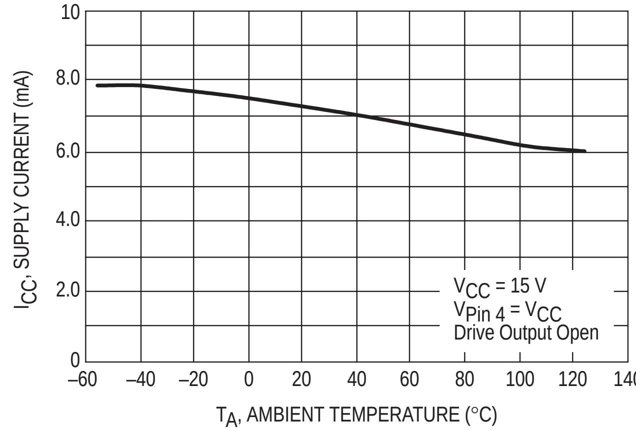
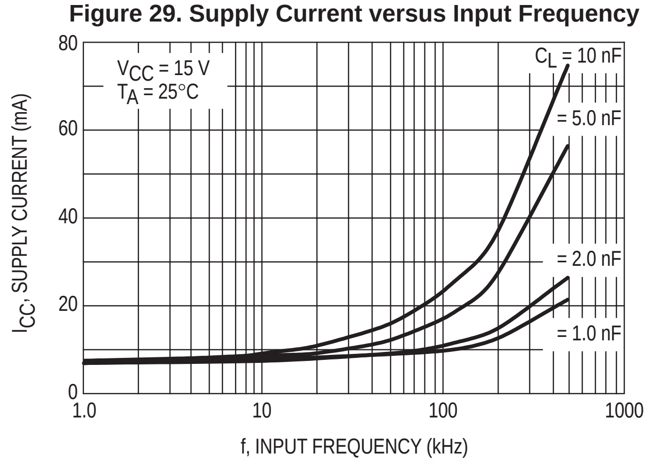


Figure 29. Supply Current versus Input Frequency



OPERATING DESCRIPTION

GATE DRIVE

Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. The switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn–on, turn–off and off–state impedance. A single resistor may be used to control both turn–on and turn–off as shown in Figure 30. However, the resistor value selected must be a compromise in turn–on abruptness and turn–off losses. Using a single resistor is normally suitable only for very low frequency PWM. An optimized gate drive output stage is shown in Figure 31. This circuit allows turn–on and turn–off to be optimized separately. The turn–on resistor, R_{on}, provides control over the IGBT turn–on speed. In motor control circuits, the resistor sets the turn–on di/dt that controls how fast the free–wheel diode is cleared. The interaction of the IGBT and free–wheeling diode determines the turn–on dv/dt. Excessive turn–on dv/dt is a common problem in half–bridge circuits. The turn–off resistor, R_{off}, controls the turn–off speed and ensures that the IGBT remains off under commutation stresses. Turn–off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn–off losses. This is particularly true for fast IGBTs. It is also possible to turn–off an IGBT too fast. Excessive turn–off speed will result in large overshoot voltages. Normally, the turn–off resistor is a small fraction of the turn–on resistor.

The MC33153 contains a bipolar totem pole output stage that is capable of sourcing 1.0 amp and sinking 2.0 amps peak. This output also contains a pull down resistor to ensure that the IGBT is off whenever there is insufficient V_{CC} to the MC33153.

In a PWM inverter, IGBTs are used in a half–bridge configuration. Thus, at least one device is always off. While the IGBT is in the off–state, it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on, clearing the upper diode, the turn–on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot–through currents, it is necessary to provide a low sink impedance to the device that is in the off–state. In most applications the turn–off resistor can be made small enough to hold off the device that is under commutation without causing excessively fast turn–off speeds.

Figure 30. Using a Single Gate Resistor

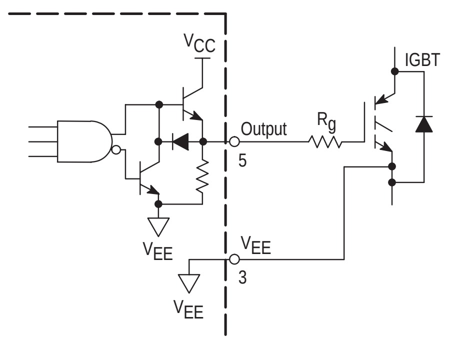
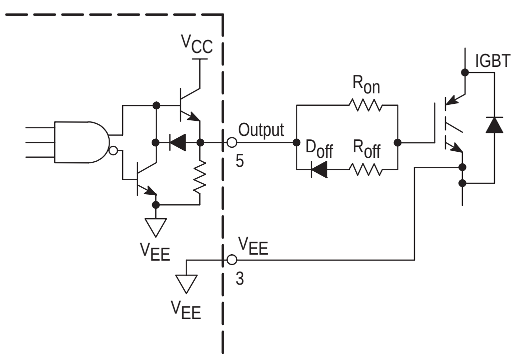


Figure 31. Using Separate Resistors for Turn–On and Turn–Off



A negative bias voltage can be used to drive the IGBT into the off–state. This is a practice carried over from bipolar Darlington drives and is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot–through. The MC33153 has separate pins for V_{EE} and Kelvin Ground. This permits operation using a +15/–5.0 V supply.

INTERFACING WITH OPTOISOLATORS

Isolated Input

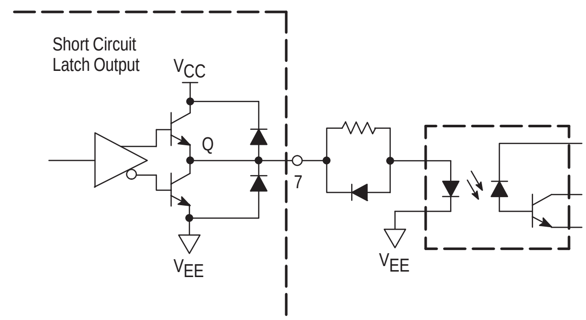
The MC33153 may be used with an optically isolated input. The optoisolator can be used to provide level shifting, and if desired, isolation from ac line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett Packard HCPL4053. The IGBT gate turn–on resistor should be set large enough to ensure that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL4053 has an active low open–collector output. Thus, when the LED is on, the output will be low. The MC33153 has an inverting input pin to interface directly with an optoisolator using a pull up resistor. The input may also be interfaced directly to 5.0 V CMOS logic or a microcontroller.

Optoisolator Output Fault

The MC33153 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again, a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on, and provides a low impedance path when off. An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 32.

Figure 32. Output Fault Optoisolator



UNDERVOLTAGE LOCKOUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to achieve the rated on–voltage. At gate voltages below 13 V, the on–voltage increases dramatically, especially at higher currents. At very low gate voltages, below 10 V, the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33153 will typically start up at about 12 V. The UVLO circuit has about 1.0 V of hysteresis and will disable the output if the supply voltage falls below about 11 V.

PROTECTION CIRCUITRY

Desaturation Protection

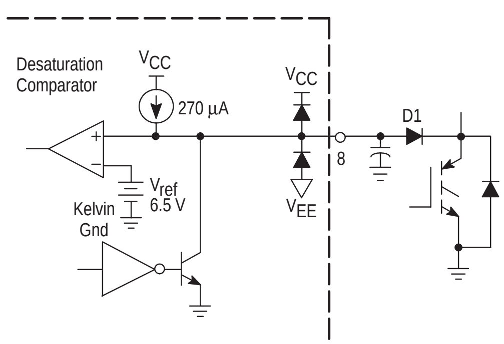
Bipolar Power circuits have commonly used what is known as "Desaturation Detection". This involves monitoring the collector voltage and turning off the device if this voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven, the device is in saturation. When the collector current rises above the knee, the device pulls out of saturation. The maximum current the device will conduct in the linear region is a function of the base current and the dc current gain (h_{FE}) of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However, the output current is a function of gate voltage instead of current. The maximum current depends on the gate voltage and the device type. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device. Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33153 has a Fault Blanking/Desaturation Comparator which senses the collector voltage and provides an output indicating when the device is not fully saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is "on" and saturated, D1 will pull down the voltage on the Fault Blanking/Desaturation Input. When the IGBT pulls out of saturation or is "off", the current source will pull up the input and trip the comparator. The comparator threshold is 6.5 V, allowing a maximum on–voltage of about 5.8 V.

A fault exists when the gate input is high and V_{CE} is greater than the maximum allowable $V_{CE(sat)}$. The output of the Desaturation Comparator is ANDed with the gate input signal and fed into the Short Circuit and Overcurrent Latches. The Overcurrent Latch will turn–off the IGBT for the remainder of the cycle when a fault is detected. When input goes high, both latches are reset. The reference voltage is tied to the Kelvin Ground instead of the V_{EE} to make the threshold independent of negative gate bias. Note that for proper operation of the Desaturation Comparator and the Fault Output, the Current Sense Input must be biased above the Overcurrent and Short Circuit Comparator thresholds. This can be accomplished by connecting Pin 1 to V_{CC}.

Figure 33. Desaturation Detection



The MC33153 also features a programmable fault blanking time. During turn–on, the IGBT must clear the opposing free–wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has been cleared, the voltage will come down quickly to the $V_{CE(sat)}$ of the device. Following turn–on, there is normally considerable ringing on the collector due to the C_{OSS} capacitance of the IGBTs and the parasitic wiring inductance. The fault signal from the Desaturation Comparator must be blanked sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn "off", allowing the internal current source to charge the blanking capacitor. The time required for the blanking capacitor to charge up from the on–voltage of the internal NPN transistor to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $V_{CE(sat)}$ level of the IGBT to the trip voltage of the comparator. Fault blanking can be disabled by leaving Pin 8 unconnected.

Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs. This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability. Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear with respect to the collector current. Because IGBTs have a very low incremental on–resistance, sense IGBTs behave much like low–on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV.

The sense IGBT approach requires fault blanking to prevent false tripping during turn–on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror output normally produces large transient voltages during both turn–on and turn–off due to the collector to mirror capacitance. With non–sensing types of IGBTs, a low resistance current shunt (5.0 to 50 mΩ) can be used to sense the emitter current. When the output is an actual short circuit, the inductance will be very low. Since the blanking circuit provides a fixed minimum on–time, the peak current under a short circuit can be very high. A short circuit discern function is implemented by the second comparator which has a higher trip voltage. The short circuit signal is latched and appears at the Fault Output. When a short circuit is detected, the IGBT should be turned–off for several milliseconds allowing it to cool down before it is turned back on. The sense circuit is very similar to the desaturation circuit. It is possible to build a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

APPLICATION INFORMATION

Figure 34 shows a basic IGBT driver application. When driven from an optoisolator, an input pull up resistor is required. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used for a floating supply. If the protection features are not required, then both the Fault Blanking/Desaturation and Current Sense Inputs should both be connected to the Kelvin Ground (Pin 2). When used with a single supply, the Kelvin Ground and V_{EE} pins should be connected together. Separate gate resistors are recommended to optimize the turn–on and turn–off drive.

Figure 34. Basic Application

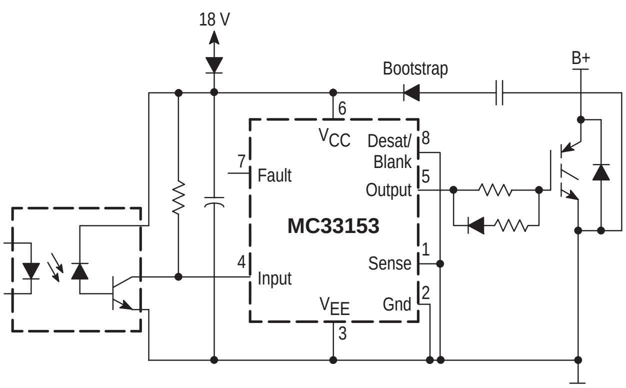
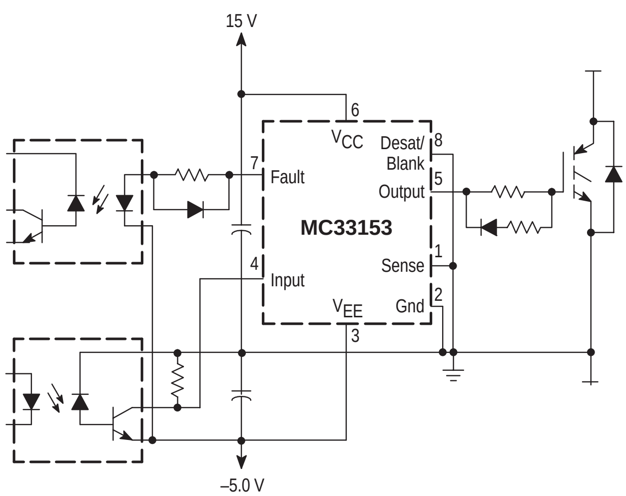


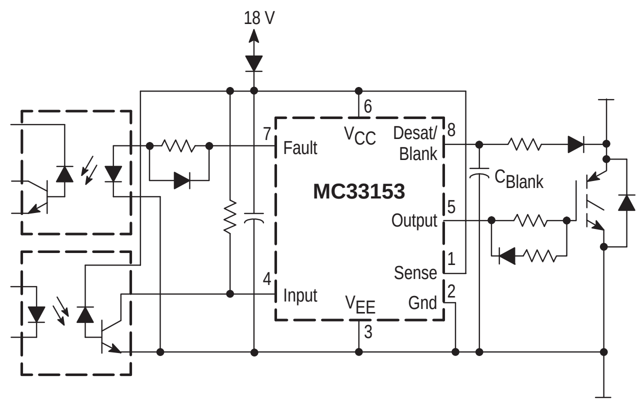
Figure 35. Dual Supply Application



When used in a dual supply application as in Figure 35, the Kelvin Ground should be connected to the emitter of the IGBT. If the protection features are not used, then both the Fault Blanking/Desaturation and the Current Sense Inputs should be connected to Ground. The input optoisolator should always be referenced to V_{EE}.

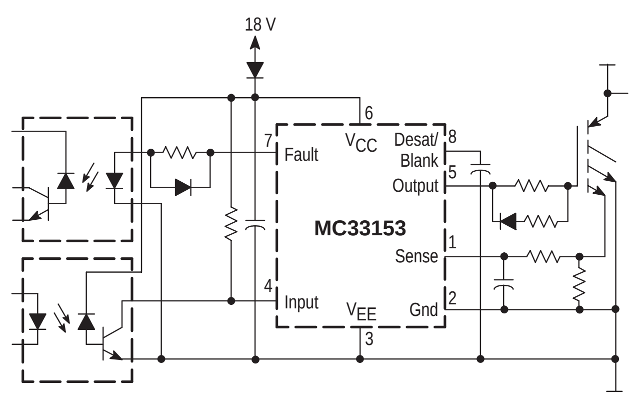
If desaturation protection is desired, a high voltage diode is connected to the Fault Blanking/Desaturation pin. The blanking capacitor should be connected from the Desaturation pin to the V_{EE} pin. If a dual supply is used, the blanking capacitor should be connected to the Kelvin Ground. The Current Sense Input should be tied high because the two comparator outputs are ANDed together. Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free–wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode can be used to protect the IC from reverse voltage transients.

Figure 36. Desaturation Application



When using sense IGBTs or a sense resistor, the sense voltage is applied to the Current Sense Input. The sense trip voltages are referenced to the Kelvin Ground pin. The sense voltage is very small, typically about 65 mV, and sensitive to noise. Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to V_{EE}. The stray capacitance on the blanking pin provides a very small level of blanking if left open. The blanking pin should not be grounded when using current sensing, that would disable the sense. The blanking pin should never be tied high, that would short out the clamp transistor.

Figure 37. Sense IGBT Application



MOTOROLA

MC33154

Advance Information

Single IGBT High Current Gate Driver

SINGLE IGBT HIGH CURRENT GATE DRIVER

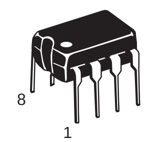
SEMICONDUCTOR TECHNICAL DATA

The MC33154 is specifically designed as an IGBT driver for high powered applications including ac induction motor control, brushless dc motor control, and uninterruptable power supplies. This device also offers a cost effective solution for driving power MOSFETS and Bipolar transistors.

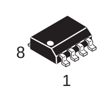
Device protections include the choice of desaturation or overcurrent sensing and an undervoltage lockout to provide assurance of proper gate drive voltage.

These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 4.0 A Source –2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBT's
- Current Source for Blanking Timing
- Protection Against Over–Current and Short Circuit
- Under–Voltage Lockout Optimized for IGBT's
- Negative Gate Drive Capability

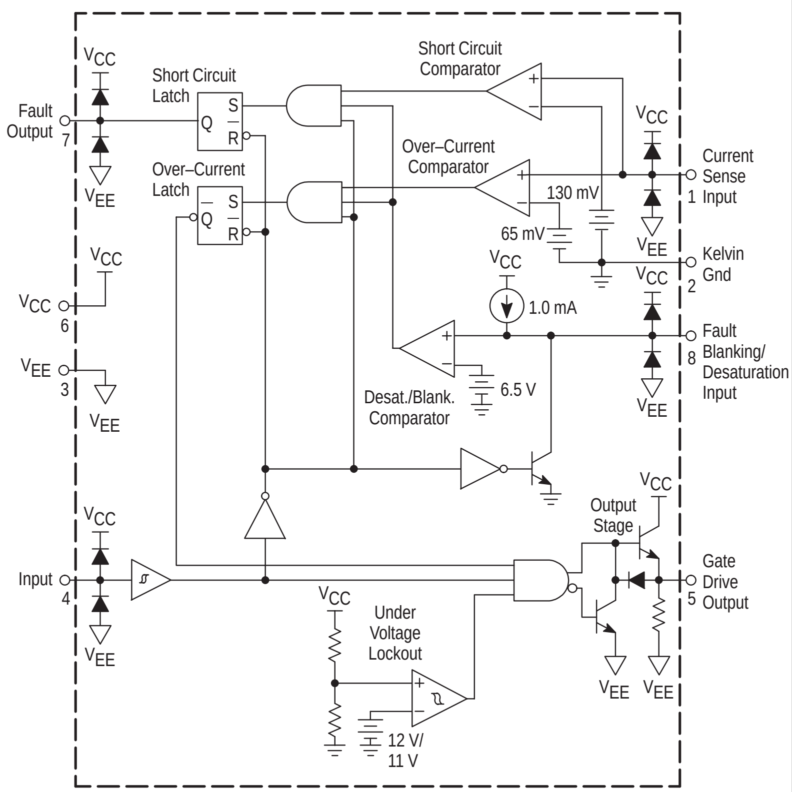


P SUFFIX
PLASTIC PACKAGE
CASE 626

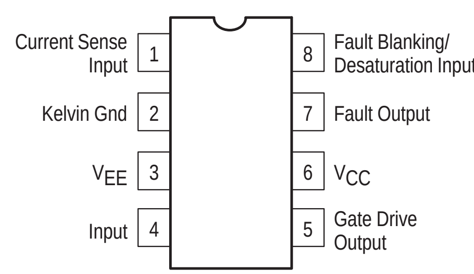


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC33154D	T_A = –40° to +85°C	Plastic SO–8
MC33154P	T_A = –40° to +85°C	Plastic DIP–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage V_{CC} to V_{EE}; $V_{EE} \leq$ KGND $\leq V_{CC}$ Kelvin Ground to V_{EE} (Note 1)	 $V_{CC} - V_{EE}$ KGnd – V_{EE}	 20 20	V
Input	V_{in}	V_{EE} –0.3 to V_{CC}	V
Current Sense Input	V_{CS}	–0.3 to V_{CC}	V
Fault Blanking/Desaturation Input	V_{BD}	–0.3 to V_{CC}	V
Gate Drive Output Source Current Sink Current Diode Clamp Current	I_O	 4.0 2.0 1.0	A
Fault Output Source Current Sink Current	I_{FO}	 25 10	mA
Power Dissipation and Thermal Characteristics D Suffix SO–8 Package, Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air P Suffix DIP–8 Package, Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS
(V_{CC} = 20 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 1] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Input Threshold Voltage High State (Logic 1) @ T_A = 25°C @ T_A = –40 to +85°C Low State (Logic 0)	 V_{IH} V_{IL}	 4.5	 9.0 7.0	 10.5 11.6 –	V
Input Current — High State (V_{IH} = 10.5 V) — Low State (V_{IL} = 4.5 V)	I_{IH} I_{IL}	– –	100 50	500 100	µA
GATE DRIVE OUTPUT					
Output Voltage Low State (I_{Sink} = 1.0 A) High State (I_{Source} = 2.0 A)	 V_{OL} V_{OH}	 – 17	 2.0 18	 2.5 –	V
Output Pull–Down Resistor	R_{PD}	–	100	200	kΩ
FAULT OUTPUT					
Output Voltage Low State (I_{Sink} = 5.0 mA) High State (I_{Source} = 20 mA)	 V_{FL} V_{FH}	 – 17	 0.2 18.3	 1.0 –	V
SWITCHING CHARACTERISTICS					
Propagation Delay (50% Input to 50% Output C_L = 15 nF) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	 $t_{PLH\ (in/out)}$ $t_{PHL\ (in/out)}$	 – –	 200 120	 300 300	ns
Drive Output Rise Time (10% to 90%) C_L = 15 nF	t_r	–	80	200	ns
Drive Output Fall Time (90% to 10%) C_L = 15 nF	t_f	–	80	200	ns
Propagation Delay Current Sense Input to Drive Output	 $t_{P(OC)}$	 –	 0.4	 1.0	µs

NOTE: 1. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33154 T_{high} = +85°C for MC33154

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 1] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Fault Blanking/Desaturation Input to Drive Output	$t_{P(FLT)}$	–	0.4	1.0	
UVLO					
Start–up Voltage	$V_{CC\ start}$	11.3	12	12.6	V
Disable Voltage	$V_{CC\ dis}$	10.4	11	11.7	V
COMPARATORS					
Over Current Trip Voltage (V_{Pin8} > 7.0 V)	V_{SOC}	50	65	80	mV
Short Current Trip Voltage (V_{Pin8} > 7.0 V)	V_{SSC}	100	130	160	mV
Desaturation Threshold (V_{Pin1} > 100 mV)	$V_{th(FLT)}$	6.0	6.5	7.0	V
Sense Input Current (V_{SI} = 0 V)	I_{SI}	–	–1.4	–10	μA
FAULT BLANKING/DESATURATION INPUT					
Current Source (V_{Pin8} = 0 V, V_{Pin4} ≥ 10.5 V)	I_{chg}	0.8	1.0	1.2	mA
Discharge Current (V_{Pin8} = 15 V, V_{Pin4} = 0 V)	I_{dschg}	0.8	2.5	–	mA
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby ($V_{Pin\ 4}$ = 0 V, Output Open)		–	9.0	14	
Operating (C_L = 15 nF, f_{in} = 20 kHz)		–	15	25	

NOTE: 1. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33154 T_{high} = +85°C for MC33154

Figure 1. Input Current versus Logic Input Voltage

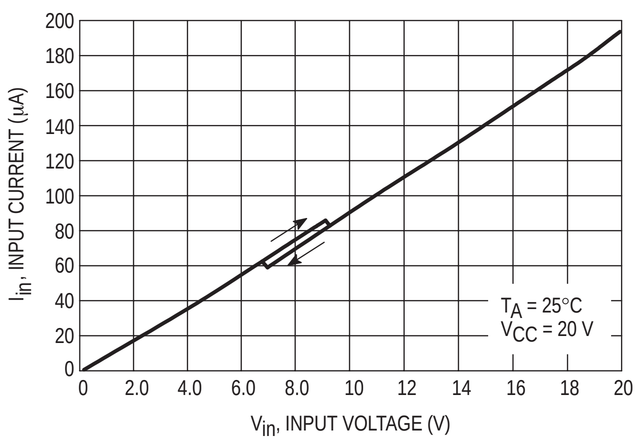


Figure 2. Output Voltage versus Input Voltage

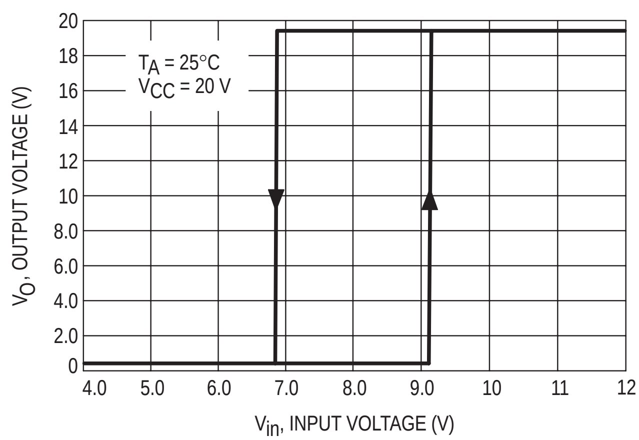


Figure 3. Input Threshold Voltage versus Supply Voltage

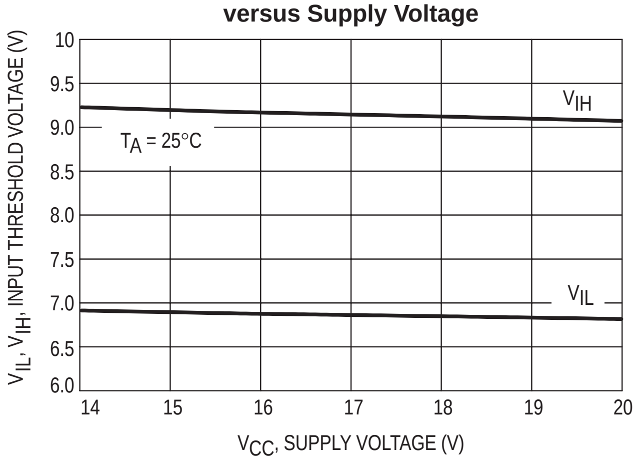


Figure 4. Input Thresholds versus Temperature

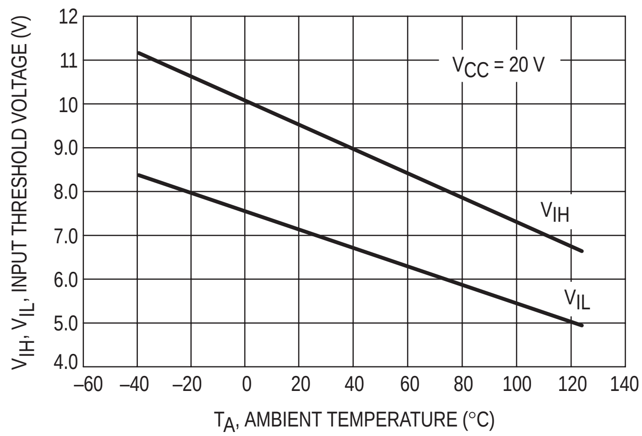


Figure 5. Drive Output Low State Voltage versus Temperature

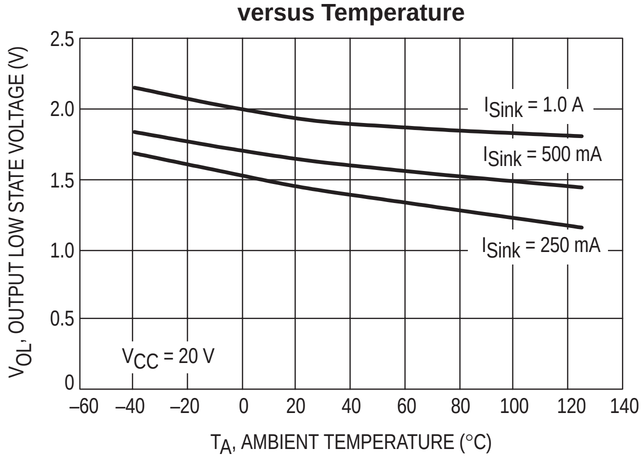


Figure 6. Drive Output Low State Voltage versus Sink Current

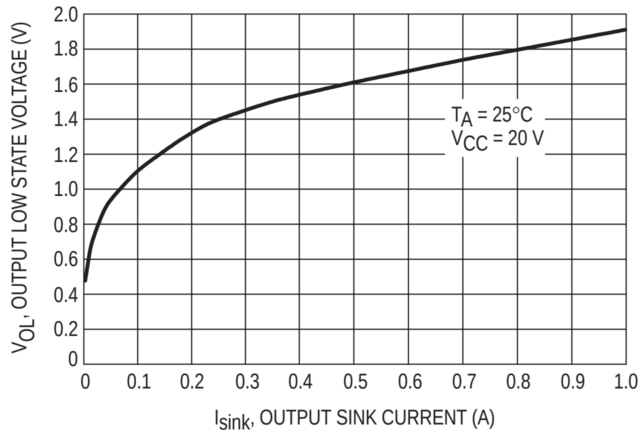


Figure 7. Drive Output High State Voltage versus Temperature

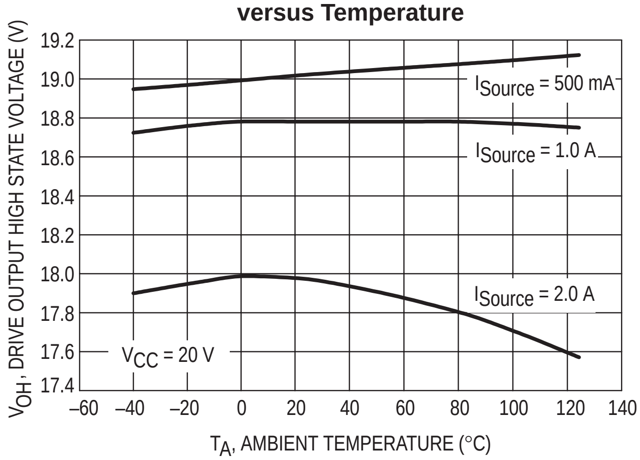


Figure 8. Output Saturation High versus Output Current

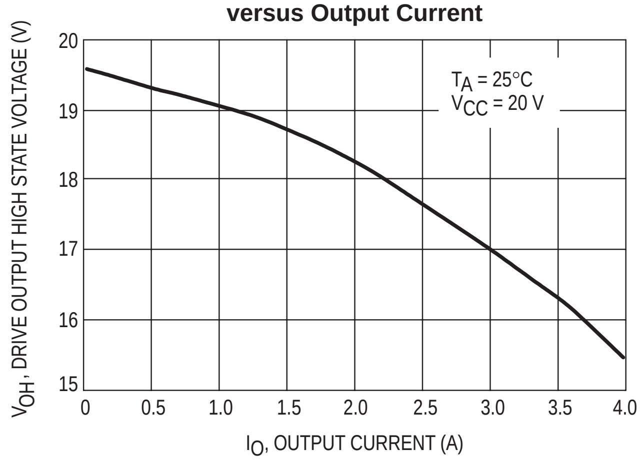


Figure 9. Drive Output Voltage versus Current Sense Input Voltage

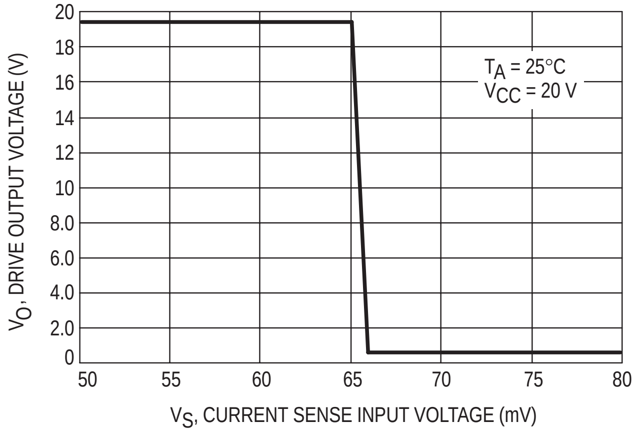


Figure 10. Fault Output Voltage versus Current Sense Input Voltage

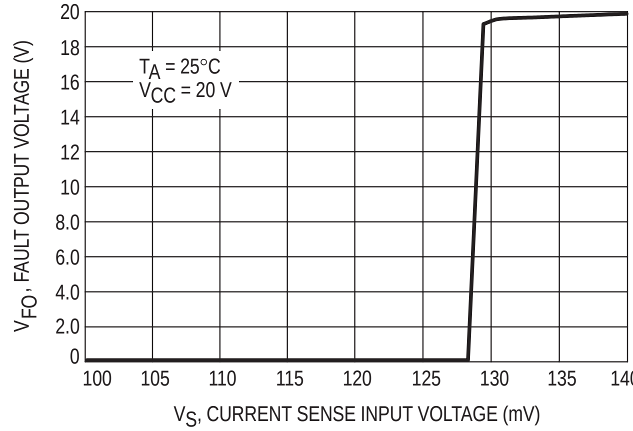


Figure 11. Overcurrent Threshold Voltage versus Temperature

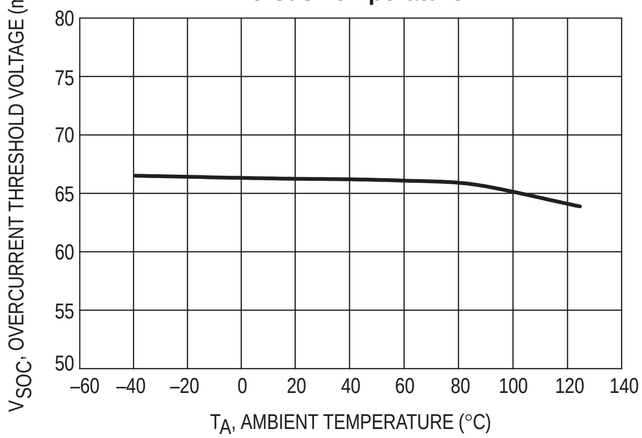


Figure 12. Short Circuit Threshold Voltage versus Temperature

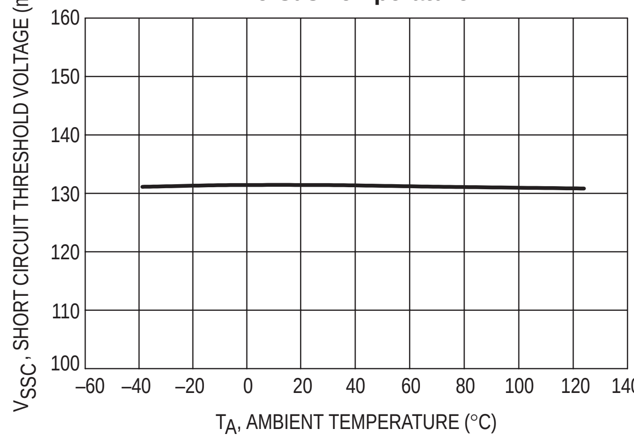


Figure 13. Sense Input Current versus Sense Voltage

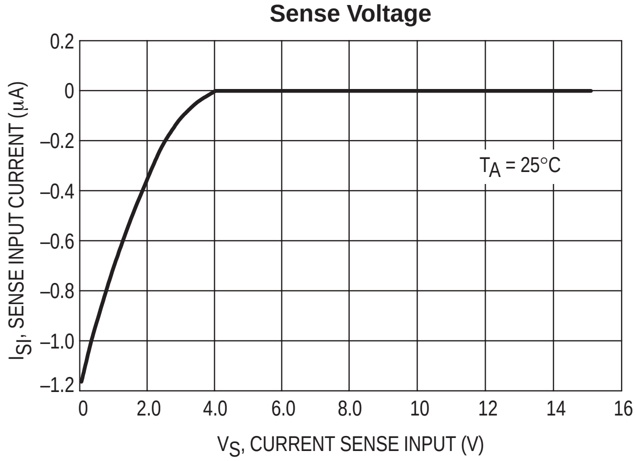


Figure 14. Output Voltage versus Blanking/Desaturation Voltage

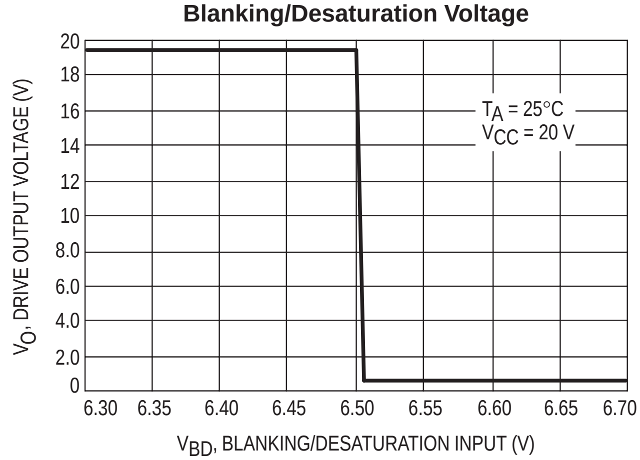


Figure 15. Desaturation Threshold versus Temperature

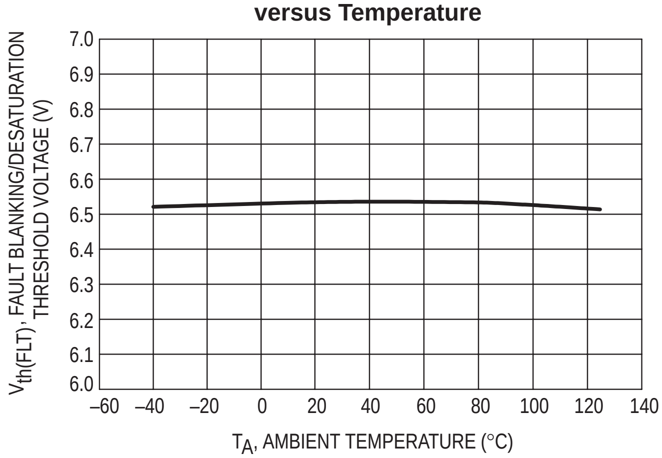


Figure 16. Blanking/Desaturation Threshold versus Supply Voltage

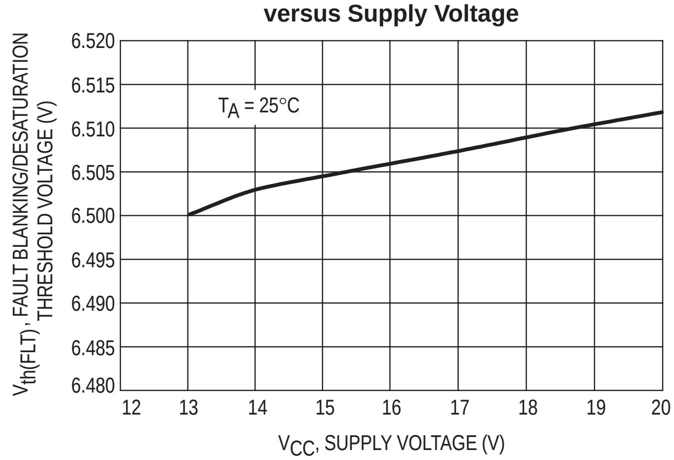


Figure 17. Blanking Current Source versus Temperature

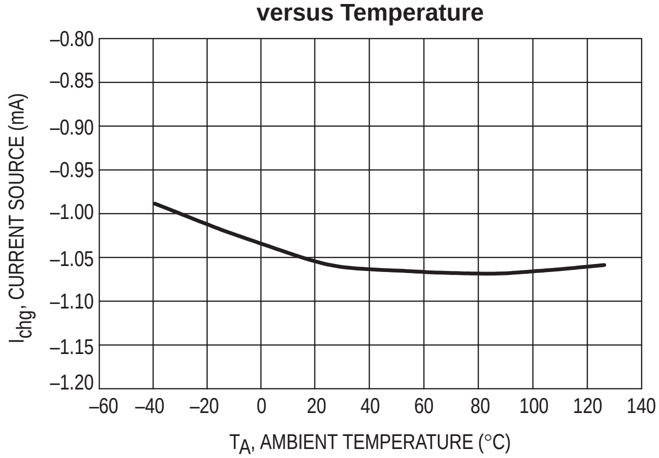


Figure 18. Blanking Current versus Supply Voltage

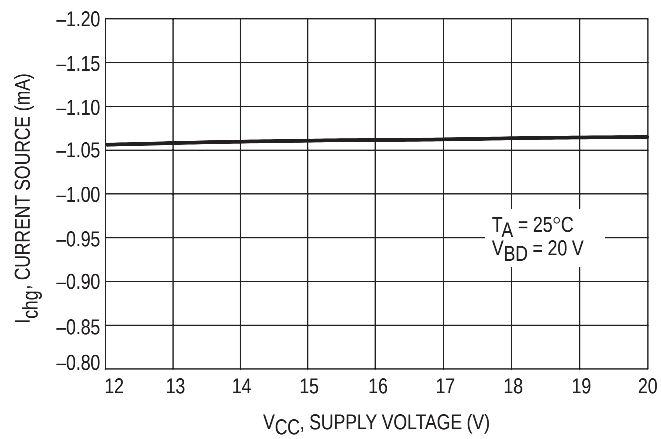


Figure 19. Blanking Current versus Blanking/Desaturation Voltage

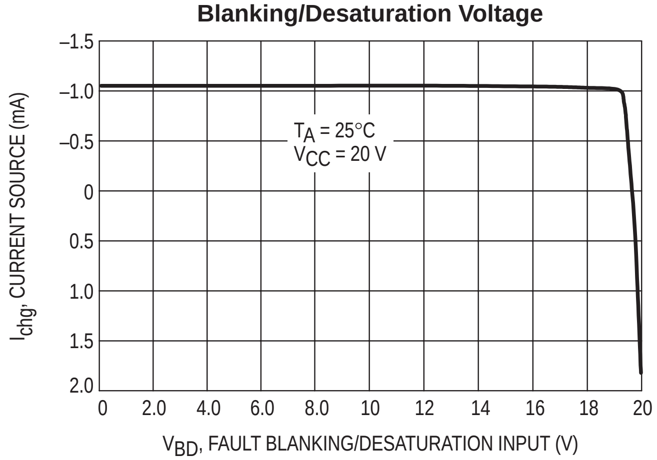


Figure 20. Blanking Discharge Current versus Blanking/Desaturation Voltage

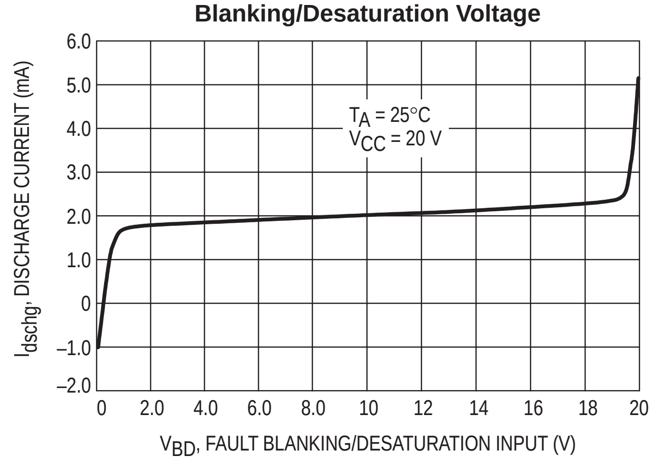


Figure 21. Fault Output Voltage Low versus Fault Output Current

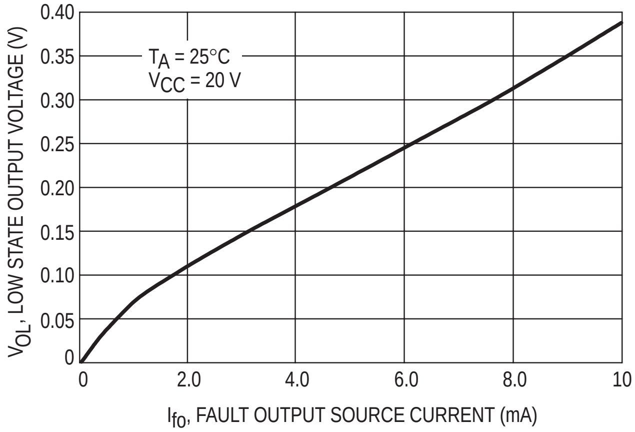


Figure 22. Fault Output Voltage High versus Fault Output Current

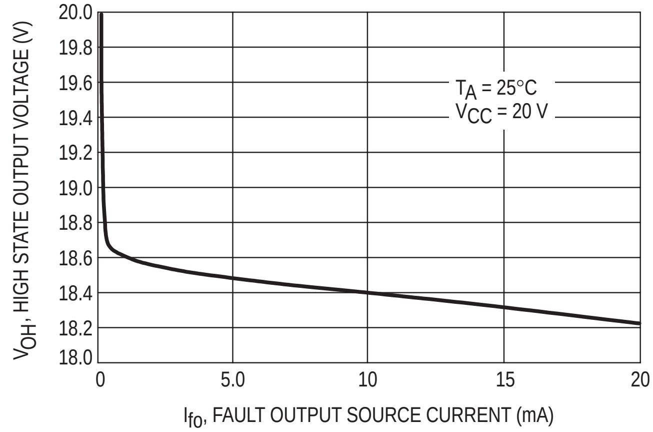


Figure 23. UVLO Start Threshold versus Temperature

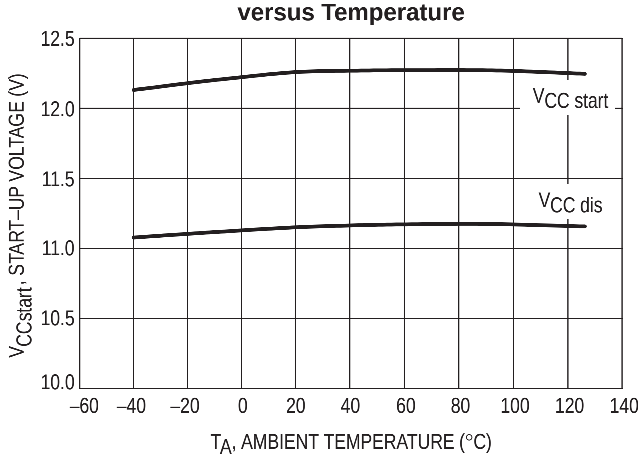


Figure 24. Standby Supply Current versus Supply Voltage

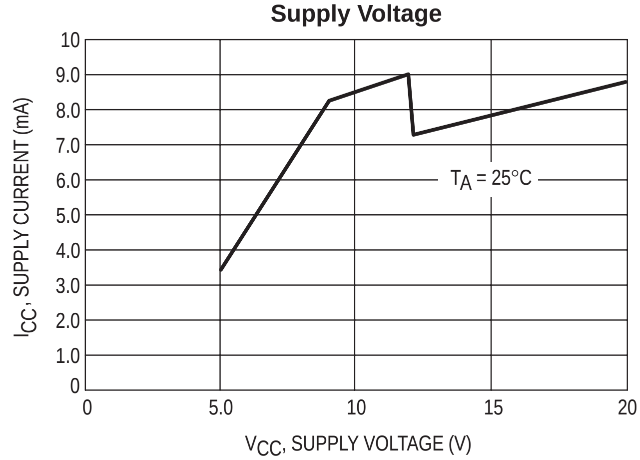
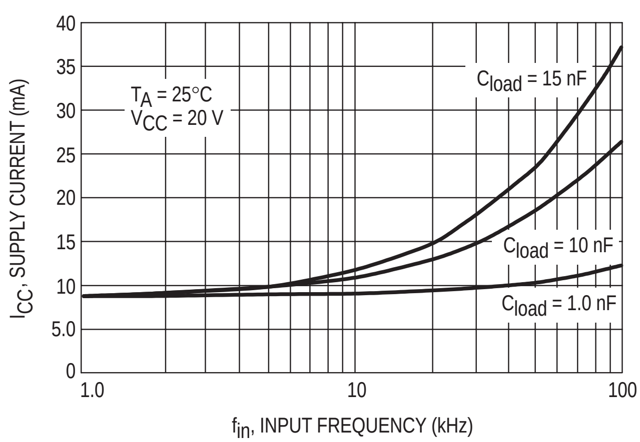


Figure 25. Supply Current versus Input Frequency



OPERATING DESCRIPTION

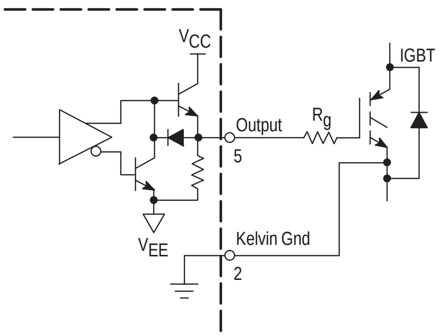
GATE DRIVE

Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. Switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn–on, turn–off, and off–state impedance.

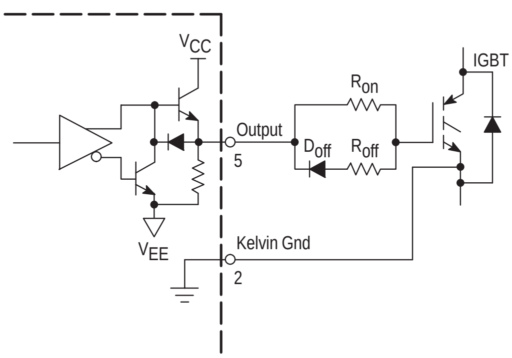
A single resistor may be used to control both turn–on and turn–off and shown in Figure 30. However, the resistor value selected must be a compromise in turn–on abruptness and turn–off losses. Using a single resistor is normally suitable only for very low frequency PWM.

Figure 26. Using a Single Gate Resistor



An optimized gate drive output stage is shown in Figure 31. This circuit allows turn–on and turn–off to be optimized separately.

Figure 27. Using Separate Resistors for Turn–On and Turn–Off



The turn–on resistor R_{on} provides control over the IGBT turn–on speed. In motor control circuits, the resistor sets the turn–on di/dt that controls how fast the free–wheel diode is cleared. The interaction of the IGBT and freewheeling diode determines the turn–on dv/dt.

Excessive turn–on dv/dt is a common problem in half–bridge circuits.

The turn–off resistor R_{off} controls the turn–off speed and ensures that the IGBT remains off under commutation stresses. Turn–off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn–off losses. This is particularly true for fast IGBTs. It is also possible to turn–off an IGBT too fast. Excessive turn–off speed will result in large overshoot voltages. Normally the turn–off resistor is a small fraction of the turn–on resistor.

The MC33154 has a bipolar totem pole output. The output stage is capable of sourcing 4.0 amps and sinking 2.0 amps peak. The output stage also contains a pull down resistor to ensure that the IGBT is off when the gate drive power is not applied.

In a PWM inverter, IGBTs are used in a half–bridge configuration. Thus, at least one device is always off. While the IGBT is in the off–state it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on clearing the upper diode, the turn–on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot–through currents it is necessary to provide a low sink impedance to the device in the off–state. Fortunately, the turn–off resistor can be made small enough to hold off the device under commutation without causing excessively fast turn–off speeds.

Sometimes a negative bias voltage is used in the off–state. This is a practice carried over from bipolar Darlington drives. A negative bias is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot–through. The MC33154 has separate pins for V_{EE} and Kelvin Gnd. This permits operation using a +15/–5 volt supply.

INTERFACING WITH OPTOISOLATORS

Isolated Input

The MC33154 may be used with an optically isolated input. The optoisolator can be used to provide level shifting and if desired, isolation from AC line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett–Packard HCPL0453. The IGBT gate turn–on resistor should be set large enough to ensure that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL0453 has an active low open–collector output. Thus, when the LED is ON, the output will be low. The MC33154 has a non–inverting input pin to interface directly with an optoisolator using a pull up resistor.

Optoisolator Output Fault

The MC33154 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on and provides a low impedance path when off.

An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 32.

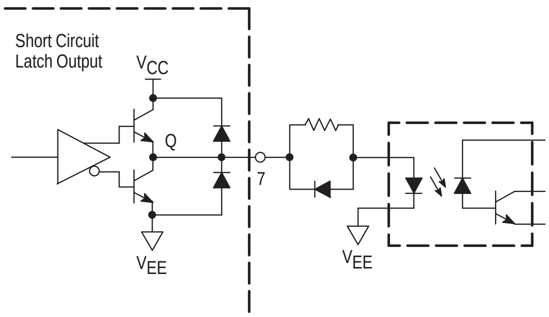


Figure 28. Output Fault Optoisolator

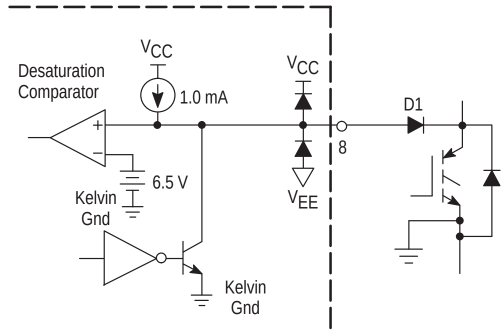


Figure 29. Desaturation Detection Using a Diode

UNDER VOLTAGE LOCK OUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to guarantee device saturation. At gate voltages below 13 V, the "on" state voltage increases dramatically, especially at higher currents. At very lower gate voltages, below 10 V, the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33154 will typically start up at about 12 V. The UVLO circuit has about 1.0 volt of hysteresis. The UVLO will disable the output if the supply voltage falls below about 11 V.

PROTECTION CIRCUITRY

Desaturation Protection

Bipolar Power circuits have commonly used what is known as "Desaturation Detection". This involves monitoring the collector voltage and turning off the device if the collector voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven the device is in saturation. When the collector current rises above the knee, the device pulls out of saturation.

The maximum current the device will conduct in the linear region is a function of the base current and hfe of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However the output current is a function of gate voltage, not current. The maximum current depends on the gate voltage and the device. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device.

Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33154 has a desaturation comparator which senses the collector voltage and provides an output indicating when the device is not full saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is ON and saturated, diode D1 will pull down the voltage on the desaturation input. When the IGBT is OFF or pulls out of saturation, the current source will pull up the voltage on the desaturation input. The voltage reference is set to about 6.5 V. This will allow a maximum ON–voltage of about 5.0 V.

A fault exists when the gate input is high and V_{CE} of the IGBT is greater than the maximum allowable $V_{CE(sat)}$. The output of the desaturation comparator is ANDed with the gate input signal and fed into the Short Circuit (SC) latch. The SC latch will turn–off the IGBT for the remainder of the cycle when a fault is detected. When the input is toggled low, the latch will reset. The reference voltage is tied to the Kelvin Ground instead of the V_{EE} to make the threshold independent of negative gate bias.

The MC33154 also features a programmable turn–on blanking time. During turn–on the IGBT must clear the opposing free wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has been cleared the voltage will come down quickly to the $V_{CE(sat)}$ of the device. Following turn–on there is normally considerable ringing on the collector due to the C_{OSS} of the IGBTs and the parasitic wiring inductance.

The error signal from the desaturation signal must be blanked out sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn–off, and the current source will charge up the blanking capacitor. The time required for blanking capacitor to charge up from the on–voltage of the clamp FET to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $V_{CE(sat)}$ to the trip voltage of the comparator.

Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs.

This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability.

Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear concerning collector current.

Because IGBTs have a very low incremental on–resistance, sense IGBTs behave much like low–on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV.

The sense IGBT approach requires a blanking time to prevent false tripping during turn–on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror normally produces large transient voltages during both turn–on and turn–off due to the collector to mirror capacitance.

A low resistance current shunt may also be used to sense the emitter current. A very low resistance shunt (5.0 mΩ to 50 mΩ) must be used with high current IGBTs. The output voltage of a current shunt is also very low.

When the output is an actual short circuit the inductance will be very low. Since the blanking circuit provides a fixed minimum on–time the peak current under a short circuit may be very high. A short circuit discern function may be implemented using a second comparator with a higher trip voltage.

This circuit can distinguish between an overcurrent and a shorted output condition. Under an actual short circuit the die temperature may get very hot. When a short circuit is detected the transistor should be turned–off for several milliseconds to cool down before the device is turned back on.

The sense circuit is very similar to the Desaturation circuit. The MC33154 uses a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

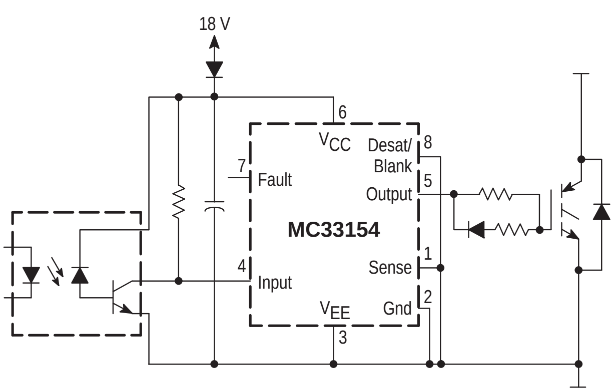
APPLICATION EXAMPLES

The simplest gate drive circuit using the MC33154 is shown in Figure 34. The optoisolator requires a pull up resistor. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used to for a floating supply. If the protection features are not used, then both the desaturation input and the current sense input should be grounded.

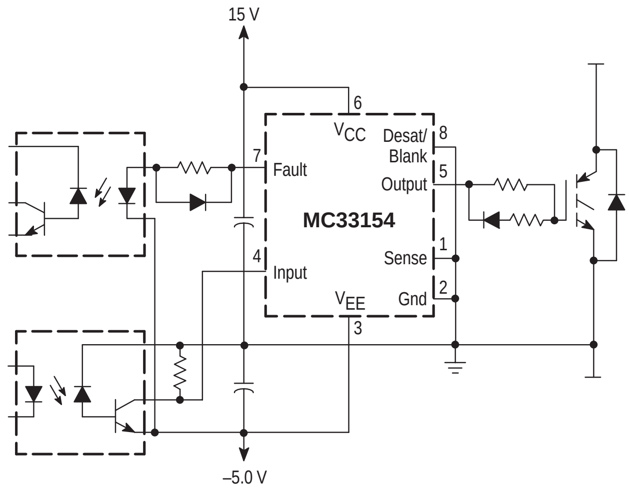
When used with a single supply the Kelvin Gnd and V_{EE} pins should be connected. Separate resistors are recommended for turn–on and turn–off.

Figure 30. Basic Application



When used with a dual supply as shown in Figure 35, the Gnd pin should be Kelvin connected to the emitter of the IGBT. If the protection features are not used, then both the desaturation input and the current sense input should be connected to Gnd. The input optoisolator, however, should be referenced to V_{EE}.

Figure 31. Dual Supply Application

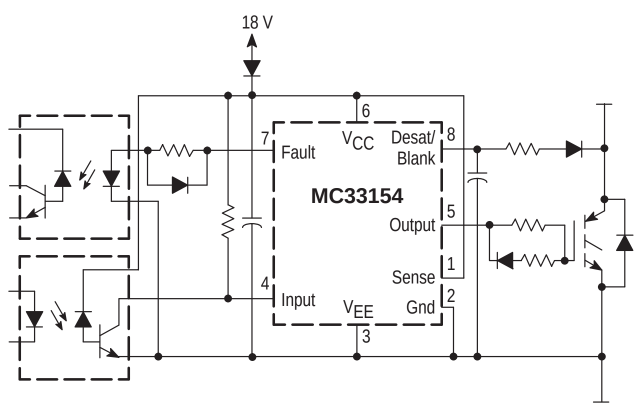


If Desaturation protection is desired as shown in Figure 32, a high voltage diode is connected to the Desaturation/Blanking pin. The blanking capacitor should be connected from the Desaturation pin to the V_{EE} pin. If a dual supply is used the blanking capacitor should be connected to the Kelvin Gnd.

Because desaturation protection is used in this example, the sense input should be tied high. The MC33154 design ANDs the output of the overcurrent comparators with the output of the desaturation comparator, allowing the circuit designer to choose either type of protection.

Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode may be used to protect the IC from reverse voltage transients.

Figure 32. Desaturation Application

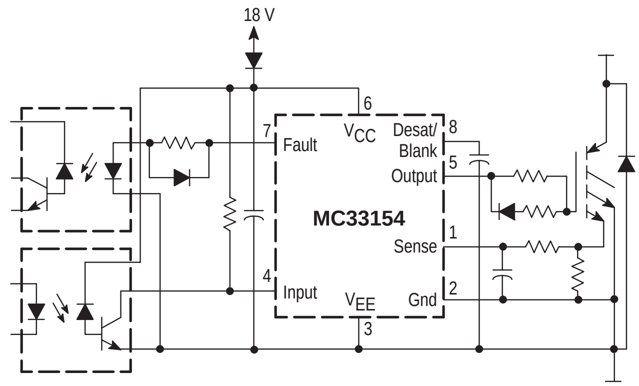


When using sense IGBTs or a sense resistor, as shown in Figure 33, the sense voltage is applied to the current sense input. The sense trip voltages are referenced to the Kelvin Gnd pin. The sense voltage is very small, typically about 65 mV, and sensitive to noise.

Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to V_{EE}. The stray capacitance on the blanking pin provides a very small level of blanking if left open.

The blanking pin should not be grounded when using current sensing. That would disable the overcurrent sense. The blanking pin should never be tied high. That would short out the internal IC clamp transistor.

Figure 33. Sense IGBT Application



Chapter Five

Surface Mount Package Information Tape and Reel Specifications

Table of Contents

INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT–223 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figures 1, 2 and 3.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

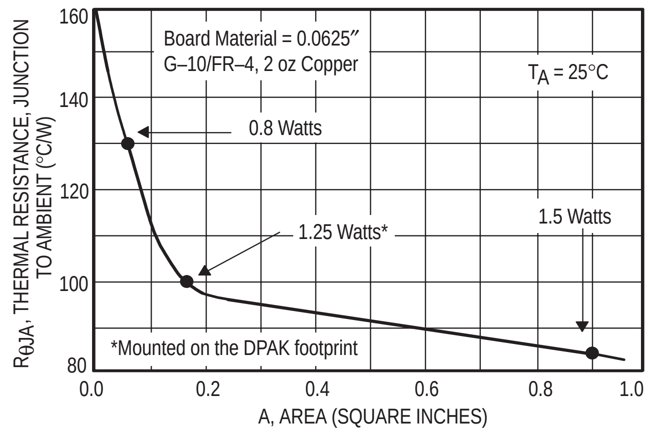


Figure 1. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)

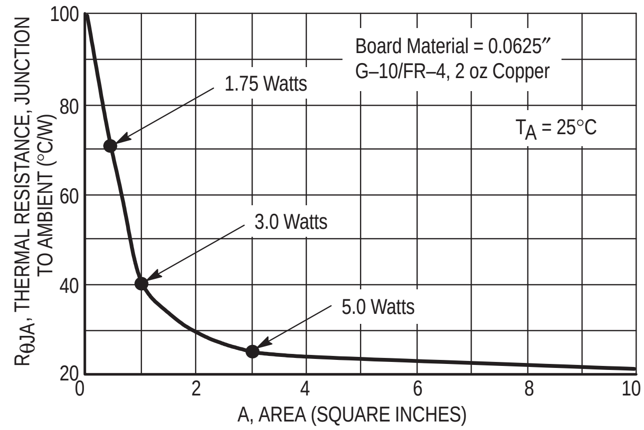


Figure 2. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

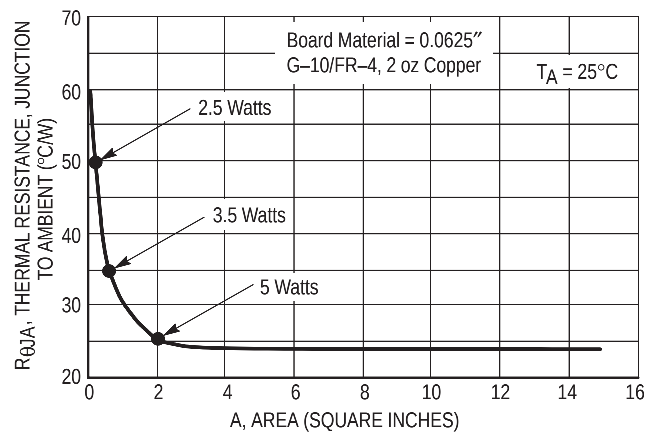


Figure 3. Thermal Resistance versus Drain Pad Area for the D^2PAK Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SOT–223 and SO–8 packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If a 1:1 opening is used to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 4 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

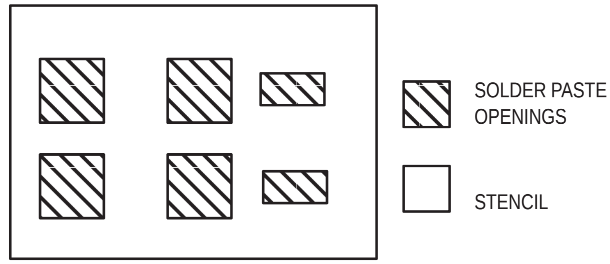


Figure 4. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 5 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

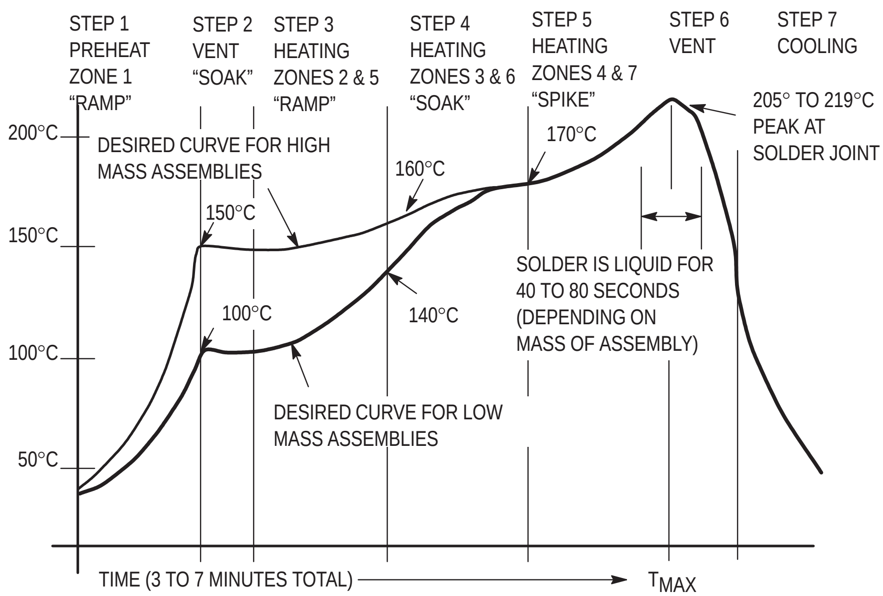
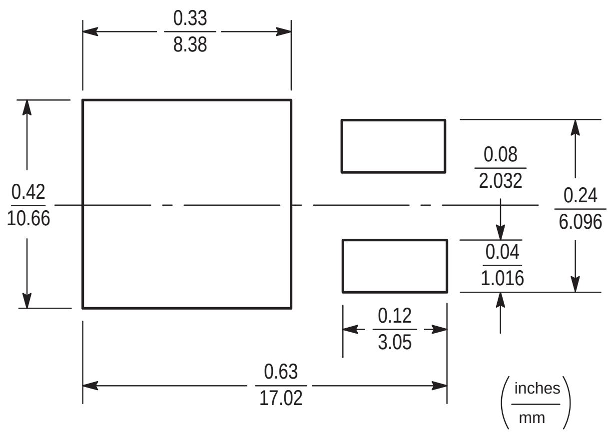
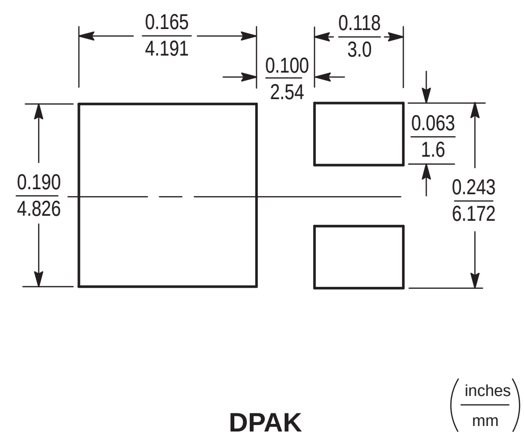


Figure 5. Typical Solder Heating Profile

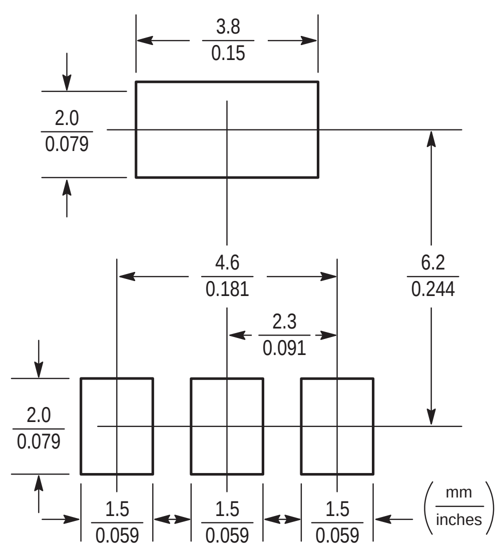
Footprints for Soldering



D2PAK



DPAK



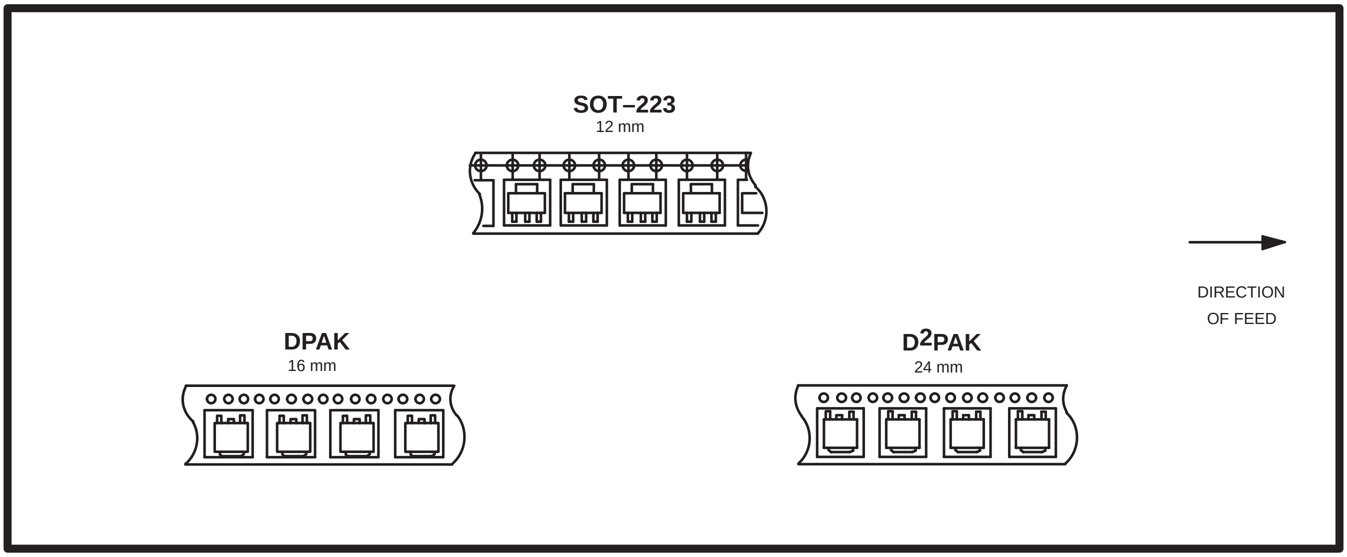
SOT 223

Tape and Reel Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel–back" cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- SOT–223 in 12 mm Tape
- DPAK in 16 mm Tape
- D^{2}PAK in 24 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

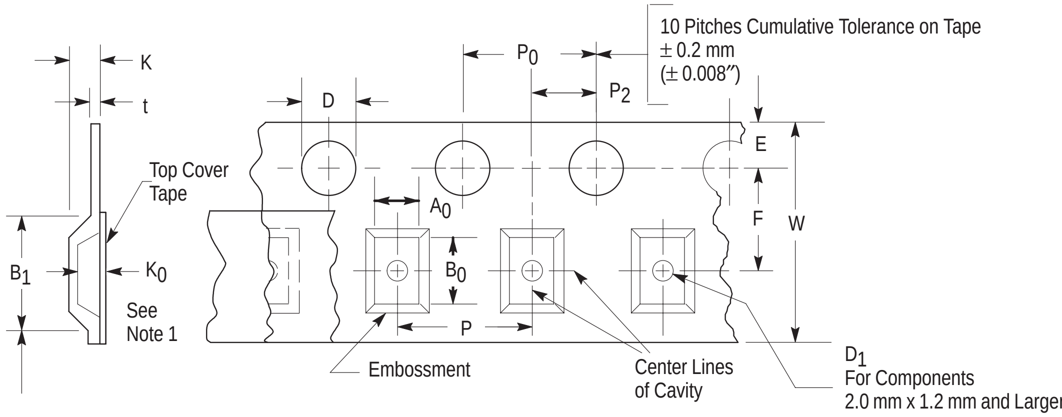


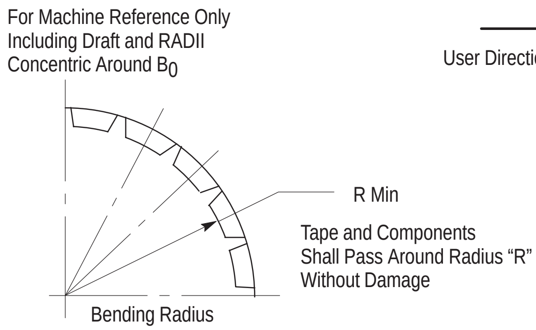
EMBOSSED TAPE AND REEL ORDERING INFORMATION

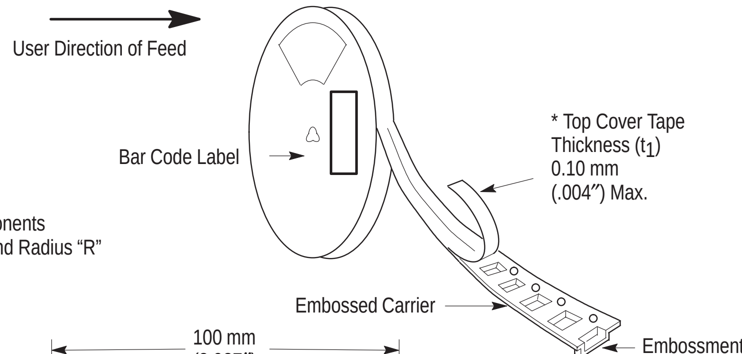
Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
DPAK	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	T4
D^{2}PAK	24	16.0 ± 0.1 (.630 ± .004)	330 (13)	800	T4
SOT–223	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
	12		330 (13)	4,000	T3

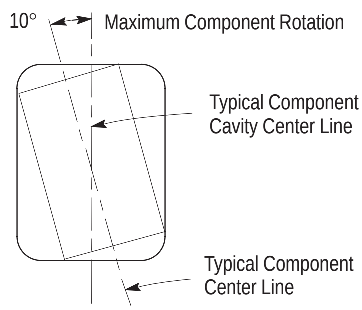
EMBOSSED TAPE AND REEL DATA FOR DISCRETES

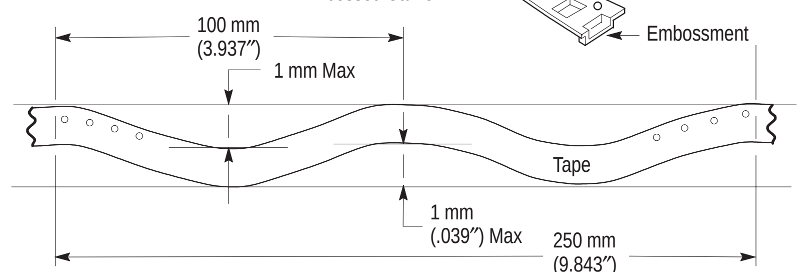
CARRIER TAPE SPECIFICATIONS











Camber (Top View)
Allowable Camber To Be 1 mm/100 mm Nonaccumulative Over 250 mm

DIMENSIONS

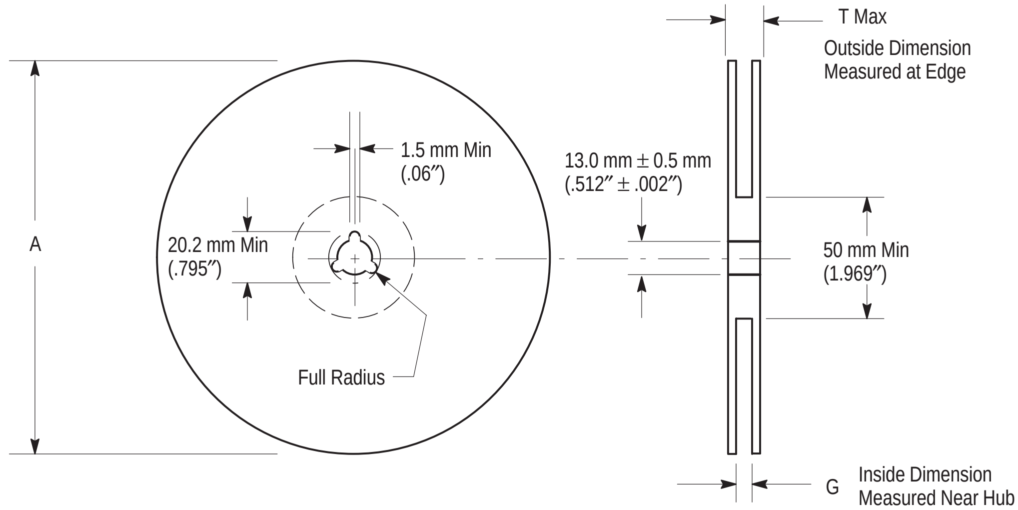
Tape Size	B_1 Max	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
12 mm	8.2 mm (.323″)	1.5 + 0.1 mm − 0.0 (.059 + .004″ − 0.0)	1.5 mm Min (.060″)	1.75 ± 0.1 mm (.069 ± .004″)	5.5 ± 0.05 mm (.217 ± .002″)	6.4 mm Max (.252″)	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .002″)	30 mm (1.18″)	0.6 mm (.024″)	12 ± .30 mm (.470 ± .012″)
16 mm	12.1 mm (.476″)				7.5 ± 0.10 mm (.295 ± .004″)	7.9 mm Max (.311″)					16.3 mm (.642″)
24 mm	20.1 mm (.791″)				11.5 ± 0.1 mm (.453 ± .004″)	11.9 mm Max (.468″)					24.3 mm (.957″)

Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 16–6.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, –0.0 (.49″ + .079″, –0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, –0.0 (.646″ + .078″, –0.00)	22.4 mm (.882″)
24 mm	360 mm (14.173″)	24.4 mm + 2.0 mm, –0.0 (.961″ + .070″, –0.00)	30.4 mm (1.197″)

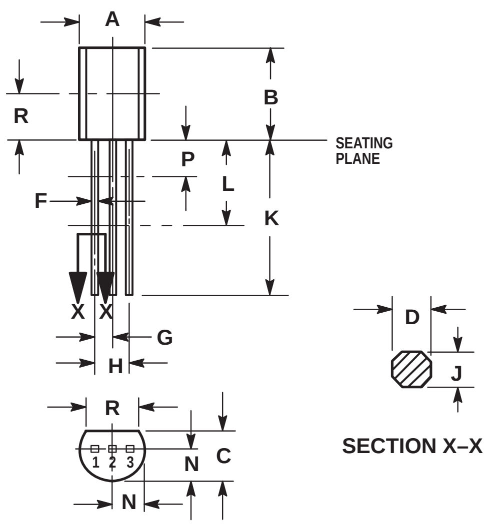
Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

Chapter Six

Package Outline Dimensions

Package Outline Dimensions

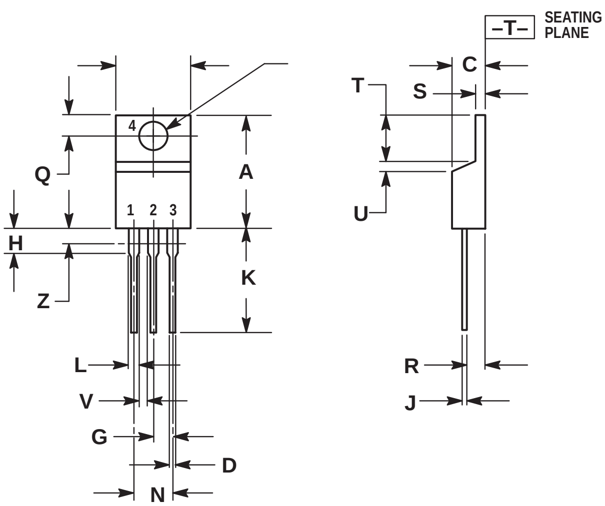


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MIMIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.022	0.46	0.56
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.135	—	3.43	—

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

CASE 029–05
(TO–226AE)
ISSUE AE



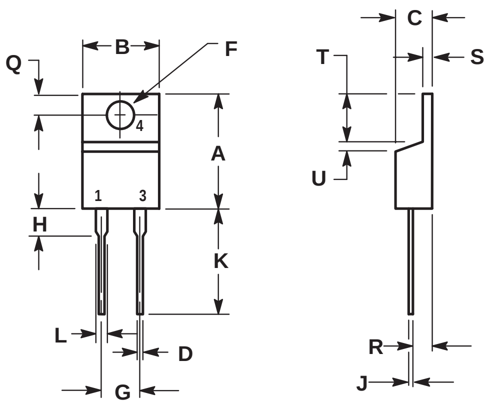
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–09
(TO–220AB)
ISSUE Z

PACKAGE OUTLINE DIMENSIONS (continued)

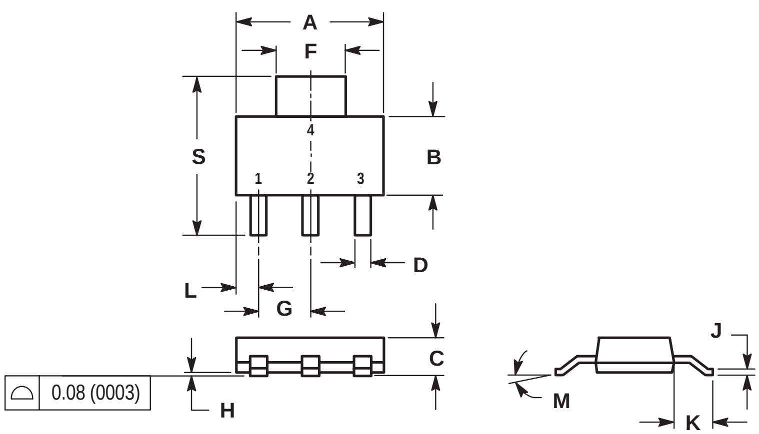


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.595	0.620	15.11	15.75
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.82
D	0.025	0.035	0.64	0.89
F	0.142	0.147	3.61	3.73
G	0.190	0.210	4.83	5.33
H	0.110	0.130	2.79	3.30
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.14	1.39
T	0.235	0.255	5.97	6.48
U	0.000	0.050	0.000	1.27

STYLE 1:
PIN 1. CATHODE
2. N/A
3. ANODE
4. CATHODE

CASE 221B–04
ISSUE C



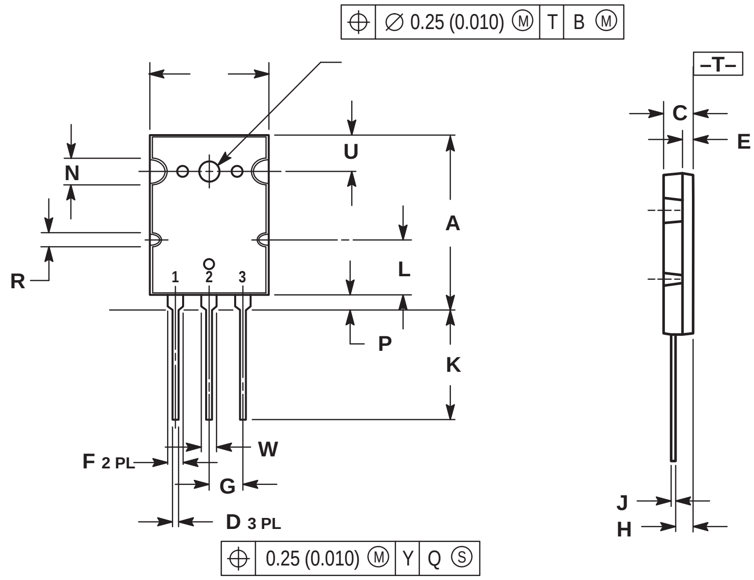
NOTES:
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0°	10°	0°	10°
S	0.264	0.287	6.70	7.30

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 318E–04
ISSUE J

PACKAGE OUTLINE DIMENSIONS (continued)

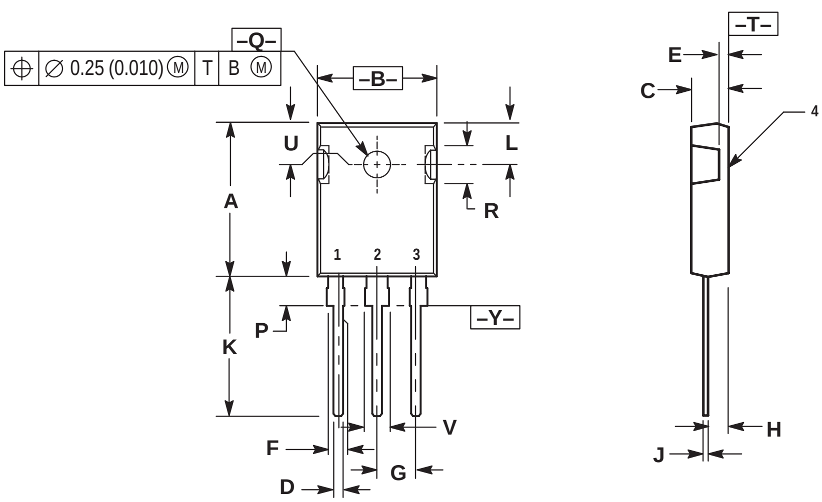


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

CASE 340G–02
ISSUE F

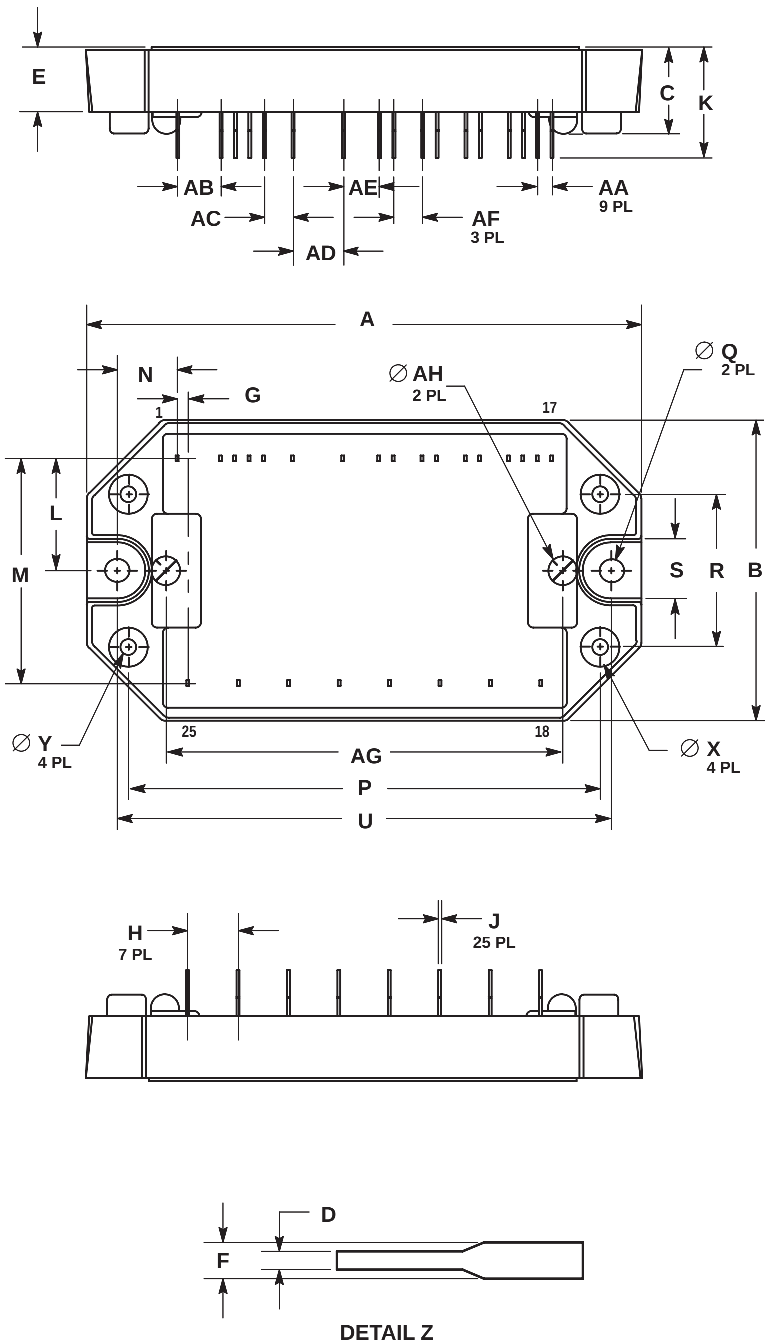


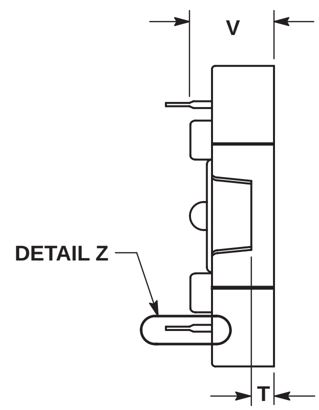
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340K–01
ISSUE A





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. LEAD LOCATION DIMENSIONS (ie: M, G. AA...) ARE TO THE CENTER OF THE LEAD.

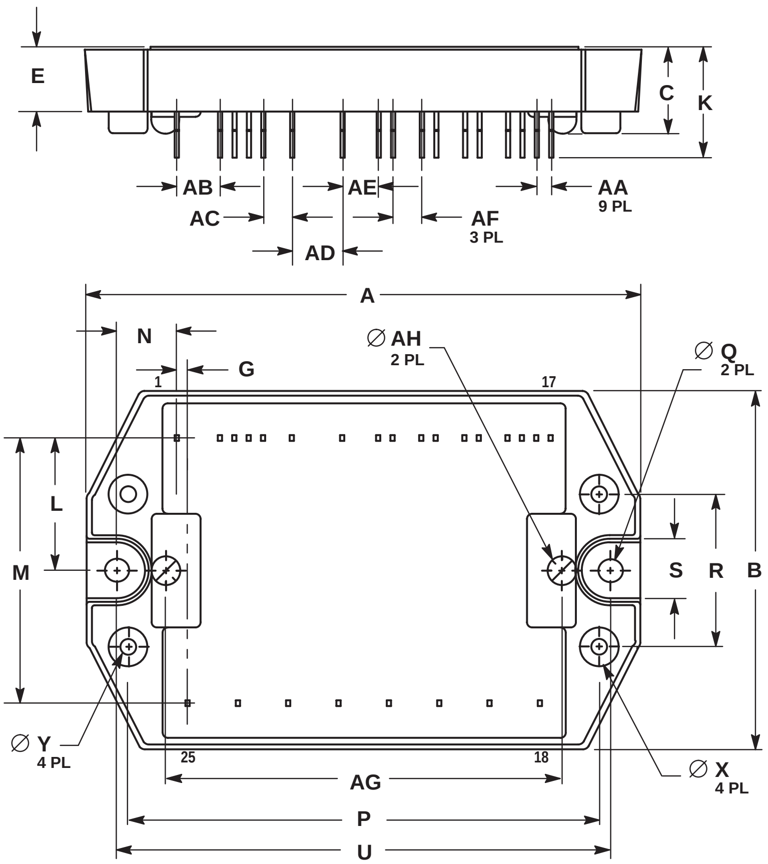
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	97.54	98.55	3.840	3.880
B	52.45	53.47	2.065	2.105
C	14.60	15.88	0.575	0.625
D	0.43	0.84	0.017	0.033
E	10.80	12.06	0.425	0.475
F	0.94	1.35	0.037	0.053
G	1.60	2.21	0.063	0.087
H	8.58	9.19	0.338	0.362
J	0.30	0.71	0.012	0.028
K	18.80	20.57	0.74	0.81
L	19.30	20.32	0.760	0.800
M	38.99	40.26	1.535	1.585
N	9.78	11.05	0.385	0.435
P	82.55	83.57	3.250	3.290
Q	4.01	4.62	0.158	0.182
R	26.42	27.43	1.040	1.080
S	12.06	12.95	0.475	0.515
T	4.32	5.33	0.170	0.210
U	86.36	87.38	3.400	3.440
V	14.22	15.24	0.560	0.600
X	6.55	7.16	0.258	0.282
Y	2.49	3.10	0.098	0.122
AA	2.24	2.84	0.088	0.112
AB	7.32	7.92	0.288	0.312
AC	4.78	5.38	0.188	0.212
AD	8.58	9.19	0.338	0.362
AE	6.05	6.65	0.238	0.262
AF	4.78	5.38	0.188	0.212
AG	69.34	70.36	2.730	2.770
AH	–––	5.08	–––	0.200

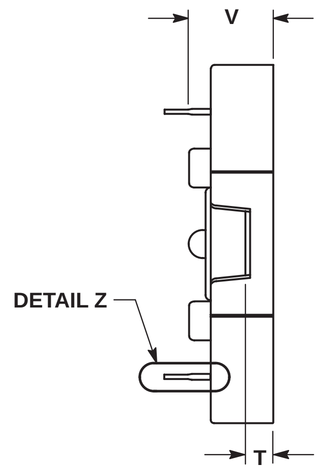
STYLE 1:

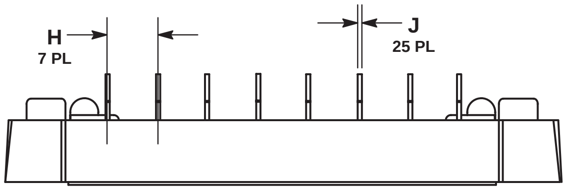
PIN 1. P1	PIN 6. N2	PIN 11. G3	PIN 16. G2	PIN 21. B
2. T–	7. P2	12. K5	17. G4	22. T
3. T+	8. K1	13. G5	18. W	23. S
4. I+	9. G1	14. G6	19. V	24. R
5. I–	10. K3	15. G7	20. U	25. N1

CASE 440–02
ISSUE A

PACKAGE OUTLINE DIMENSIONS (continued)







DETAIL Z

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. LEAD LOCATION DIMENSIONS (ie: M, G, AA...) ARE TO THE CENTER OF THE LEAD.

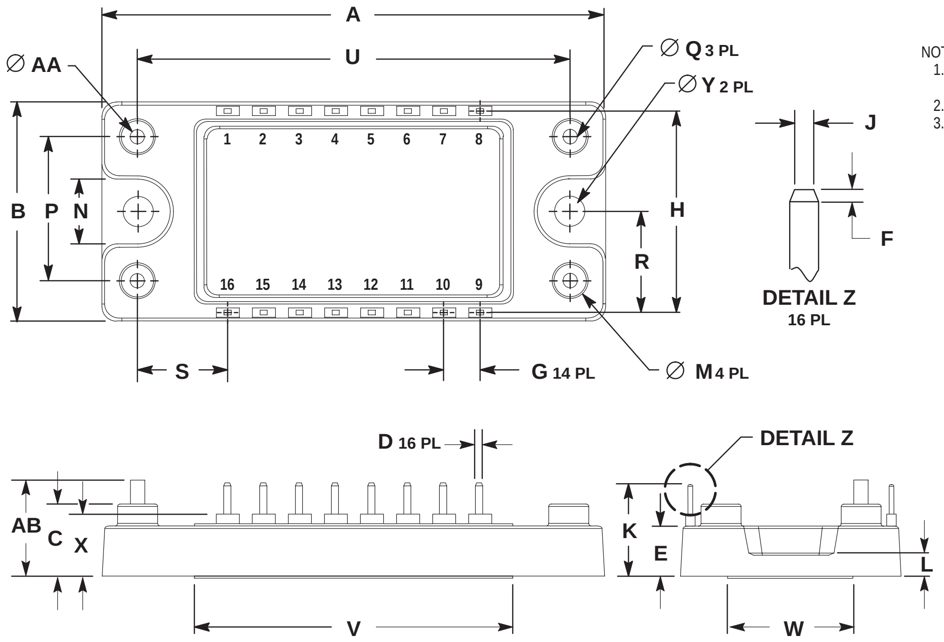
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	97.54	98.55	3.840	3.880
B	62.74	63.75	2.470	2.510
C	14.60	15.88	0.575	0.625
D	0.56	0.97	0.022	0.038
E	10.80	12.06	0.425	0.475
F	0.81	1.22	0.032	0.048
G	1.60	2.21	0.063	0.087
H	8.58	9.19	0.338	0.362
J	0.56	0.97	0.022	0.038
K	18.80	20.57	0.740	0.810
L	22.86	23.88	0.900	0.940
M	46.23	47.24	1.820	1.860
N	9.78	11.05	0.385	0.435
P	82.55	83.57	3.250	3.290
Q	4.01	4.62	0.158	0.182
R	26.42	27.43	1.040	1.080
S	12.06	12.95	0.475	0.515
T	4.32	5.33	0.170	0.210
U	86.36	87.38	3.400	3.440
V	14.22	15.24	0.560	0.600
X	6.55	7.16	0.258	0.282
Y	2.49	3.10	0.098	0.122
AA	2.24	2.84	0.088	0.112
AB	7.32	7.92	0.288	0.312
AC	4.78	5.38	0.188	0.212
AD	8.58	9.19	0.338	0.362
AE	6.05	6.65	0.238	0.262
AF	4.78	5.38	0.188	0.212
AG	69.34	70.36	2.730	2.770
AH	—	5.08	—	0.200

STYLE 1:

PIN 1. P1	PIN 6. N2	PIN 11. G3	PIN 16. G2	PIN 21. B
2. T–	7. P2	12. K5	17. G4	22. T
3. T+	8. K1	13. G5	18. W	23. S
4. I+	9. G1	14. G6	19. V	24. R
5. I–	10. K3	15. G7	20. U	25. N1

CASE 440A–02
ISSUE A

PACKAGE OUTLINE DIMENSIONS (continued)

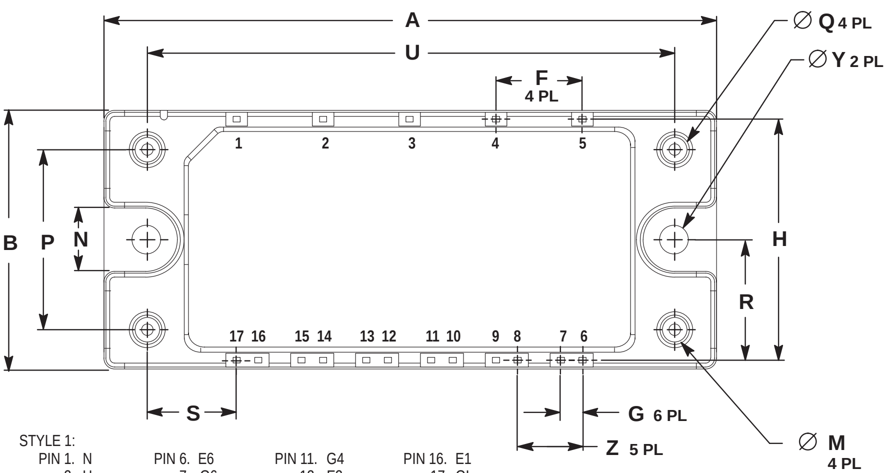


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. LEAD LOCATION DIMENSIONS (ie: G, S, R, H ...) ARE TO THE CENTER OF THE LEAD.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	88.39	89.41	3.480	3.520
B	38.35	39.37	1.510	1.550
C	12.32	13.59	0.485	0.535
D	0.89	1.65	0.035	0.065
E	8.64	9.65	0.340	0.380
F	0.13	0.64	0.005	0.025
G	5.97	6.73	0.235	0.265
H	33.91	34.67	1.335	1.365
J	0.41	1.22	0.016	0.048
K	16.26	17.27	0.640	0.680
L	3.71	4.72	0.146	0.186
M	5.46	6.48	0.215	0.255
N	10.92	11.94	0.430	0.470
P	24.89	25.91	0.980	1.020
Q	2.01	2.62	0.079	0.103
R	16.76	17.53	0.660	0.690
S	15.49	16.26	0.610	0.640
U	75.69	76.71	2.980	3.020
V	55.88	57.15	2.200	2.250
W	29.97	30.99	1.180	1.220
Y	5.26	5.77	0.207	0.227
X	11.30	12.07	0.445	0.475
AA	2.29	2.79	0.090	0.110
AB	16.26	17.27	0.640	0.680

CASE 464–03
ISSUE B

STYLE 1:
PIN 1. G1
2. E1
3. NC
4. G3
PIN 5. E3
6. G5
7. E5
8. NC
PIN 9. E6
10. G6
11. E4
12. G4
PIN 13. NC
14. E2
15. G2
16. P

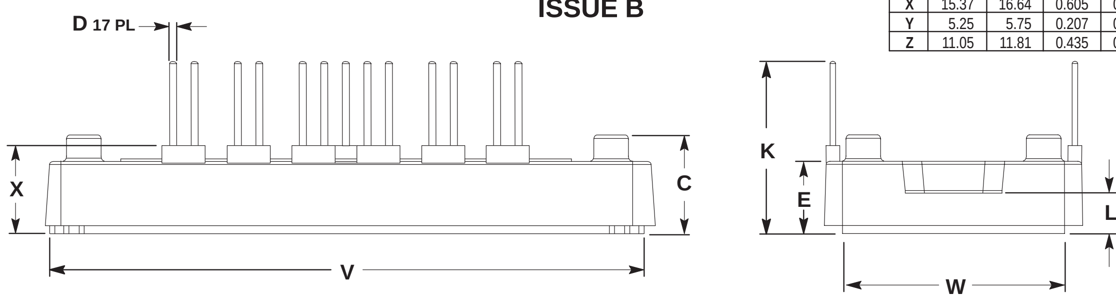


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. LEAD LOCATION DIMENSIONS (ie: G, S, R, H, F...) ARE TO THE CENTER OF THE LEAD.

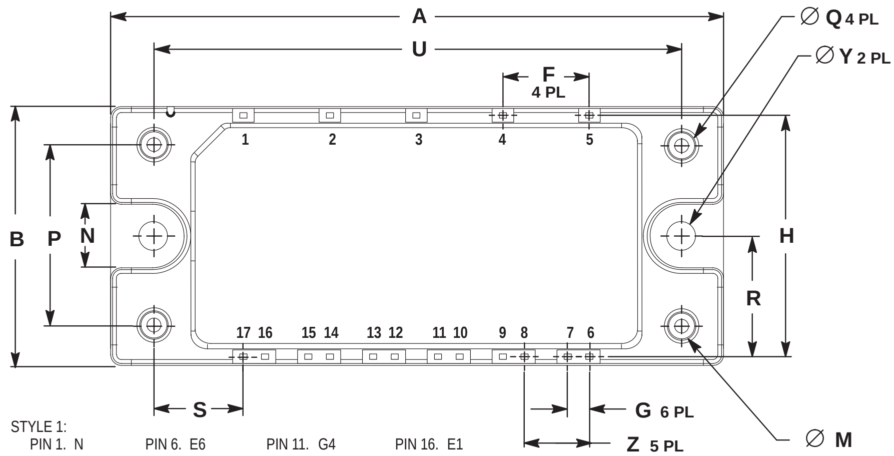
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	107.75	—	4.242
B	—	45.75	—	1.801
C	16.37	17.64	0.644	0.694
D	0.77	1.53	0.030	0.060
E	12.49	13.51	0.492	0.532
F	14.86	15.62	0.585	0.615
G	3.43	4.19	0.135	0.165
H	41.53	42.29	1.635	1.665
K	29.99	31.01	1.181	1.221
L	6.29	7.31	0.248	0.288
M	5.46	6.48	0.215	0.255
N	10.49	11.51	0.413	0.453
P	31.49	32.51	1.240	1.280
Q	2.00	2.60	0.079	0.103
R	20.57	21.33	0.810	0.840
S	15.62	16.38	0.615	0.645
U	92.49	93.51	3.641	3.681
V	104.17	105.44	4.101	4.151
W	37.49	38.51	1.476	1.516
X	15.37	16.64	0.605	0.655
Y	5.25	5.75	0.207	0.227
Z	11.05	11.81	0.435	0.465

STYLE 1:
PIN 1. N
2. U
3. V
4. W
5. P
PIN 6. E6
7. G6
8. E5
9. G5
10. E4
PIN 11. G4
12. E3
13. G3
14. E2
15. G2
PIN 16. E1
17. GI

CASE 464A–02
ISSUE B



PACKAGE OUTLINE DIMENSIONS (continued)



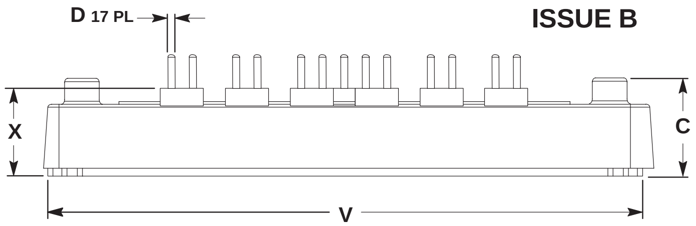
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. LEAD LOCATION DIMENSIONS (ie: G, S, R, H, F...) ARE TO THE CENTER OF THE LEAD.

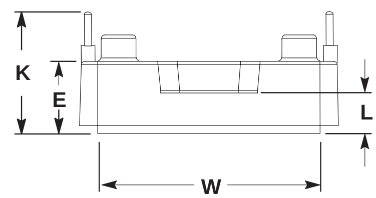
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	——	107.75	——	4.242
B	——	45.75	——	1.801
C	16.37	17.64	0.644	0.694
D	0.77	1.53	0.030	0.060
E	12.49	13.51	0.492	0.532
F	14.86	15.62	0.585	0.615
G	3.43	4.19	0.135	0.165
H	41.53	42.29	1.635	1.665
K	19.81	20.60	0.780	0.881
L	6.29	7.31	0.248	0.288
M	5.46	6.48	0.215	0.288
N	10.49	11.51	0.413	0.453
P	31.49	32.51	1.240	1.280
Q	2.00	2.60	0.079	0.103
R	20.57	21.33	0.810	0.840
S	15.62	16.38	0.615	0.645
U	92.49	93.51	3.641	3.681
V	104.17	105.44	4.101	4.151
W	37.49	38.51	1.476	1.516
X	15.37	16.64	0.605	0.655
Y	5.25	5.75	0.207	0.227
Z	11.05	11.81	0.435	0.465

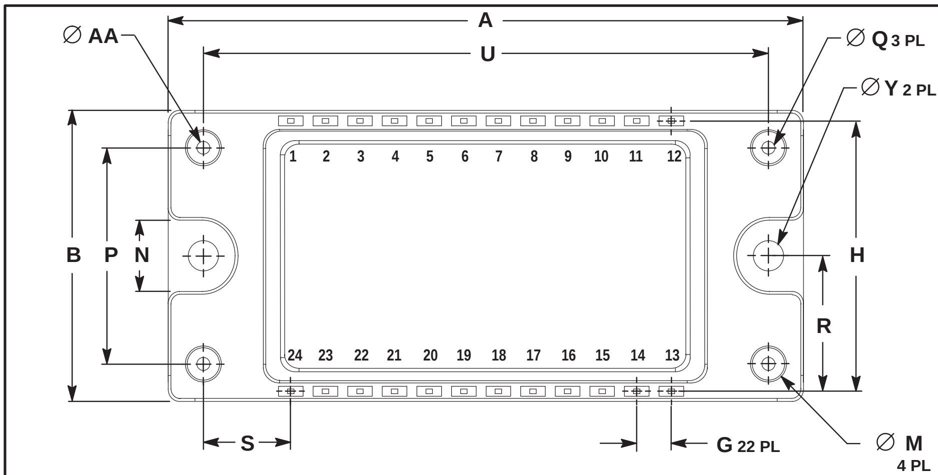
STYLE 1:

PIN 1. N	PIN 6. E6	PIN 11. G4	PIN 16. E1
2. U	7. G6	12. E3	17. GI
3. V	8. E5	13. G3	
4. W	9. G5	14. E2	
5. P	10. E4	15. G2	

CASE 464B–03
ISSUE B





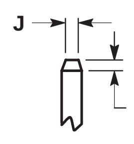


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. LEAD LOCATION DIMENSIONS (ie: P, Q, R, S...) ARE TO THE CENTER OF THE LEAD.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	111.51	112.52	4.390	4.430
B	50.93	51.94	2.005	2.045
C	12.32	13.59	0.485	0.535
D	0.89	1.65	0.035	0.065
E	8.64	9.65	0.340	0.380
F	0.13	0.64	0.005	0.025
G	5.97	6.73	0.235	0.265
H	46.48	47.50	1.830	1.870
J	0.41	1.22	0.016	0.048
K	16.26	17.27	0.640	0.680
L	3.71	4.72	0.146	0.186
M	5.46	6.48	0.215	0.255
N	10.92	11.94	0.430	0.470
P	37.60	38.60	1.480	1.520
Q	2.01	2.62	0.079	0.103
R	23.24	23.75	0.915	0.935
S	14.35	15.37	0.565	0.605
U	99.10	100.08	3.900	3.940
V	81.28	82.55	3.200	3.240
W	42.67	43.69	1.680	1.720
Y	5.15	5.77	0.203	0.227
X	11.30	12.07	0.445	0.475
AA	2.01	2.72	0.079	0.107
AB	16.26	17.27	0.640	0.680

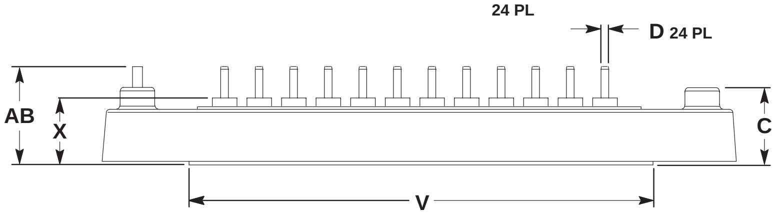
STYLE 1:

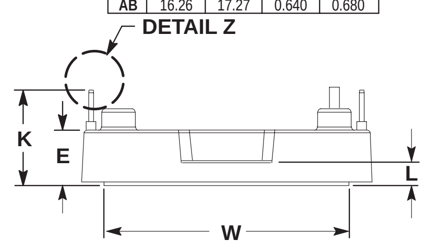
PIN 1. W	PIN 7. B+	PIN 13. P1	PIN 19. G6
2. G1	8. B–	14. TC+	20. C6
3. V	9. R	15. TC–	21. G4
4. G3	10. S	16. E7	22. E4
5. U	11. T	17. G7	23. G2
6. G5	12. N	18. P2	24. E2



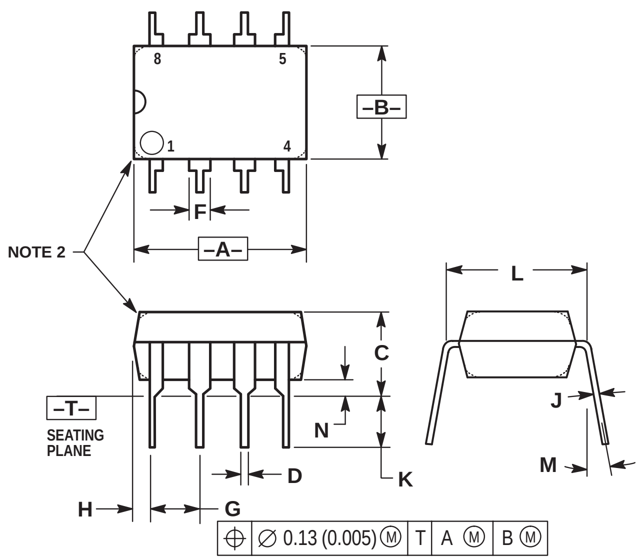
DETAIL Z
24 PL

CASE 464D–01
ISSUE O





PACKAGE OUTLINE DIMENSIONS (continued)

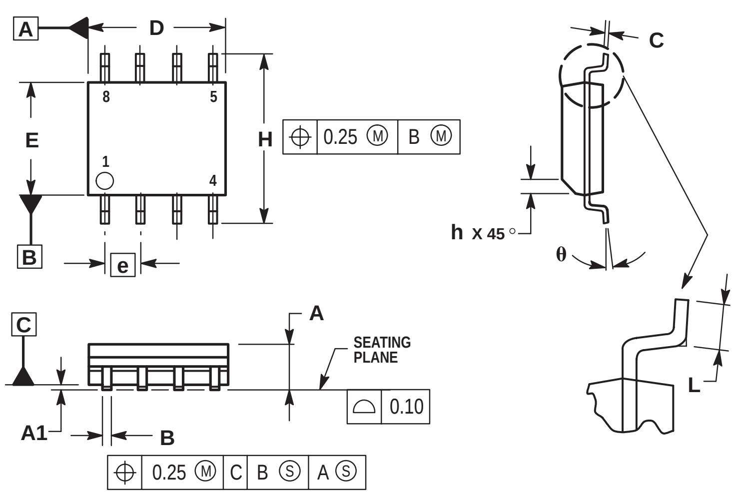


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

CASE 626–05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

CASE 751–06
ISSUE T

Chapter Seven

Distributors and Sales Offices

MOTOROLA AUTHORIZED DISTRIBUTOR & WORLDWIDE SALES OFFICES

NORTH AMERICAN DISTRIBUTORS

UNITED STATES

ALABAMA
Huntsville
Allied Electronics, Inc. .... (205)721–3500
Arrow Electronics .... (205)837–6955
FAI .... (205)837–9209
Future Electronics .... (205)830–2322
Hamilton/Hallmark .... (205)837–8700
Newark .... (205)837–9091
Wyle Electronics .... (205)830–1119
Mobile
Allied Electronics, Inc. .... (334)476–1875
ARIZONA
Phoenix
Allied Electronics, Inc. .... (602)831–2002
FAI .... (602)731–4661
Future Electronics .... (602)968–7140
Hamilton/Hallmark .... (602)736–7000
Wyle Electronics .... (602)804–7000
Tempe
Arrow Electronics .... (602)431–0030
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Arrow Zeus .... (714)581–4622
FAI .... (714)753–4778
Future Electronics .... (714)453–1515
Hamilton/Hallmark .... (714)789–4100
Wyle Laboratories Corporate .. (714)753–9953
Wyle Electronics .... (714)789–9953
Los Angeles
FAI .... (818)879–1234
Manhattan Beach
PENSTOCK .... (310)546–8953
Newberry Park
PENSTOCK .... (805)375–6680
Orange County
Allied Electronics, Inc. .... (714)727–3010
Palo Alto
Newark .... (415)812–6300
Rancho Cordova
Wyle Electronics .... (916)638–5282
Riverside
Allied Electronics, Inc. .... (909)980–6522
Newark .... (909)980–2105
Rocklin
Hamilton/Hallmark .... (916)632–4500
Roseville
Wyle Electronics .... (916)783–9953
Sacramento
Allied Electronics, Inc. .... (916)632–3104
FAI .... (916)782–7882
Newark .... (916)565–1760
San Diego
Allied Electronics, Inc. .... (619)279–2550
Arrow Electronics .... (619)565–4800
FAI .... (619)623–2888
Future Electronics .... (619)625–2800
Hamilton/Hallmark .... (619)571–7540
Newark .... (619)453–8211
PENSTOCK .... (619)623–9100
Wyle Electronics .... (619)558–6600
San Fernando Valley
Allied Electronics, Inc. .... (818)598–0130

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Allied Electronics, Inc. .... (408)383–0366
Arrow Electronics .... (408)441–9700
Arrow Electronics .... (408)428–6400
Arrow Zeus .... (408)629–4789
FAI .... (408)434–0369
Future Electronics .... (408)434–1122
Santa Clara
Wyle Electronics .... (408)727–2500
Santa Fe Springs
Newark .... (310)929–9722
Sierra Madre
PENSTOCK .... (818)355–6775
Sunnyvale
Hamilton/Hallmark .... (408)435–3600
PENSTOCK .... (408)730–0300
Thousand Oaks
Newark .... (805)449–1480
Woodland Hills
Hamilton/Hallmark .... (818)594–0404
COLORADO
Lakewood
FAI .... (303)237–1400
Future Electronics .... (303)232–2008
Denver
Allied Electronics, Inc. .... (303)790–1664
Newark .... (303)373–4540
Englewood
Arrow Electronics .... (303)799–0258
Hamilton/Hallmark .... (303)790–1662
PENSTOCK .... (303)799–7845
Thornton
Wyle Electronics .... (303)457–9953
CONNECTICUT
Bloomfield
Newark .... (203)243–1731
Cheshire
Allied Electronics, Inc. .... (203)272–7730
FAI .... (203)250–1319
Future Electronics .... (203)250–0083
Hamilton/Hallmark .... (203)271–5700
Wallingford
Arrow Electronics .... (203)265–7741
Wyle Electronics .... (203)269–8077
FLORIDA
Altamonte Springs
Future Electronics .... (407)865–7900
Clearwater
FAI .... (813)530–1665
Future Electronics .... (813)530–1222
Deerfield Beach
Arrow Electronics .... (305)429–8200
Wyle Electronics .... (954)420–0500
Ft. Lauderdale
FAI .... (954)428–9494
Future Electronics .... (954)426–4043
Hamilton/Hallmark .... (954)677–3500
Newark .... (954)486–1151
Jacksonville
Allied Electronics, Inc. .... (904)739–5920
Newark .... (904)399–5041
Lake Mary
Arrow Electronics .... (407)333–9300
Arrow Zeus .... (407)333–3055
Largo/Tampa/St. Petersburg
Hamilton/Hallmark .... (813)507–5000
Newark .... (813)287–1578
Wyle Electronics .... (813)576–3004
Miami
Allied Electronics, Inc. .... (305)558–2511
Maitland
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